

# **EXHIBIT L-21(a)**

IEEE 100

THE  
AUTHORITATIVE  
DICTIONARY  
OF IEEE STANDARDS TERMS  
SEVENTH EDITION



Published by  
Standards Information Network  
IEEE Press

# **IEEE 100**

# **The Authoritative Dictionary of**

# **IEEE Standards Terms**

**Seventh Edition**



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IEEE Press

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*Print: ISBN 0-7381-2601-2*

*SP1122*

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## Library of Congress Cataloging-in-Publication Data

IEEE 100 : the authoritative dictionary of IEEE standards terms.—7th ed.

p. cm.

ISBN 0-7381-2601-2 (paperback : alk. paper)

1. Electric engineering—Dictionaries. 2. Electronics—Dictionaries. 3. Computer engineering—Dictionaries. 4. Electric engineering—Acronyms. 5. Electronics—Acronyms. 6. Computer engineering—Acronyms. I. Institute of Electrical and Electronics Engineers.

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00-050601

(2) An address signaling method for PTS using 16 pairs of frequencies to represent digits and other characters. Although it is most commonly used by a station set to signal into a switching system, it may be used for signaling from a local switching system to another system for certain services. The DTMF codes are pairs of frequencies, each consisting of one out of four frequencies from a low group and one out of three or four frequencies from a mutually exclusive higher group. Performance is measured as tolerances for each frequency signaling level twist and timing. (COM/TA) 973-1990w

**dual-tone multifrequency pulsing (telephone switching systems)** A means of pulsing utilizing a simultaneous combination of one of a lower group of frequencies and one of a higher group of frequencies to represent each digit or character. (COM) 312-1977w

**dubbing (electroacoustics)** A term used to describe the combining of two or more sources of sound into a complete recording at least one of the sources being a recording. *See also:* phonograph pickup; rerecording. (SP) [32]

**duck tape** Tape of heavy cotton fabric, such as duck or drill, that may be impregnated with an asphalt, rubber, or synthetic compound. (T&D/PE) [10]

**duct (1)** A single enclosed raceway for conductors or cable. (T&D/NESC) C2-1997

(2) **(underground electric systems)** A single enclosed runway for conductors or cables. (T&D/PE) [10]

**duct bank (conduit run)** An arrangement of conduit providing one or more continuous ducts between two points. *Note:* An underground runway for conductors or cables, large enough for workmen to pass through, is termed a gallery or tunnel. (T&D/PE) [10]

**duct edge fair-lead (cable shield)** A collar or thimble, usually flared, inserted at the duct entrance in a manhole for the purpose of protecting the cable sheath or insulation from being worn away by the duct edge. (PE/T&D) [4], [10]

**duct entrance** The opening of a duct at a manhole, distributor box, or other accessible space. (T&D/PE) [10]

**ductility factor (seismic design of substations)** The ratio of the maximum displacement (ultimate) to the displacement that corresponds to initiation of the yielding. (PE/SUB) 693-1984s

**ducting (1)** Guided propagation of radio waves inside an atmospheric or tropospheric radio duct. *See also:* atmospheric radio duct. (AP/PROP) 211-1997

(2) Confinement of near-horizontally directed electromagnetic waves to a restricted horizontal layer in the atmosphere, resulting from a sufficiently steep negative vertical gradient of the atmospheric refractive index in a limited altitude region. *Note:* The region of steep gradient is not necessarily identical to the dimensions of the duct. *Synonyms:* trapping; super-refraction. (AES) 686-1997

**duct rodding (rodding a duct)** The threading of a duct by means of a jointed rod of suitable design for the purpose of pulling in the cable-pulling rope, mandrel, or the cable itself. (T&D/PE) [10]

**duct sealing** The closing of the duct entrance for the purpose of excluding water, gas, or other undesirable substances. (T&D/PE) [10]

**duct spacer (rotating machinery) (vent finger)** A spacer between adjacent packets of laminations to provide a radial ventilating duct. (PE) [9]

**duct system** A continuous passageway for the transmission of air which, in addition to ducts, may include duct fittings, dampers, plenums, fans, and accessory air handling equipment. (NESC/NEC) [86]

**duct ventilated (rotating machinery) (pipe ventilated)** A term applied to apparatus that is so constructed that a cooling gas can be conveyed to or from it through ducts. (PE) [9]

**DUI** *See:* duration of unscheduled interrupt.

**dumb terminal** A terminal that can only send and receive information; that is, one that is lacking in local processing

capability and built-in logic. *Contrast:* intelligent terminal.

(C) 610.10-1994w

**dumbwaiter** A hoisting and lowering mechanism equipped with a car that moves in guides in a substantially vertical direction, the floor area of which does not exceed 9 square feet, whose total inside height whether or not provided with fixed or removable shelves does not exceed 4 feet, the capacity of which does not exceed 500 pounds, and which is used exclusively for carrying materials. (EEC/PE) [119]

**dummy** Pertaining to a nonfunctioning item used to satisfy some format or logic requirement or to fulfill prescribed conditions. For example, a dummy report containing only titles and column headings with place-holding data instead of real data. (C) 610.5-1990w

(2) (A) Pertaining to a nonfunctional item used to satisfy some format or logic requirement or to fulfill prescribed conditions. *See also:* dummy instruction; dummy address. (B) Pertaining to an item such as a character, data item or statement that has the appearance of a specified item, but not the capacity to function as such. *Synonym:* placeholder. (C) 610.10-1994

**dummy address** A nonfunctional address used for illustration or instruction purposes. (C) 610.10-1994w

**dummy antenna** A device that has the necessary impedance characteristics of an antenna and the necessary power-handling capabilities, but that does not radiate or receive radio waves. *Note:* In receiver practice, that portion of the impedance not included in the signal generator is often called dummy antenna. *See also:* radio receiver. 188-1952w

**dummy-antenna system** An electric network that simulates the impedance characteristics of an antenna system. *See also:* navigation. (AES/GCS) 173-1959w

**dummy coil (rotating machinery)** A coil that is not required electrically in a winding, but that is installed for mechanical reasons and left unconnected. *See also:* rotor; stator. (PE) [9]

**dummy data** Data that is used to satisfy some format or logic requirement or to fulfill prescribed conditions. For example, an artificial character used as a placeholder variable within a program. (C) 610.5-1990w

**dummy finger** A passive electrode that may be included in an interdigital transducer in order to suppress wavefront distortion. (UFFC) 1037-1992w

**dummy instruction (A)** An item of data, in the form of an instruction, that requires modification before being executed. *Synonyms:* do-nothing instruction; no-op instruction. (B) An item of data, in the form of an instruction, that is inserted into a sequence of instructions, but that is not intended to be executed. (C) 610.10-1994

**dummy load (radio transmission)** A dissipative but essentially nonradiating substitute device having impedance characteristics simulating those of the substituted device. *See also:* artificial load; radio transmission. (IM/HFIM) [40]

**dummy parameter** *See:* formal parameter.

**dump (A) (computers)** To copy the contents of all or part of a storage, usually from an internal storage into an external storage. (B) **(computers)** A process as in definition (A). (C) **(computers)** The data resulting from the process as in definition (A). *See also:* static dump; selective dump; dynamic dump; snapshot dump. (MIL) [2]

(2) (A) **(software)** A display of some aspect of a computer program's execution state, usually the contents of internal storage or registers. Types include change dump, dynamic dump, memory dump, postmortem dump, selective dump, snapshot dump; static dump. (B) **(software)** A display of the contents of a file or device. (C) **(software)** To copy the contents of internal storage to an external medium. (D) **(software)** To produce a display or copy as in definitions (A), (B), or (C). (C) 610.12-1990

**dump energy (1)** Energy generated from any source that cannot be stored and that is beyond the immediate needs of the electric system producing the energy. (PE/PSE) 858-1993w

# **EXHIBIT L-22**

**EX. L-22**  
**LGD US PATENT NO. 5,748,266**

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**EXHIBIT L-22**  
**U.S. PATENT NO. 5,748,266**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 1**

1. A color filter and common electrode carried by a facing substrate for assembly with an array substrate to form a liquid crystal display panel, the color filter comprising a plurality of pillars formed higher than other portions of the color filter for contact with objects formed on the array substrate to specify a cell gap, wherein the pillars are covered with the common electrode.

**ASSERTED CLAIM 3**

3. A liquid crystal display panel comprising:  
 an array substrate having pixel electrodes arranged like a matrix, an active element for each of the pixel electrodes, a storage capacitance provided at some of the pixel electrodes, and a storage capacitance line for outputting the reference potential of the storage capacitance;  
 a facing substrate having a plurality of pillars arranged so as to face the array substrate, the pillars being formed higher than other portions of the facing substrate, the pillars together with objects formed on the array substrate that face the pillars specifying a cell gap, and a common electrode for all pixels covering at least some of the pillars, the common electrode being electrically connected to the storage capacitance line at the portions of the common electrode covering the pillars; and  
 a liquid crystal layer held between the array substrate and the facing substrate.

**LGD's Claim Construction**

**common electrode<sup>1</sup>** - a conductor, typically made of a transparent material, on the color filter substrate that receives a reference voltage relative to the pixel electrode voltages

**common electrode for all pixels covering at least some of the pillars<sup>2</sup>** - the common electrode is formed on the protruded surface of at least some of the pillars

**the common electrode being electrically connected to the storage capacitance line at the portions of the common electrode covering the pillars** - the common electrode is electrically connected to the storage capacitance line in the pixel area where the pillars covered with the common electrode contact the objects on the array substrate

<sup>1</sup> Disputed Term "common electrode" also appears in asserted claims 6, and 7 the same context.

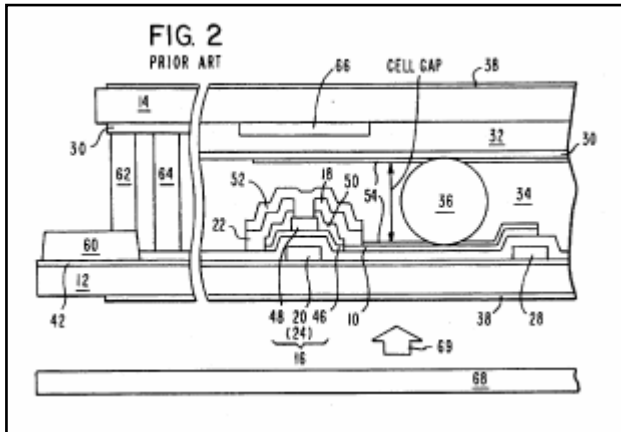
<sup>2</sup> Disputed Term "common electrode for all pixels covering at least some of the pillars" also appears in asserted claim 7 in the same context.

**INTRINSIC EVIDENCE FOR DISPUTED TERM “COMMON ELECTRODE”**

To prevent a signal delay of an active-matrix liquid crystal display from occurring in an active-matrix liquid crystal display having an active element for each pixel electrode, a potential is supplied to a common electrode from a storage capacitance line by forming a pillar of a color filter to specify a cell gap between an array substrate having the storage capacitance line and a facing substrate having the color filter and electrically connecting the common electrode covering the pillar of the color filter with the storage capacitance line on the array substrate. Thereby, it is possible to disuse a transfer dotting process which is a factor of decreasing the yield and also a factor of decreasing the effective display area. Moreover, because the potential is supplied to the common electrode from the storage capacitance line, it is possible to prevent a signal delay of the common electrode from occurring and moreover realize a high-image-quality screen even in a large and high-definition liquid crystal display without causing irregularity of a display screen or decrease of a contrast ratio.

Abstract

**INTRINSIC EVIDENCE FOR DISPUTED TERM “COMMON ELECTRODE” (cont’d):**



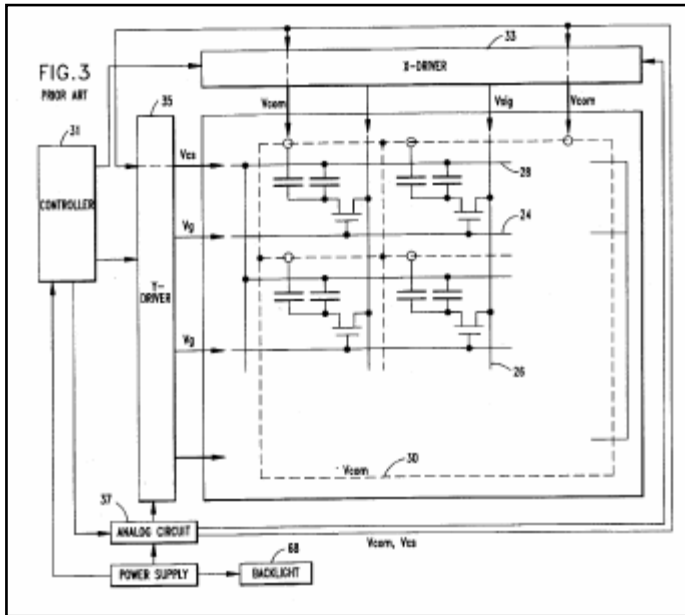
Among these layers and films, the undercoat layer 42, channel protective layer 48, passivation film 52, and alignment film 54 may not be deposited. A common electrode 30 is formed at the facing substrate 14 side of the TFT-LCD correspondingly to an area in which pixel electrodes 10 on the array substrate 12 are arranged like a matrix. Input signals are supplied to an OLB (Outer Lead Bonding) electrode 60 extended from a pixel area in which the pixel electrode 10 on the array substrate 12 is formed up to the perimeter of the area. Among the potentials of these signals, the potential of the common electrode 30 on the facing substrate is supplied from a plurality of portions of electrodes on the array substrate through a transfer 62 using

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conductive paste at the outside of the pixel area. The common electrode 30 is made of a transparent material such as ITO (Indium Tin Oxide) because it is necessary to pass light through the electrode 30. However, because the material has a large electric resistance, the electric resistance

1:57 - 2:4

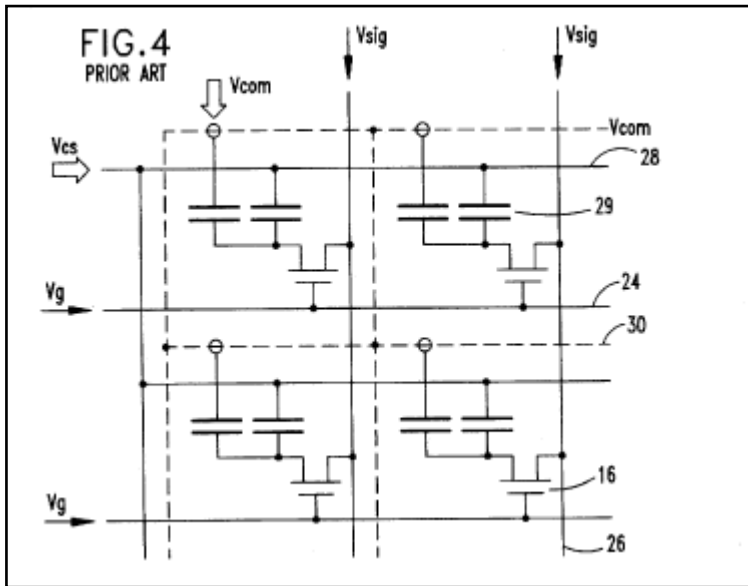
**INTRINSIC EVIDENCE FOR DISPUTED TERM “COMMON ELECTRODE” (cont’d):**



FIGS. 3 and 4 show an equivalent circuit of an existing TFT-LCD. An input signal supplied to the existing TFT-LCD is described below by referring to FIGS. 3 and 4. A controller 31 converts image data into a form to be supplied to an X-driver 33 and a Y-driver 35 of a driver IC. Moreover, an analog circuit 37 generates a voltage for each input signal. Input signals to be supplied to the TFT-LCD include a scanning signal ( $V_g$ ) of a gate line 24 supplied from the Y-driver 35, a display signal ( $V_{sig}$ ) of a data line 26 supplied from the X-driver 33, a common-electrode potential ( $V_{com}$ ) of a common electrode 30, and a storage capacitance line potential ( $V_{cs}$ ) of a storage capacitance line 28. The potentials of these input signals are all supplied to the OLB electrode 60 extended from the pixel area in which the pixel electrodes 10 on the array substrate 12 are formed up to the perimeter of the area as shown in FIG. 2. Then, among the potentials of these input signals, the potential  $V_{com}$  is supplied to the common electrode 30 through the transfer 62.

2:25-42

**INTRINSIC EVIDENCE FOR DISPUTED TERM “COMMON ELECTRODE” (cont’d):**



FIGS. 3 and 4 show an equivalent circuit of an existing TFT-LCD. An input signal supplied to the existing TFT-LCD is described below by referring to FIGS. 3 and 4. A controller 31 converts image data into a form to be supplied to an X-driver 33 and a Y-driver 35 of a driver IC. Moreover, an analog circuit 37 generates a voltage for each input signal. Input signals to be supplied to the TFT-LCD include a scanning signal ( $V_g$ ) of a gate line 24 supplied from the Y-driver 35, a display signal ( $V_{sig}$ ) of a data line 26 supplied from the X-driver 33, a common-electrode potential ( $V_{com}$ ) of a common electrode 30, and a storage capacitance line potential ( $V_{cs}$ ) of a storage capacitance line 28. The potentials of these input signals are all supplied to the OLB electrode 60 extended from the pixel area in which the pixel electrodes 10 on the array substrate 12 are formed up to the perimeter of the area as shown in FIG. 2. Then, among the potentials of these input signals, the potential  $V_{com}$  is supplied to the common electrode 30 through the transfer 62.

2:25-42

**INTRINSIC EVIDENCE FOR DISPUTED TERM “COMMON ELECTRODE” (cont'd):**

A driving method in which a polarity is inverted because the potential of a common electrode at the facing substrate side synchronizes with the display signal Vsig is referred to as common-voltage AC inversion driving (Vcom inversion) which is distinguished from a method in which common voltage is constant. The Vcom inversion driving has an advantage that the maximum voltage amplitude of the

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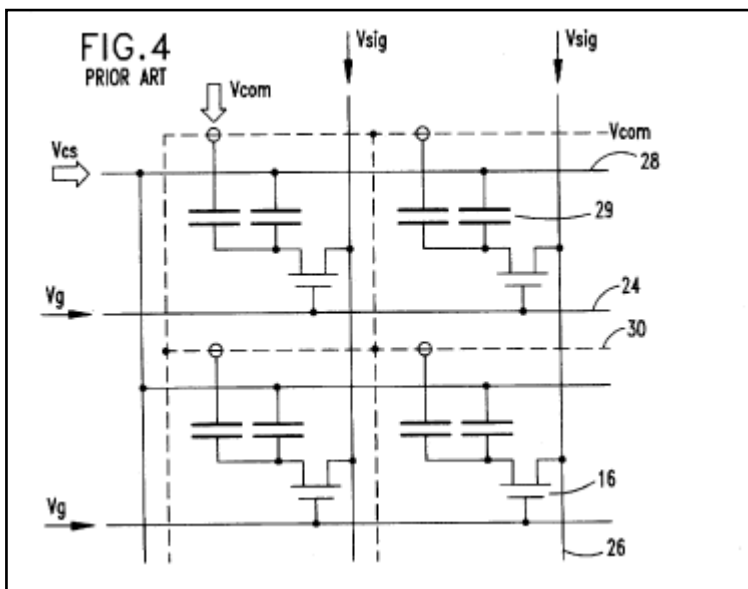
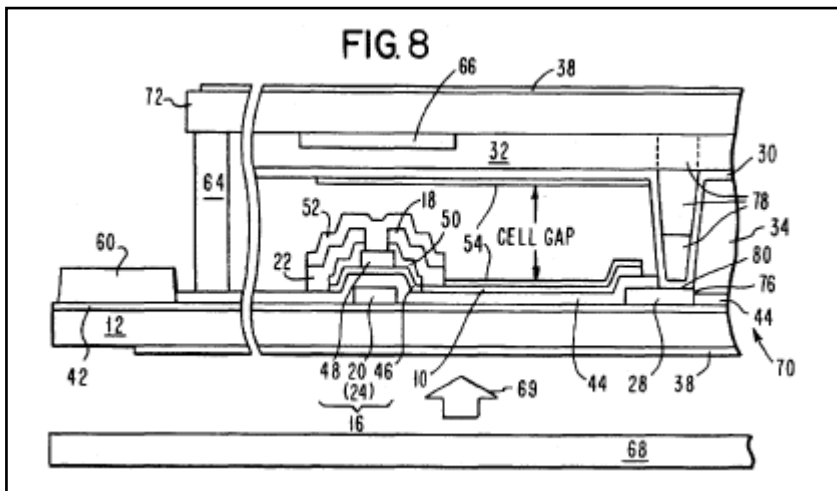
display signal Vsig can be decreased because the voltage amplitude of the common electrode biased to the voltage amplitude of the display signal Vsig is applied to a liquid crystal layer. It is requested from the market of the TFT-LCD

2:61 - 3:4

According to the present invention, the potential of the storage capacitance line 28 is supplied to the common electrode 30 on a facing substrate from joints formed everywhere in a pixel area. Originally, the common-

5:7-10

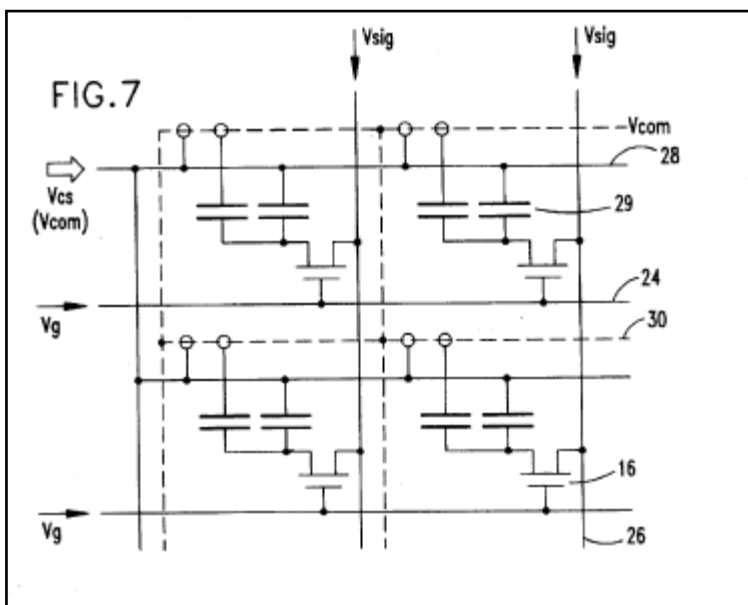
**INTRINSIC EVIDENCE FOR DISPUTED TERM “COMMON ELECTRODE” (cont'd):**



Furthermore, as shown in FIG. 8, the embodiment 1 may have a structure in which the gate insulating film 44 is formed on the storage capacitance line 28 in a pixel area on the array substrate 12. That is, the embodiment 1 has a structure in which a hole 76 is formed at part of the gate insulating film 44 on the storage capacitance line 28, the common electrode 30 at a portion covering the pillar 78 of a color filter formed on the color filter substrate 72 is overlapped with the position of the hole 76, and the common electrode 30 contacts the storage capacitance line 28 so that they are electrically connected each other. Though the

7:4-13

**INTRINSIC EVIDENCE FOR DISPUTED TERM “COMMON ELECTRODE” (cont'd):**



As another method for connecting a common electrode with a storage capacitance line, the storage capacitance line 28 may be formed on the pixel electrode 10 formed on the array substrate 12 through the insulating film 74. In this case, a joint 80 between the storage capacitance line 28 and the common electrode 30 covering the pillar 78 of a color filter is three-dimensionally superimposed on a storage capacitance area 82.

In the case of the third embodiment, a layer 84 made of a conductive body such as a metal formed simultaneously with the data line 26 is first formed on the storage capacitance line 28, and then it is connected with the common electrode 30 to constitute the joint 80 instead of directly connecting the common electrode 30 to the storage capacitance line 28 like the first and second embodiments. Therefore, it is possible to perform fine adjustment for realizing an optically-optimized cell gap by the formation of the conductive body.

7:44-61

**INTRINSIC EVIDENCE FOR DISPUTED TERM “COMMON ELECTRODE” (cont'd):**

Then, the process for manufacturing the liquid crystal display panel **70** of this embodiment is described below.

First, the process for manufacturing the array substrate **12** is described below.

In the first process, the undercoat layer **42** is formed on the array substrate **12**.

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In the second process, the gate electrode **20**, gate line **24**, and storage capacitance line **28** are formed on the undercoat layer **42**.

In the third process, the gate insulating film **44** is formed.

In the fourth process, the semiconductor layer **46** of the TFT **16** is formed.

In the fifth process, the pixel electrode **10** is formed.

In the sixth process, the hole **76** is formed on part of the gate insulating film **44** on the storage capacitance line **28**.

In the seventh process, the source electrode **18** and drain electrode **22** of the TFT **16** and the data line **26** are formed.

In the eighth process, the passivation film **52** covering the TFT **16** is formed.

In the ninth process, the alignment film **54** is formed and treated through rubbing.

Then, the method for manufacturing the color filter substrate **72** is described below.

In the first process, the color filter **32** is formed on the facing substrate **14**, and the pillar **78** of a color filter is formed at a position corresponding to the hole **76** on the array substrate **12**.

In the second process, the common electrode **30** is formed on the color filter **32**.

In the third process, the alignment film **54** is formed and treated through rubbing.

The array substrate **12** and the color filter substrate **77** finished through the above processes are made to face each other and the storage capacitance line **28** viewed through the hole **76** on the array substrate **12** is overlapped with the common electrode **30** at the portion covering the pillar **78** of a color filter on the facing substrate **14** to electrically connect them each other.

Then, the liquid crystal display panel **70** is finished by sealing the perimeter of the assembly with a sealant **64**, injecting liquid crystal into the assembly through an injection hole (not illustrated), and closing the injection hole.

7:62-8:39

**INTRINSIC EVIDENCE FOR DISPUTED TERM “COMMON ELECTRODE” (cont'd):**

The present invention provides a large high-definition liquid crystal display without causing a signal delay even around the central portion of a common electrode. Moreover, because the present invention disuses processes for scattering spacers and dotting transfers, the yield is improved and the cost is decreased.

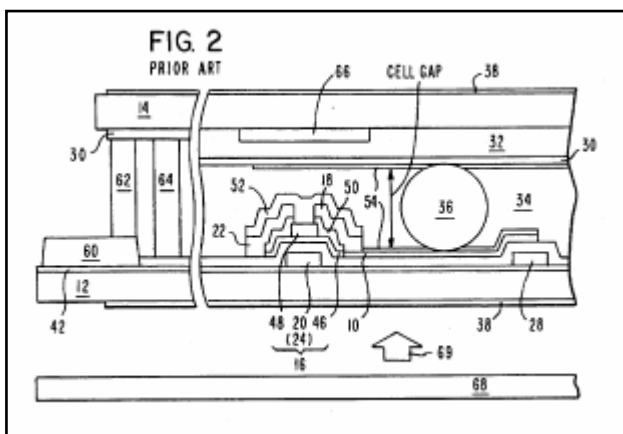
8:39-45

**INTRINSIC EVIDENCE FOR DISPUTED TERM “COMMON ELECTRODE” (cont'd):**

It is said to be unclear in Claims 1 and 5 which elements are “formed higher than other portions” and specify “a cell gap together with objects formed on the array substrate”. These elements are the pillars, which are now expressly identified. It is asked also which elements are electrically connected to the storage capacitance line. The answer is the portions of the common electrode covering at least some of the pillars. This has been clarified as well. The phrase “working on all pixels” is said to be not understood. This phrase merely refers to the fact that the common electrode is the common electrode for all of the pixels. This phrase has been deleted and the concept moved forward in Claims 1 and 5.

App. 08/615,012, 08/05/1997  
Amendment, pg. 6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “COMMON ELECTRODE FOR ALL PIXELS COVERING AT LEAST SOME OF THE PILLARS”:**



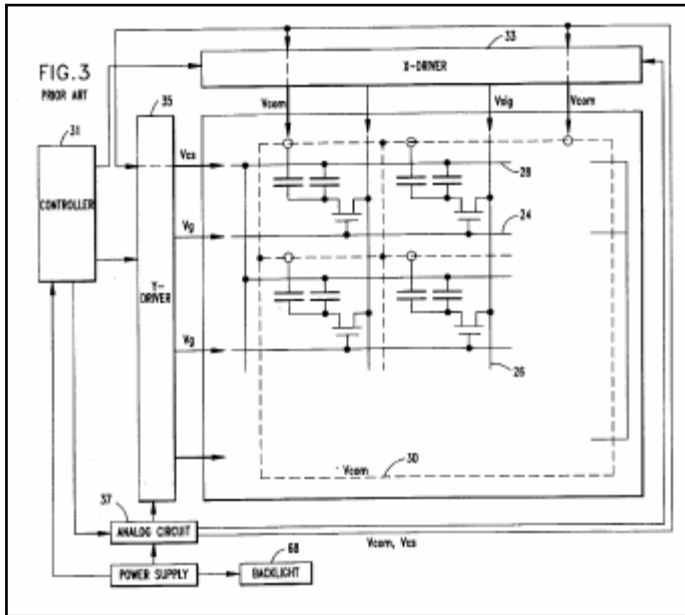
Among these layers and films, the undercoat layer 42, channel protective layer 48, passivation film 52, and alignment film 54 may not be deposited. A common electrode 30 is formed at the facing substrate 14 side of the TFT-LCD correspondingly to an area in which pixel electrodes 10 on the array substrate 12 are arranged like a matrix. Input signals are supplied to an OLB (Outer Lead Bonding) electrode 60 extended from a pixel area in which the pixel electrode 10 on the array substrate 12 is formed up to the perimeter of the area. Among the potentials of these signals, the potential of the common electrode 30 on the facing substrate is supplied from a plurality of portions of electrodes on the array substrate through a transfer 62 using

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conductive paste at the outside of the pixel area. The common electrode 30 is made of a transparent material such as ITO (Indium Tin Oxide) because it is necessary to pass light through the electrode 30. However, because the material has a large electric resistance, the electric resistance

1:57 - 2:4

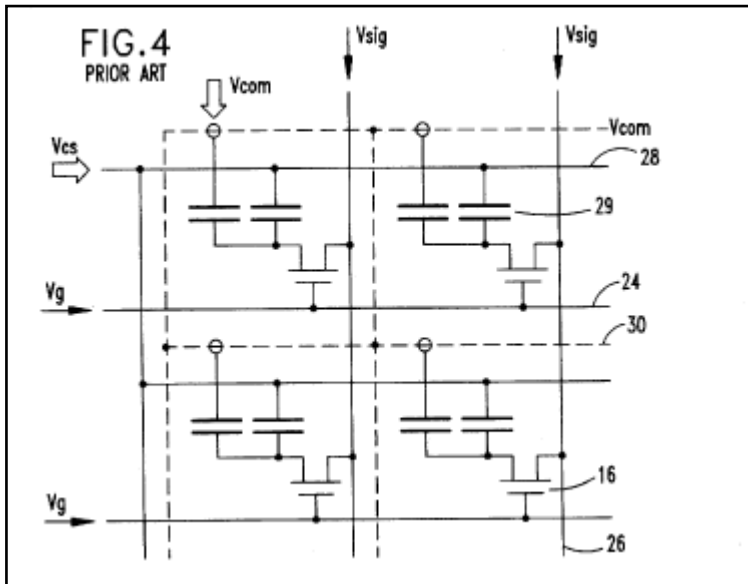
**INTRINSIC EVIDENCE FOR DISPUTED TERM “COMMON ELECTRODE FOR ALL PIXELS COVERING AT LEAST SOME OF THE PILLARS” (cont’d):**



FIGS. 3 and 4 show an equivalent circuit of an existing TFT-LCD. An input signal supplied to the existing TFT-LCD is described below by referring to FIGS. 3 and 4. A controller 31 converts image data into a form to be supplied to an X-driver 33 and a Y-driver 35 of a driver IC. Moreover, an analog circuit 37 generates a voltage for each input signal. Input signals to be supplied to the TFT-LCD include a scanning signal ( $V_g$ ) of a gate line 24 supplied from the Y-driver 35, a display signal ( $V_{sig}$ ) of a data line 26 supplied from the X-driver 33, a common-electrode potential ( $V_{com}$ ) of a common electrode 30, and a storage capacitance line potential ( $V_{cs}$ ) of a storage capacitance line 28. The potentials of these input signals are all supplied to the OLB electrode 60 extended from the pixel area in which the pixel electrodes 10 on the array substrate 12 are formed up to the perimeter of the area as shown in FIG. 2. Then, among the potentials of these input signals, the potential  $V_{com}$  is supplied to the common electrode 30 through the transfer 62.

2:25-42

**INTRINSIC EVIDENCE FOR DISPUTED TERM “COMMON ELECTRODE FOR ALL PIXELS COVERING AT LEAST SOME OF THE PILLARS” (cont’d):**



FIGS. 3 and 4 show an equivalent circuit of an existing TFT-LCD. An input signal supplied to the existing TFT-LCD is described below by referring to FIGS. 3 and 4. A controller 31 converts image data into a form to be supplied to an X-driver 33 and a Y-driver 35 of a driver IC. Moreover, an analog circuit 37 generates a voltage for each input signal. Input signals to be supplied to the TFT-LCD include a scanning signal (Vg) of a gate line 24 supplied from the Y-driver 35, a display signal (Vsig) of a data line 26 supplied from the X-driver 33, a common-electrode potential (Vcom) of a common electrode 30, and a storage capacitance line potential (Vcs) of a storage capacitance line 28. The potentials of these input signals are all supplied to the OLB electrode 60 extended from the pixel area in which the pixel electrodes 10 on the array substrate 12 are formed up to the perimeter of the area as shown in FIG. 2. Then, among the potentials of these input signals, the potential Vcom is supplied to the common electrode 30 through the transfer 62.

2:25-42

**INTRINSIC EVIDENCE FOR DISPUTED TERM “COMMON ELECTRODE FOR ALL PIXELS COVERING AT LEAST SOME OF THE PILLARS” (cont’d):**

A driving method in which a polarity is inverted because the potential of a common electrode at the facing substrate side synchronizes with the display signal Vsig is referred to as common-voltage AC inversion driving (Vcom inversion) which is distinguished from a method in which common voltage is constant. The Vcom inversion driving has an advantage that the maximum voltage amplitude of the

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display signal Vsig can be decreased because the voltage amplitude of the common electrode biased to the voltage amplitude of the display signal Vsig is applied to a liquid crystal layer. It is requested from the market of the TFT-LCD

2:61 - 3:4

Moreover, as shown in FIG. 2, the existing TFT-LCD has a problem in the structure of supplying the potential of the common electrode 30 on the facing substrate 14 from a plurality of portions at the perimeter of a pixel area of the array substrate 12 side to the common electrode 30 on the facing substrate 14 through the transfer 62 using conductive paste. Because this structure requires a high-accuracy alignment of the transfer 62, it uses two or more transfers to prevent defectives from being produced due to a deviation of a transfer. However, the manufacturing yield is decreased due to defectives produced in a process for dotting a transfer. Moreover, there is the restriction on design that an area for dotting a transfer must be formed at the perimeter of a pixel area. That is, because an area independent of display must exclusively be formed on the array substrate 12 and the facing substrate 14, an effective display area to a substrate size is decreased. However, it is inevitable to use the above structure because it is indispensable for an existing liquid crystal display in view of design.

4:31-49

**INTRINSIC EVIDENCE FOR DISPUTED TERM “COMMON ELECTRODE FOR ALL PIXELS COVERING AT LEAST SOME OF THE PILLARS” (cont’d):**

**SUMMARY OF THE INVENTION**

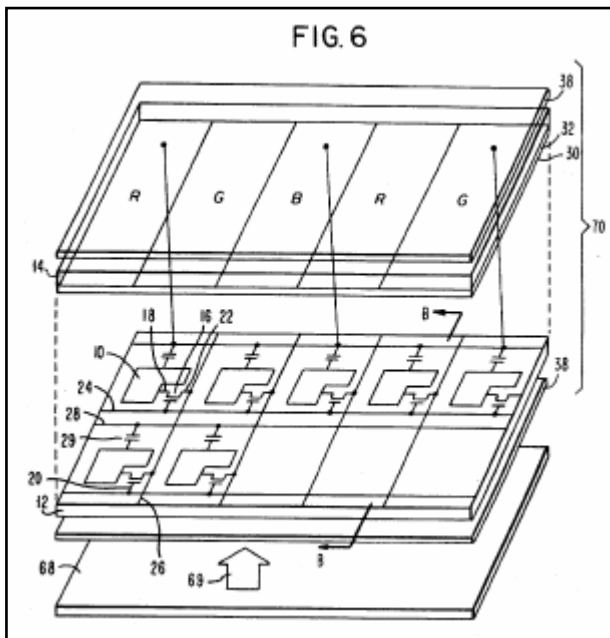
It is an object of the present invention to provide a TFT-LCD making it possible to prevent a signal delay from occurring even around the central portion of a common electrode and moreover prevent irregularity of a display screen and decrease of a contrast ration from occurring.

It is another object of the present invention to provide a TFT-LCD making it possible to keep a cell gap constant without using spacers.

It is still another object of the present invention to provide a TFT-LCD making it possible to supply a potential to a common electrode on a facing substrate without dotting a transfer.

4:51-64

**INTRINSIC EVIDENCE FOR DISPUTED TERM “COMMON ELECTRODE FOR ALL PIXELS COVERING AT LEAST SOME OF THE PILLARS” (cont’d):**



As shown in FIG. 8, the present invention uses a pillar 78 of a color filter 32 instead of a spacer in order to keep a cell gap between two substrates constant. Then, a signal delay of

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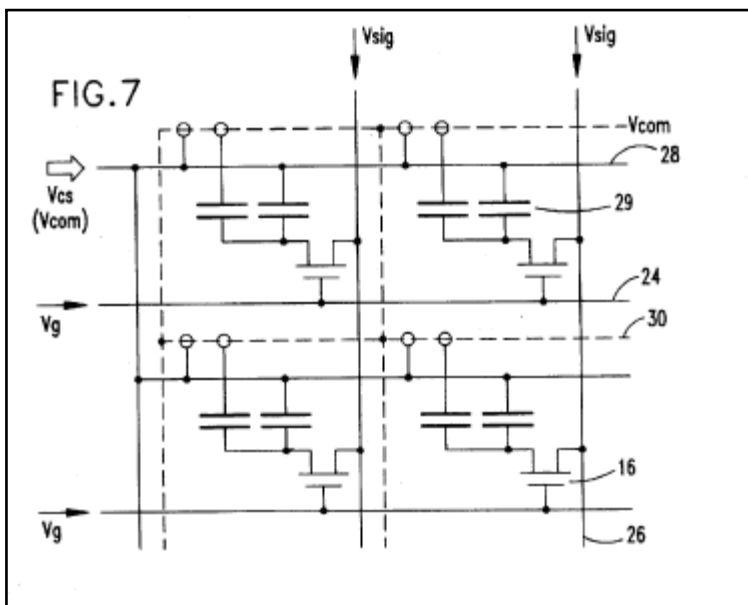
a common electrode 30 is prevented from occurring by forming a portion for electrically connecting a common electrode 30 covering the pillar 78 of the color filter 32 with a storage capacitance line 28 everywhere in a pixel area and supplying a potential of the common electrode 30 from the storage capacitance line 28.

4:65-5:6

According to the present invention, the potential of the storage capacitance line 28 is supplied to the common electrode 30 on a facing substrate from joints formed everywhere in a pixel area. Originally, the common-

5:7-10

**INTRINSIC EVIDENCE FOR DISPUTED TERM “COMMON ELECTRODE FOR ALL PIXELS COVERING AT LEAST SOME OF THE PILLARS” (cont’d):**



As shown in FIG. 8, the present invention uses a pillar 78 of a color filter 32 instead of a spacer in order to keep a cell gap between two substrates constant. Then, a signal delay of

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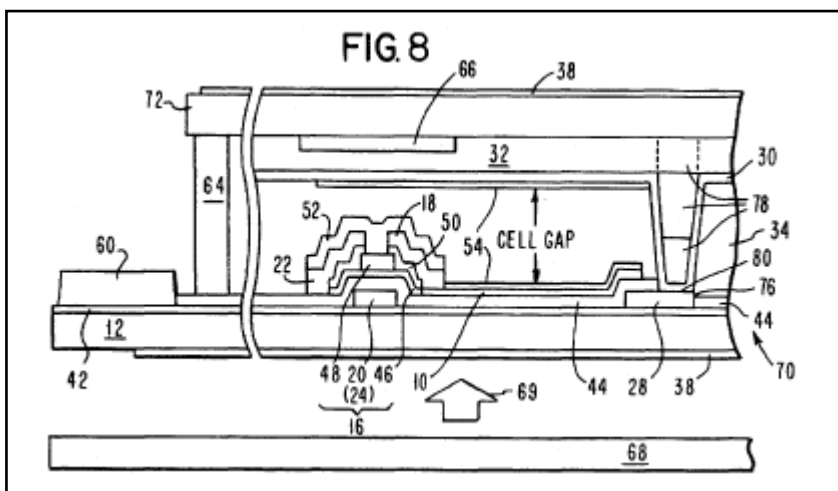
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4:65-5:6

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5:7-10

**INTRINSIC EVIDENCE FOR DISPUTED TERM “COMMON ELECTRODE FOR ALL PIXELS COVERING AT LEAST SOME OF THE PILLARS” (cont’d):**



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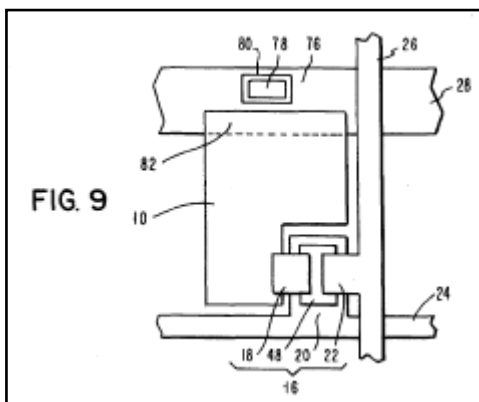
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4:65-5:6

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5:7-10

**INTRINSIC EVIDENCE FOR DISPUTED TERM “COMMON ELECTRODE FOR ALL PIXELS COVERING AT LEAST SOME OF THE PILLARS” (cont’d):**



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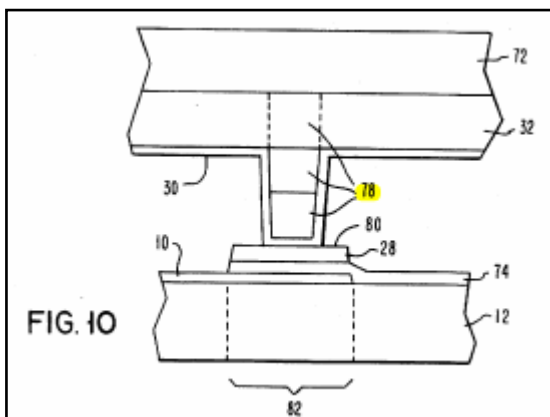
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4:65-5:6

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5:7-10

**INTRINSIC EVIDENCE FOR DISPUTED TERM “COMMON ELECTRODE FOR ALL PIXELS COVERING AT LEAST SOME OF THE PILLARS” (cont’d):**



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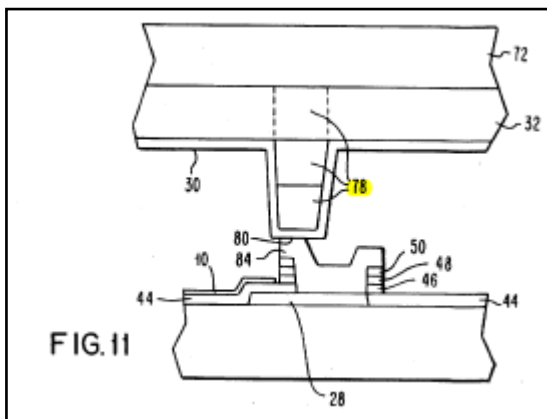
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4:65-5:6

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5:7-10

**INTRINSIC EVIDENCE FOR DISPUTED TERM “COMMON ELECTRODE FOR ALL PIXELS COVERING AT LEAST SOME OF THE PILLARS” (cont’d):**



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4:65-5:6

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5:7-10

**INTRINSIC EVIDENCE FOR DISPUTED TERM “COMMON ELECTRODE FOR ALL PIXELS COVERING AT LEAST SOME OF THE PILLARS” (cont’d):**

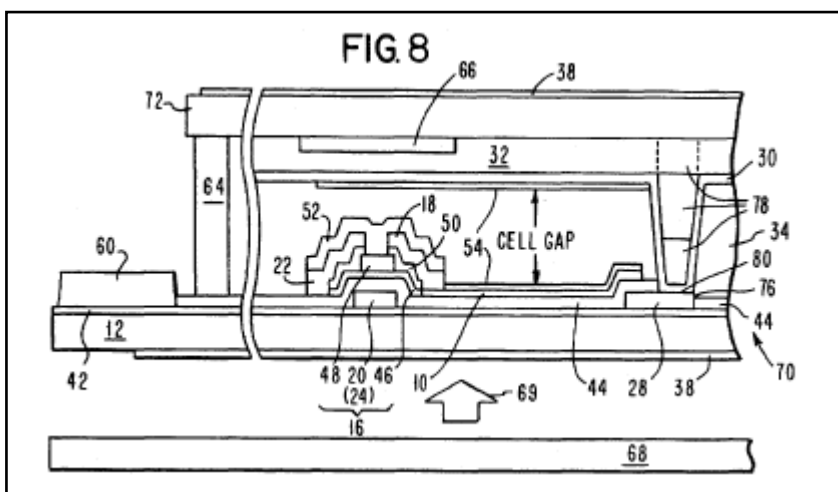
A pillar of a color filter on a facing substrate requires only change of mask patterns for the color filter but the number of processes does not increase. Moreover, it is possible to form a pillar by laminating red, green, and blue color filters or any two color filters of them. Furthermore, any sequence of colors to be laminated is not determined for a color-filter laminating portion. Furthermore, it is possible to fine-adjust a cell gap by forming a laminate structure containing a plurality of conductive materials at a position on an array substrate where a pillar is fitted on a facing substrate, connecting the laminate structure to a common electrode on

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the facing substrate through a conductive body layer electrically connected to a storage capacitance line, and specifying the cell gap by the sum of the height of the laminate structure on the array substrate and that of the pillar on the facing substrate.

5:57-6:5

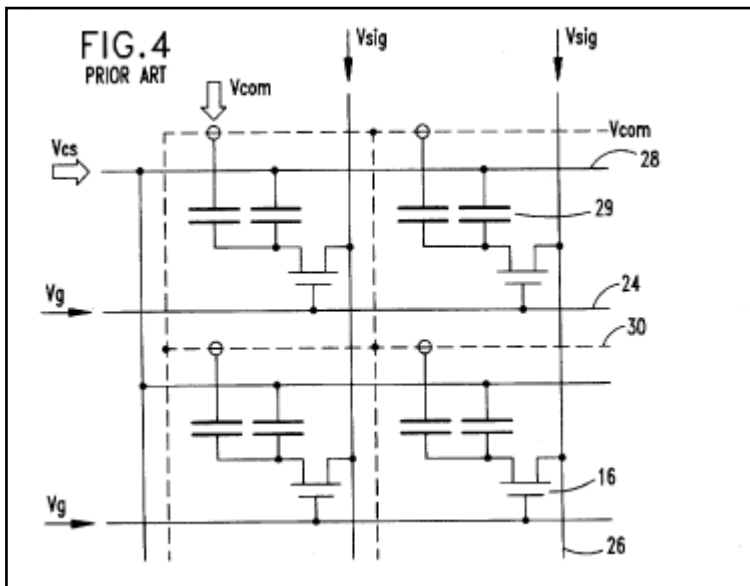
**INTRINSIC EVIDENCE FOR DISPUTED TERM “COMMON ELECTRODE FOR ALL PIXELS COVERING AT LEAST SOME OF THE PILLARS” (cont’d):**



Furthermore, as shown in FIG. 8, the embodiment 1 may have a structure in which the gate insulating film 44 is formed on the storage capacitance line 28 in a pixel area on the array substrate 12. That is, the embodiment 1 has a structure in which a hole 76 is formed at part of the gate insulating film 44 on the storage capacitance line 28, the common electrode 30 at a portion covering the pillar 78 of a color filter formed on the color filter substrate 72 is overlapped with the position of the hole 76, and the common electrode 30 contacts the storage capacitance line 28 so that they are electrically connected each other. Though the

7:4-13

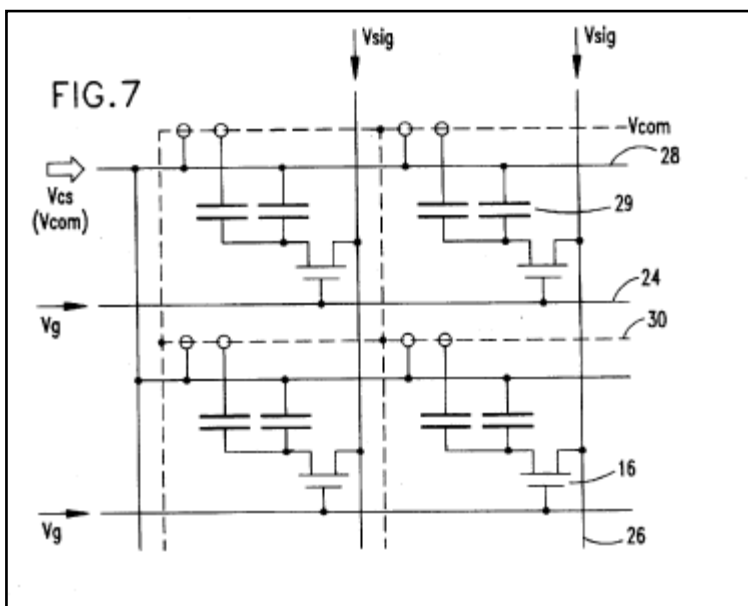
**INTRINSIC EVIDENCE FOR DISPUTED TERM “COMMON ELECTRODE FOR ALL PIXELS COVERING AT LEAST SOME OF THE PILLARS” (cont’d):**



Moreover, the present invention does not require a spherical spacer for specifying a cell gap or transfer for supplying a potential to the common electrode 30 as shown in FIG. 8. However, there is no problem in using the spacer and transfer. The equivalent circuit of the TFT-LCD of the present invention is shown in FIG. 7 for comparison with the circuit in FIG. 4. As shown in FIG. 7, the advantages are obtained that the problem of signal delay of Vcom is solved because Vcom is equal to Vcs everywhere in a screen by applying the present invention and it is unnecessary to independently supply Vcom from the outside.

7:32-42

**INTRINSIC EVIDENCE FOR DISPUTED TERM “COMMON ELECTRODE FOR ALL PIXELS COVERING AT LEAST SOME OF THE PILLARS” (cont’d):**



Moreover, the present invention does not require a spherical spacer for specifying a cell gap or transfer for supplying a potential to the common electrode 30 as shown in FIG. 8. However, there is no problem in using the spacer and transfer. The equivalent circuit of the TFT-LCD of the present invention is shown in FIG. 7 for comparison with the circuit in FIG. 4. As shown in FIG. 7, the advantages are obtained that the problem of signal delay of Vcom is solved because Vcom is equal to Vcs everywhere in a screen by applying the present invention and it is unnecessary to independently supply Vcom from the outside.

7:32-42

**INTRINSIC EVIDENCE FOR DISPUTED TERM “COMMON ELECTRODE FOR ALL PIXELS COVERING AT LEAST SOME OF THE PILLARS” (cont’d):**

As another method for connecting a common electrode with a storage capacitance line, the storage capacitance line 28 may be formed on the pixel electrode 10 formed on the array substrate 12 through the insulating film 74. In this case, a joint 80 between the storage capacitance line 28 and the common electrode 30 covering the pillar 78 of a color filter is three-dimensionally superimposed on a storage capacitance area 82.

In the case of the third embodiment, a layer 84 made of a conductive body such as a metal formed simultaneously with the data line 26 is first formed on the storage capacitance line 28, and then it is connected with the common electrode 30 to constitute the joint 80 instead of directly connecting the common electrode 30 to the storage capacitance line 28 like the first and second embodiments. Therefore, it is possible to perform fine adjustment for realizing an optically-optimized cell gap by the formation of the conductive body.

7:44-61

**INTRINSIC EVIDENCE FOR DISPUTED TERM “COMMON ELECTRODE FOR ALL PIXELS COVERING AT LEAST SOME OF THE PILLARS” (cont’d):**

Then, the process for manufacturing the liquid crystal display panel **70** of this embodiment is described below.

First, the process for manufacturing the array substrate **12** is described below.

In the first process, the undercoat layer **42** is formed on the array substrate **12**.

In the second process, the gate electrode **20**, gate line **24**, and storage capacitance line **28** are formed on the undercoat layer **42**.

In the third process, the gate insulating film **44** is formed.

In the fourth process, the semiconductor layer **46** of the TFT **16** is formed.

In the fifth process, the pixel electrode **10** is formed.

In the sixth process, the hole **76** is formed on part of the gate insulating film **44** on the storage capacitance line **28**.

In the seventh process, the source electrode **18** and drain electrode **22** of the TFT **16** and the data line **26** are formed.

In the eighth process, the passivation film **52** covering the TFT **16** is formed.

In the ninth process, the alignment film **54** is formed and treated through rubbing.

Then, the method for manufacturing the color filter substrate **72** is described below.

In the first process, the color filter **32** is formed on the facing substrate **14**, and the pillar **78** of a color filter is formed at a position corresponding to the hole **76** on the array substrate **12**.

In the second process, the common electrode **30** is formed on the color filter **32**.

In the third process, the alignment film **54** is formed and treated through rubbing.

The array substrate **12** and the color filter substrate **77** finished through the above processes are made to face each other and the storage capacitance line **28** viewed through the hole **76** on the array substrate **12** is overlapped with the common electrode **30** at the portion covering the pillar **78** of a color filter on the facing substrate **14** to electrically connect them each other.

Then, the liquid crystal display panel **70** is finished by sealing the perimeter of the assembly with a sealant **64**, injecting liquid crystal into the assembly through an injection hole (not illustrated), and closing the injection hole.

7:62-8:39

**INTRINSIC EVIDENCE FOR DISPUTED TERM “COMMON ELECTRODE FOR ALL PIXELS COVERING AT LEAST SOME OF THE PILLARS” (cont’d):**

The present invention provides a large high-definition liquid crystal display without causing a signal delay even around the central portion of a common electrode. Moreover, because the present invention disuses processes for scattering spacers and dotting transfers, the yield is improved and the cost is decreased.

8:39-45

**INTRINSIC EVIDENCE FOR DISPUTED TERM “COMMON ELECTRODE FOR ALL PIXELS COVERING AT LEAST SOME OF THE PILLARS” (cont’d):**

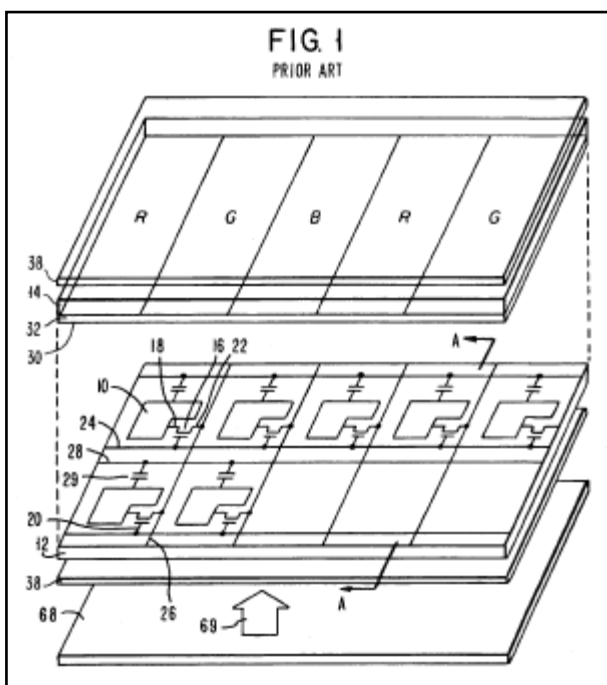
It is said to be unclear in Claims 1 and 5 which elements are “formed higher than other portions” and specify “a cell gap together with objects formed on the array substrate”. These elements are the pillars, which are now expressly identified. It is asked also which elements are electrically connected to the storage capacitance line. The answer is the portions of the common electrode covering at least some of the pillars. This has been clarified as well. The phrase “working on all pixels” is said to be not understood. This phrase merely refers to the fact that the common electrode is the common electrode for all of the pixels. This phrase has been deleted and the concept moved forward in Claims 1 and 5.

App. 08/615,012, 08/05/1997  
Amendment, pg. 6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE COMMON ELECTRODE BEING ELECTRICALLY CONNECTED TO THE STORAGE CAPACITANCE LINE AT THE PORTIONS OF THE COMMON ELECTRODE COVERING THE PILLARS”:**

To prevent a signal delay of an active-matrix liquid crystal display from occurring in an active-matrix liquid crystal display having an active element for each pixel electrode, a potential is supplied to a common electrode from a storage capacitance line by forming a pillar of a color filter to specify a cell gap between an array substrate having the storage capacitance line and a facing substrate having the color filter and electrically connecting the common electrode covering the pillar of the color filter with the storage capacitance line on the array substrate. Thereby, it is possible to disuse a transfer dotting process which is a factor of decreasing the yield and also a factor of decreasing the effective display area. Moreover, because the potential is supplied to the common electrode from the storage capacitance line, it is possible to prevent a signal delay of the common electrode from occurring and moreover realize a high-image-quality screen even in a large and high-definition liquid crystal display without causing irregularity of a display screen or decrease of a contrast ratio.

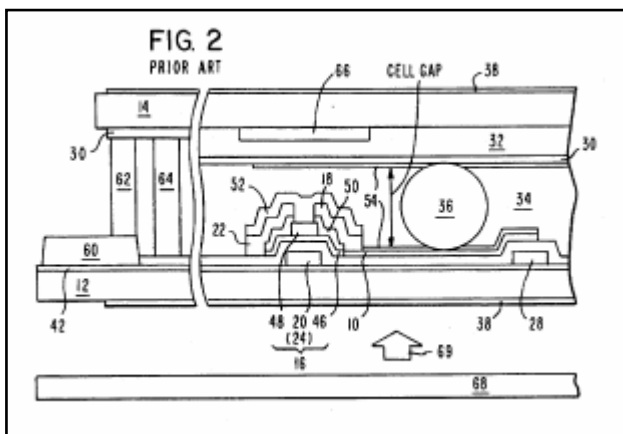
Abstract



perpendicular to each other. Moreover, each pixel electrode 10 has a necessary capacitance between the pixel electrode 10 and the storage capacitance line 28. This capacitance serves as a storage capacitance 29.

1:45

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE COMMON ELECTRODE BEING ELECTRICALLY CONNECTED TO THE STORAGE CAPACITANCE LINE AT THE PORTIONS OF THE COMMON ELECTRODE COVERING THE PILLARS” (cont’d):**



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1:45

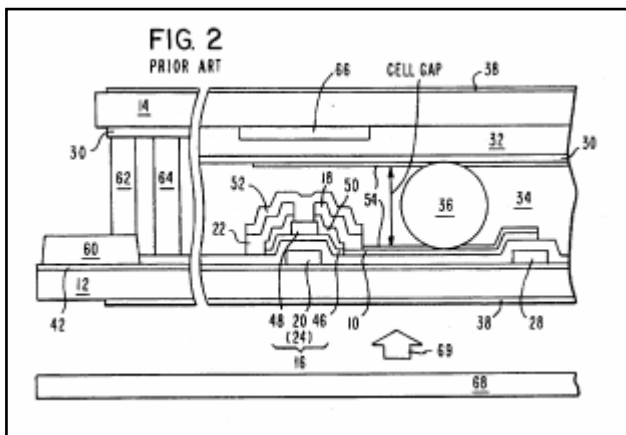
Among these layers and films, the undercoat layer 42, channel protective layer 48, passivation film 52, and alignment film 54 may not be deposited. A common electrode 30 is formed at the facing substrate 14 side of the TFT-LCD correspondingly to an area in which pixel electrodes 10 on the array substrate 12 are arranged like a matrix. Input signals are supplied to an OLB (Outer Lead Bonding) electrode 60 extended from a pixel area in which the pixel electrode 10 on the array substrate 12 is formed up to the perimeter of the area. Among the potentials of these signals, the potential of the common electrode 30 on the facing substrate is supplied from a plurality of portions of electrodes on the array substrate through a transfer 62 using

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conductive paste at the outside of the pixel area. The common electrode 30 is made of a transparent material such as ITO (Indium Tin Oxide) because it is necessary to pass light through the electrode 30. However, because the material has a large electric resistance, the electric resistance

1:57 - 2:4

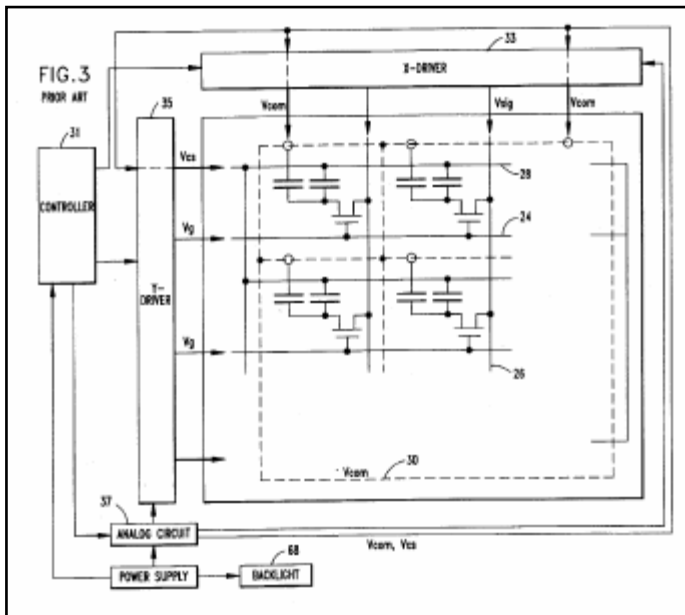
**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE COMMON ELECTRODE BEING ELECTRICALLY CONNECTED TO THE STORAGE CAPACITANCE LINE AT THE PORTIONS OF THE COMMON ELECTRODE COVERING THE PILLARS” (cont’d):**



Furthermore, a black matrix 66 is formed like a lattice. In the case of an existing liquid crystal display, transparent spherical spacers 36 are scattered in a liquid crystal layer 34 held by the array substrate 12 and the facing substrate 14 in order to keep a predetermined interval between the two substrates 12 and 14. Moreover, liquid crystal is sealed between the two substrates by a sealant 64. Furthermore, a polarizing

2:13-19

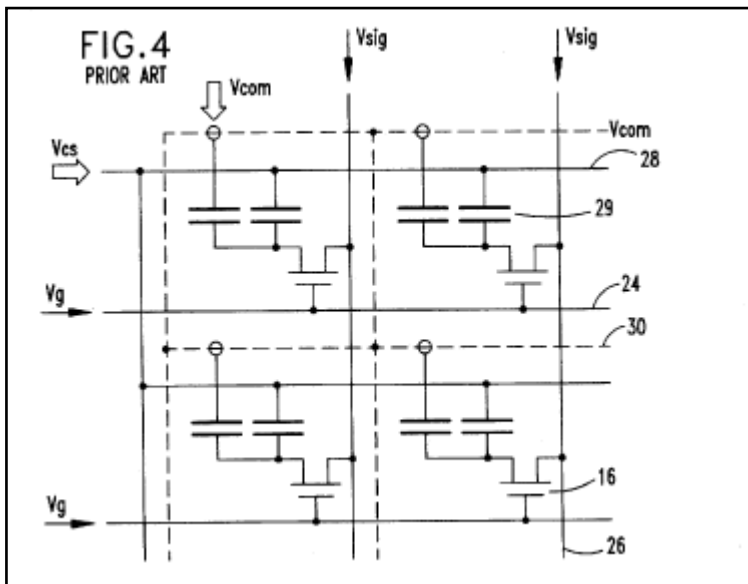
**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE COMMON ELECTRODE BEING ELECTRICALLY CONNECTED TO THE STORAGE CAPACITANCE LINE AT THE PORTIONS OF THE COMMON ELECTRODE COVERING THE PILLARS” (cont’d):**



FIGS. 3 and 4 show an equivalent circuit of an existing TFT-LCD. An input signal supplied to the existing TFT-LCD is described below by referring to FIGS. 3 and 4. A controller 31 converts image data into a form to be supplied to an X-driver 33 and a Y-driver 35 of a driver IC. Moreover, an analog circuit 37 generates a voltage for each input signal. Input signals to be supplied to the TFT-LCD include a scanning signal ( $V_g$ ) of a gate line 24 supplied from the Y-driver 35, a display signal ( $V_{sig}$ ) of a data line 26 supplied from the X-driver 33, a common-electrode potential ( $V_{com}$ ) of a common electrode 30, and a storage capacitance line potential ( $V_{cs}$ ) of a storage capacitance line 28. The potentials of these input signals are all supplied to the OLB electrode 60 extended from the pixel area in which the pixel electrodes 10 on the array substrate 12 are formed up to the perimeter of the area as shown in FIG. 2. Then, among the potentials of these input signals, the potential  $V_{com}$  is supplied to the common electrode 30 through the transfer 62.

2:25-42

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE COMMON ELECTRODE BEING ELECTRICALLY CONNECTED TO THE STORAGE CAPACITANCE LINE AT THE PORTIONS OF THE COMMON ELECTRODE COVERING THE PILLARS” (cont’d):**



FIGS. 3 and 4 show an equivalent circuit of an existing TFT-LCD. An input signal supplied to the existing TFT-LCD is described below by referring to FIGS. 3 and 4. A controller 31 converts image data into a form to be supplied to an X-driver 33 and a Y-driver 35 of a driver IC. Moreover, an analog circuit 37 generates a voltage for each input signal. Input signals to be supplied to the TFT-LCD include a scanning signal ( $V_g$ ) of a gate line 24 supplied from the Y-driver 35, a display signal ( $V_{sig}$ ) of a data line 26 supplied from the X-driver 33, a common-electrode potential ( $V_{com}$ ) of a common electrode 30, and a storage capacitance line potential ( $V_{cs}$ ) of a storage capacitance line 28. The potentials of these input signals are all supplied to the OLB electrode 60 extended from the pixel area in which the pixel electrodes 10 on the array substrate 12 are formed up to the perimeter of the area as shown in FIG. 2. Then, among the potentials of these input signals, the potential  $V_{com}$  is supplied to the common electrode 30 through the transfer 62.

2:25-42

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE COMMON ELECTRODE BEING ELECTRICALLY CONNECTED TO THE STORAGE CAPACITANCE LINE AT THE PORTIONS OF THE COMMON ELECTRODE COVERING THE PILLARS” (cont’d):**

A driving method in which a polarity is inverted because the potential of a common electrode at the facing substrate side synchronizes with the display signal  $V_{sig}$  is referred to as common-voltage AC inversion driving ( $V_{com}$  inversion) which is distinguished from a method in which common voltage is constant. The  $V_{com}$  inversion driving has an advantage that the maximum voltage amplitude of the

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display signal  $V_{sig}$  can be decreased because the voltage amplitude of the common electrode biased to the voltage amplitude of the display signal  $V_{sig}$  is applied to a liquid crystal layer. It is requested from the market of the TFT-LCD

2:61 - 3:4

Moreover, as shown in FIG. 2, the existing TFT-LCD has a problem in the structure of supplying the potential of the common electrode 30 on the facing substrate 14 from a plurality of portions at the perimeter of a pixel area of the array substrate 12 side to the common electrode 30 on the facing substrate 14 through the transfer 62 using conductive paste. Because this structure requires a high-accuracy alignment of the transfer 62, it uses two or more transfers to prevent defectives from being produced due to a deviation of a transfer. However, the manufacturing yield is decreased due to defectives produced in a process for dotting a transfer. Moreover, there is the restriction on design that an area for dotting a transfer must be formed at the perimeter of a pixel area. That is, because an area independent of display must exclusively be formed on the array substrate 12 and the facing substrate 14, an effective display area to a substrate size is decreased. However, it is inevitable to use the above structure because it is indispensable for an existing liquid crystal display in view of design.

4:31-49

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE COMMON ELECTRODE BEING ELECTRICALLY CONNECTED TO THE STORAGE CAPACITANCE LINE AT THE PORTIONS OF THE COMMON ELECTRODE COVERING THE PILLARS” (cont’d):**

**SUMMARY OF THE INVENTION**

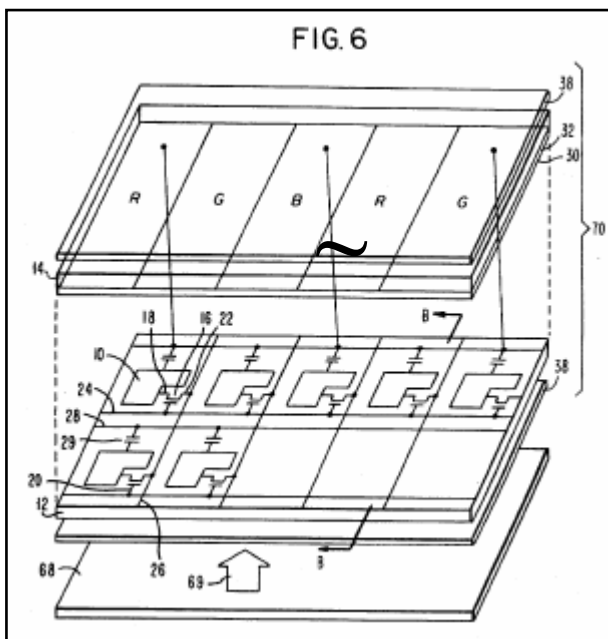
It is an object of the present invention to provide a TFT-LCD making it possible to prevent a signal delay from occurring even around the central portion of a common electrode and moreover prevent irregularity of a display screen and decrease of a contrast ration from occurring.

It is another object of the present invention to provide a TFT-LCD making it possible to keep a cell gap constant without using spacers.

It is still another object of the present invention to provide a TFT-LCD making it possible to supply a potential to a common electrode on a facing substrate without dotting a transfer.

4:51-64

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE COMMON ELECTRODE BEING ELECTRICALLY CONNECTED TO THE STORAGE CAPACITANCE LINE AT THE PORTIONS OF THE COMMON ELECTRODE COVERING THE PILLARS” (cont’d):**



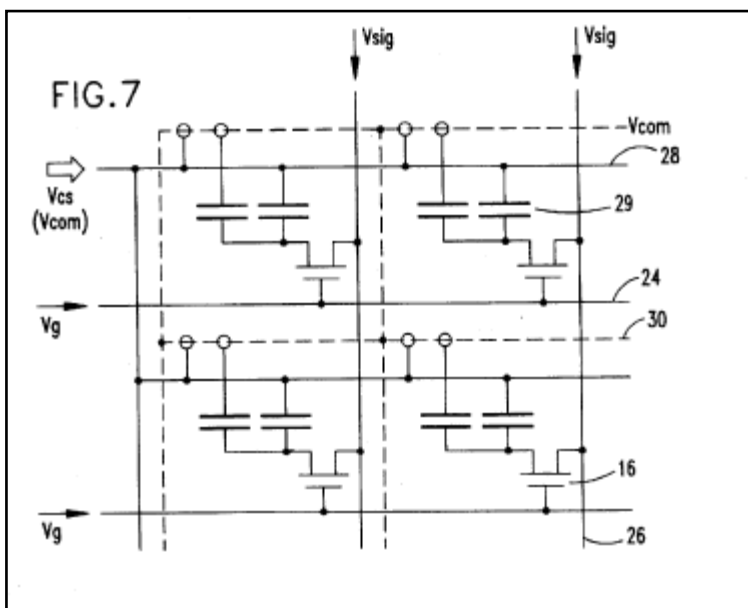
As shown in FIG. 8, the present invention uses a pillar 78 of a color filter 32 instead of a spacer in order to keep a cell gap between two substrates constant. Then, a signal delay of

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a common electrode 30 is prevented from occurring by forming a portion for electrically connecting a common electrode 30 covering the pillar 78 of the color filter 32 with a storage capacitance line 28 everywhere in a pixel area and supplying a potential of the common electrode 30 from the storage capacitance line 28.

4:65-5:6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE COMMON ELECTRODE BEING ELECTRICALLY CONNECTED TO THE STORAGE CAPACITANCE LINE AT THE PORTIONS OF THE COMMON ELECTRODE COVERING THE PILLARS” (cont’d):**



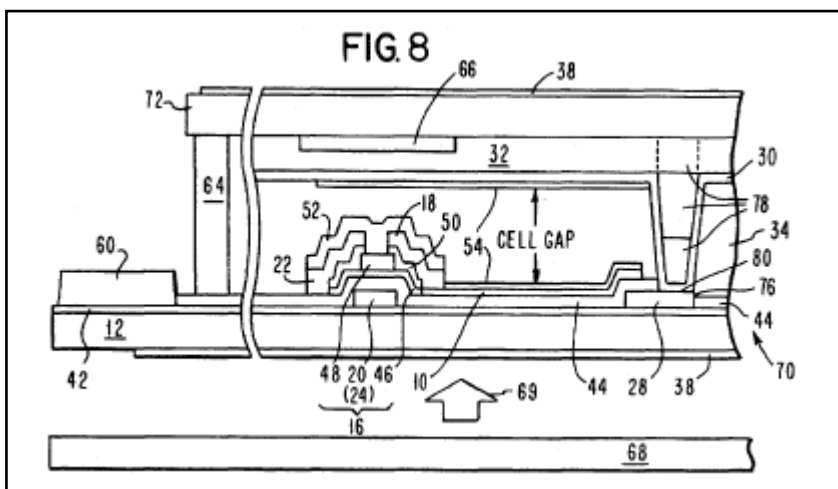
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4:65-5:6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE COMMON ELECTRODE BEING ELECTRICALLY CONNECTED TO THE STORAGE CAPACITANCE LINE AT THE PORTIONS OF THE COMMON ELECTRODE COVERING THE PILLARS” (cont’d):**



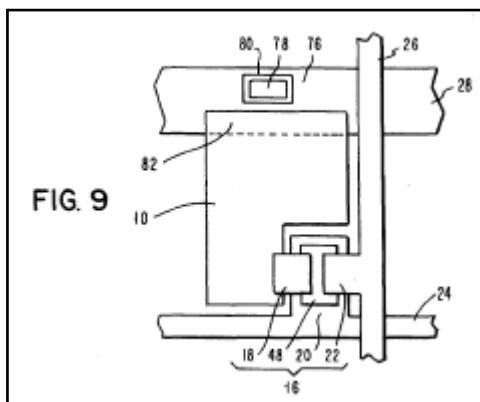
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4:65-5:6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE COMMON ELECTRODE BEING ELECTRICALLY CONNECTED TO THE STORAGE CAPACITANCE LINE AT THE PORTIONS OF THE COMMON ELECTRODE COVERING THE PILLARS” (cont’d):**



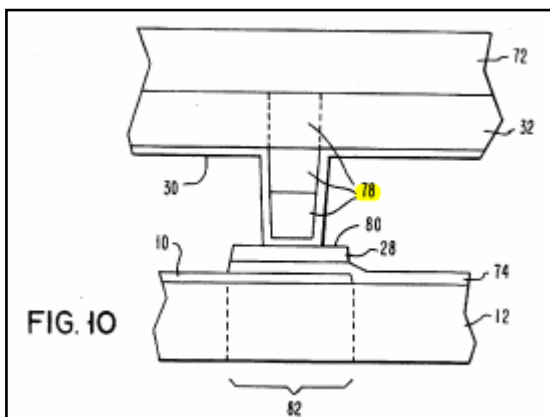
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4:65-5:6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE COMMON ELECTRODE BEING ELECTRICALLY CONNECTED TO THE STORAGE CAPACITANCE LINE AT THE PORTIONS OF THE COMMON ELECTRODE COVERING THE PILLARS” (cont’d):**



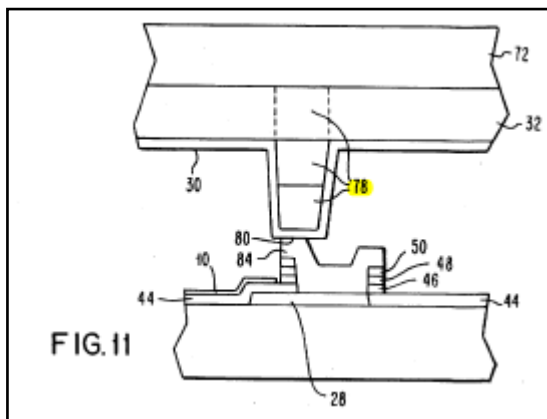
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4:65-5:6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE COMMON ELECTRODE BEING ELECTRICALLY CONNECTED TO THE STORAGE CAPACITANCE LINE AT THE PORTIONS OF THE COMMON ELECTRODE COVERING THE PILLARS” (cont’d):**



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4:65-5:6

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5:7-10

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE COMMON ELECTRODE BEING ELECTRICALLY CONNECTED TO THE STORAGE CAPACITANCE LINE AT THE PORTIONS OF THE COMMON ELECTRODE COVERING THE PILLARS” (cont’d):**

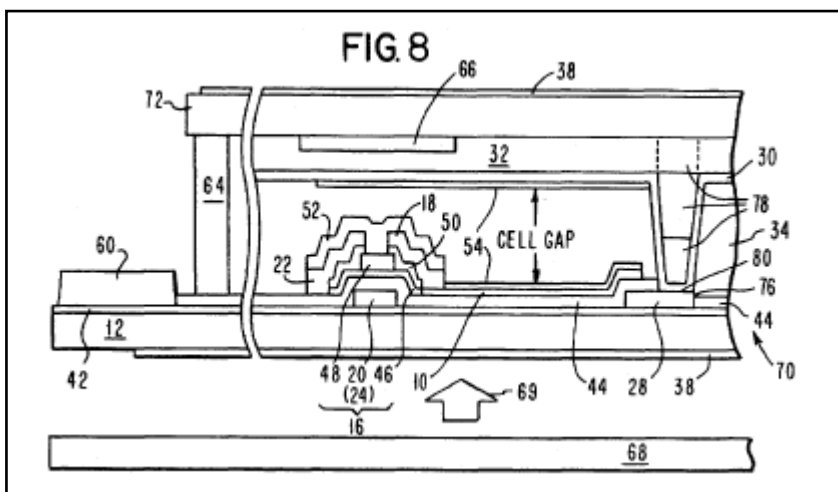
A pillar of a color filter on a facing substrate requires only change of mask patterns for the color filter but the number of processes does not increase. Moreover, it is possible to form a pillar by laminating red, green, and blue color filters or any two color filters of them. Furthermore, any sequence of colors to be laminated is not determined for a color-filter laminating portion. Furthermore, it is possible to fine-adjust a cell gap by forming a laminate structure containing a plurality of conductive materials at a position on an array substrate where a pillar is fitted on a facing substrate, connecting the laminate structure to a common electrode on

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the facing substrate through a conductive body layer electrically connected to a storage capacitance line, and specifying the cell gap by the sum of the height of the laminate structure on the array substrate and that of the pillar on the facing substrate.

5:57-6:5

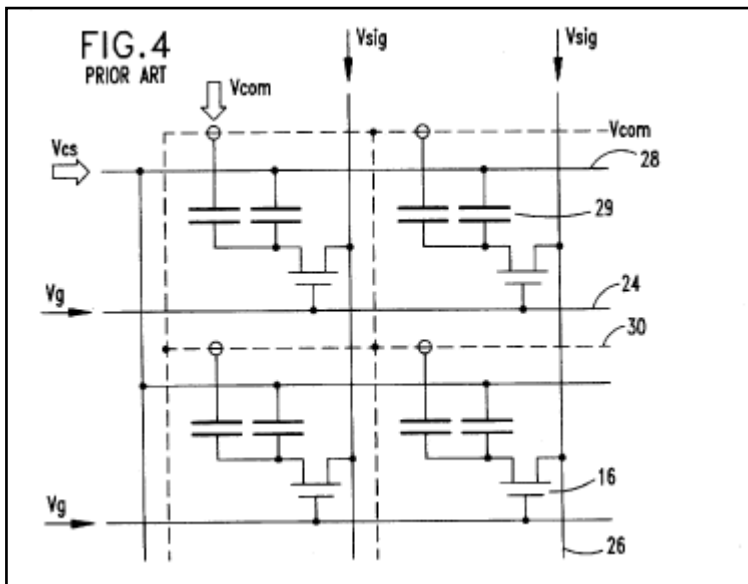
**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE COMMON ELECTRODE BEING ELECTRICALLY CONNECTED TO THE STORAGE CAPACITANCE LINE AT THE PORTIONS OF THE COMMON ELECTRODE COVERING THE PILLARS” (cont’d):**



Furthermore, as shown in FIG. 8, the embodiment 1 may have a structure in which the gate insulating film 44 is formed on the storage capacitance line 28 in a pixel area on the array substrate 12. That is, the embodiment 1 has a structure in which a hole 76 is formed at part of the gate insulating film 44 on the storage capacitance line 28, the common electrode 30 at a portion covering the pillar 78 of a color filter formed on the color filter substrate 72 is overlapped with the position of the hole 76, and the common electrode 30 contacts the storage capacitance line 28 so that they are electrically connected each other. Though the

7:4-13

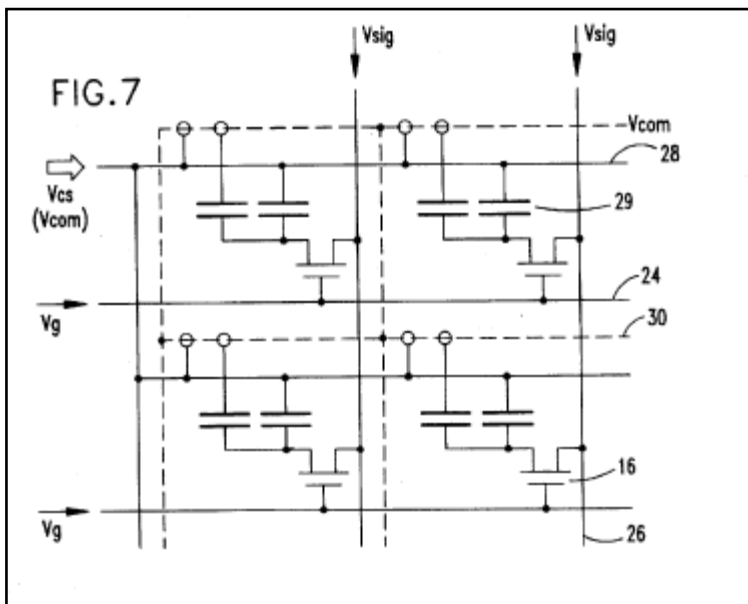
**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE COMMON ELECTRODE BEING ELECTRICALLY CONNECTED TO THE STORAGE CAPACITANCE LINE AT THE PORTIONS OF THE COMMON ELECTRODE COVERING THE PILLARS” (cont’d):**



Moreover, the present invention does not require a spherical spacer for specifying a cell gap or transfer for supplying a potential to the common electrode 30 as shown in FIG. 8. However, there is no problem in using the spacer and transfer. The equivalent circuit of the TFT-LCD of the present invention is shown in FIG. 7 for comparison with the circuit in FIG. 4. As shown in FIG. 7, the advantages are obtained that the problem of signal delay of Vcom is solved because Vcom is equal to Vcs everywhere in a screen by applying the present invention and it is unnecessary to independently supply Vcom from the outside.

7:32-42

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE COMMON ELECTRODE BEING ELECTRICALLY CONNECTED TO THE STORAGE CAPACITANCE LINE AT THE PORTIONS OF THE COMMON ELECTRODE COVERING THE PILLARS” (cont’d):**



Moreover, the present invention does not require a spherical spacer for specifying a cell gap or transfer for supplying a potential to the common electrode 30 as shown in FIG. 8. However, there is no problem in using the spacer and transfer. The equivalent circuit of the TFT-LCD of the present invention is shown in FIG. 7 for comparison with the circuit in FIG. 4. As shown in FIG. 7, the advantages are obtained that the problem of signal delay of Vcom is solved because Vcom is equal to Vcs everywhere in a screen by applying the present invention and it is unnecessary to independently supply Vcom from the outside.

7:32-42

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE COMMON ELECTRODE BEING ELECTRICALLY CONNECTED TO THE STORAGE CAPACITANCE LINE AT THE PORTIONS OF THE COMMON ELECTRODE COVERING THE PILLARS” (cont’d):**

As another method for connecting a common electrode with a storage capacitance line, the storage capacitance line 28 may be formed on the pixel electrode 10 formed on the array substrate 12 through the insulating film 74. In this case, a joint 80 between the storage capacitance line 28 and the common electrode 30 covering the pillar 78 of a color filter is three-dimensionally superimposed on a storage capacitance area 82.

In the case of the third embodiment, a layer 84 made of a conductive body such as a metal formed simultaneously with the data line 26 is first formed on the storage capacitance line 28, and then it is connected with the common electrode 30 to constitute the joint 80 instead of directly connecting the common electrode 30 to the storage capacitance line 28 like the first and second embodiments. Therefore, it is possible to perform fine adjustment for realizing an optically-optimized cell gap by the formation of the conductive body.

7:44-61

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE COMMON ELECTRODE BEING ELECTRICALLY CONNECTED TO THE STORAGE CAPACITANCE LINE AT THE PORTIONS OF THE COMMON ELECTRODE COVERING THE PILLARS” (cont’d):**

Then, the process for manufacturing the liquid crystal display panel **70** of this embodiment is described below.

First, the process for manufacturing the array substrate **12** is described below.

In the first process, the undercoat layer **42** is formed on the array substrate **12**.

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In the second process, the gate electrode **20**, gate line **24**, and storage capacitance line **28** are formed on the undercoat layer **42**.

In the third process, the gate insulating film **44** is formed.

In the fourth process, the semiconductor layer **46** of the TFT **16** is formed.

In the fifth process, the pixel electrode **10** is formed.

In the sixth process, the hole **76** is formed on part of the gate insulating film **44** on the storage capacitance line **28**.

In the seventh process, the source electrode **18** and drain electrode **22** of the TFT **16** and the data line **26** are formed.

In the eighth process, the passivation film **52** covering the TFT **16** is formed.

In the ninth process, the alignment film **54** is formed and treated through rubbing.

Then, the method for manufacturing the color filter substrate **72** is described below.

In the first process, the color filter **32** is formed on the facing substrate **14**, and the pillar **78** of a color filter is formed at a position corresponding to the hole **76** on the array substrate **12**.

In the second process, the common electrode **30** is formed on the color filter **32**.

In the third process, the alignment film **54** is formed and treated through rubbing.

The array substrate **12** and the color filter substrate **77** finished through the above processes are made to face each other and the storage capacitance line **28** viewed through the hole **76** on the array substrate **12** is overlapped with the common electrode **30** at the portion covering the pillar **78** of a color filter on the facing substrate **14** to electrically connect them each other.

Then, the liquid crystal display panel **70** is finished by sealing the perimeter of the assembly with a sealant **64**, injecting liquid crystal into the assembly through an injection hole (not illustrated), and closing the injection hole.

7:62-8:39

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE COMMON ELECTRODE BEING ELECTRICALLY CONNECTED TO THE STORAGE CAPACITANCE LINE AT THE PORTIONS OF THE COMMON ELECTRODE COVERING THE PILLARS” (cont’d):**

The present invention provides a large high-definition liquid crystal display without causing a signal delay even around the central portion of a common electrode. Moreover, because the present invention disuses processes for scattering spacers and dotting transfers, the yield is improved and the cost is decreased.

8:39-45

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE COMMON ELECTRODE BEING ELECTRICALLY CONNECTED TO THE STORAGE CAPACITANCE LINE AT THE PORTIONS OF THE COMMON ELECTRODE COVERING THE PILLARS” (cont’d):**

It is said to be unclear in Claims 1 and 5 which elements are “formed higher than other portions” and specify “a cell gap together with objects formed on the array substrate”. These elements are the pillars, which are now expressly identified. It is asked also which elements are electrically connected to the storage capacitance line. The answer is the portions of the common electrode covering at least some of the pillars. This has been clarified as well. The phrase “working on all pixels” is said to be not understood. This phrase merely refers to the fact that the common electrode is the common electrode for all of the pixels. This phrase has been deleted and the concept moved forward in Claims 1 and 5.

App. 08/615,012, 08/05/1997  
Amendment, pg. 6

**EXHIBIT \_\_\_\_\_**  
**U.S. PATENT NO. 5,748,266**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 1**

1. A color filter and common electrode carried by a facing substrate for assembly with an array substrate to form a liquid crystal display panel, the color filter comprising a plurality of pillars formed higher than other portions of the color filter for contact with objects formed on the array substrate to specify a cell gap, wherein the pillars are covered with the common electrode.

**ASSERTED CLAIM 3**

3. A liquid crystal display panel comprising:  
 an array substrate having pixel electrodes arranged like a matrix, an active element for each of the pixel electrodes, a storage capacitance provided at some of the pixel electrodes, and a storage capacitance line for outputting the reference potential of the storage capacitance;  
 a facing substrate having a plurality of pillars arranged so as to face the array substrate, the pillars being formed higher than other portions of the facing substrate, the pillars together with objects formed on the array substrate that face the pillars specifying a cell gap, and a common electrode for all pixels covering at least some of the pillars, the common electrode being electrically connected to the storage capacitance line at the portions of the common electrode covering the pillars; and  
 a liquid crystal layer held between the array substrate and the facing substrate.

**LGD's Claim Construction**

**pillars formed higher than other portions of the color filter** - patterned structures of the color filter that protrude toward the pixel array beyond the height of non-pillar portions of the color filter substrate to act as a spacer

**the pillars are covered with the common electrode** - the common electrode is formed to cover the protruded surface of the pillars

**storage capacitance line<sup>1</sup>** - a pattern of electrically conductive material within the pixel area for providing a reference voltage to the storage capacitors

**storage capacitance line for outputting the reference potential of the storage capacitance<sup>3</sup>** - a pattern of electrically conductive material within the pixel area for providing a reference voltage to the storage capacitors

<sup>1</sup> Disputed Term "storage capacitance line" also appears in asserted claims 6, 7, and 9 in the same context.

<sup>3</sup> Disputed Term "storage capacitance line" also appears in asserted claim 7 in the same context.

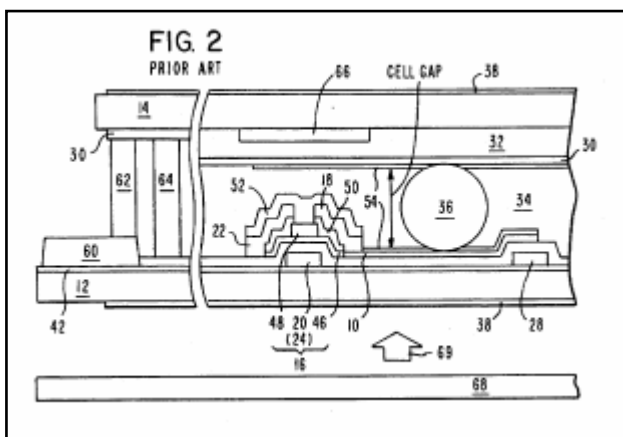
**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”:**

To prevent a signal delay of an active-matrix liquid crystal display from occurring in an active-matrix liquid crystal display having an active element for each pixel electrode, a potential is supplied to a common electrode from a storage capacitance line by forming a pillar of a color filter to specify a cell gap between an array substrate having the storage capacitance line and a facing substrate having the color filter and electrically connecting the common electrode covering the pillar of the color filter with the storage capacitance line on the array substrate. Thereby, it is possible to disuse a transfer dotting process which is a factor of decreasing the yield and also a factor of decreasing the effective display area. Moreover, because the potential is supplied to the common electrode from the storage capacitance line, it is possible to prevent a signal delay of the common electrode from occurring and moreover realize a high-image-quality screen even in a large and high-definition liquid crystal display without causing irregularity of a display screen or decrease of a contrast ratio.

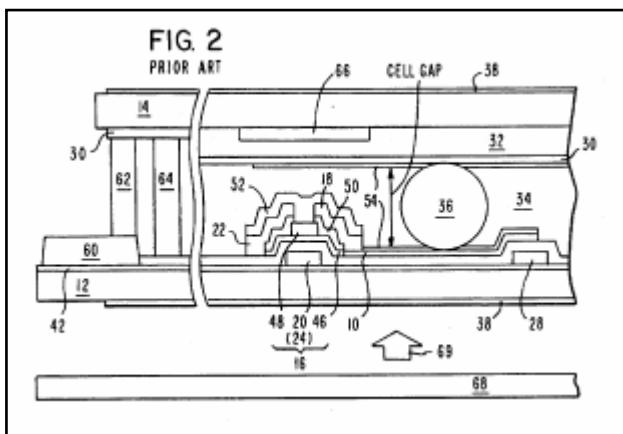
Abstract

Furthermore, because it is possible to disuse a spacer scattering process and specify a cell gap by securing the pillar of the color filter, not only the cell gap is kept constant at any place and the uniformity of the screen is maintained but also spacers do not brighten or the screen is not blackened due to coagulation of the spacers and the image quality is improved. Furthermore, the cost can be decreased because the transfer dotting process and the spacer scattering process are unnecessary.

Abstract



**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**  
**(cont’d):**



Furthermore, a black matrix 66 is formed like a lattice. In the case of an existing liquid crystal display, transparent spherical spacers 36 are scattered in a liquid crystal layer 34 held by the array substrate 12 and the facing substrate 14 in order to keep a predetermined interval between the two substrates 12 and 14. Moreover, liquid crystal is sealed between the two substrates by a sealant 64. Furthermore, a polarizing

2:13-19

**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**

**(cont'd):**

Moreover, as shown in FIG. 2, the transparent spherical spacers 36 (made of plastic and glass fiber) are hitherto

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scattered in the liquid crystal layer 34 held by the array substrate 12 and the facing substrate 14 constituting a liquid crystal display in order to keep the substrates 12 and 14 at a predetermined interval. However, under the spacers kept scattered, liquid crystal flows in a panel when an external force is applied to the panel, the spacers are moved in a cell plane due to the flowing of the liquid crystal, and thereby the spacers may scratch the surface of the thin alignment film 54 due to the movement of the spacers. Moreover, a cell gap (interval between electrodes of two substrates) may not be kept constant due to coagulation of the spacers. Unless the cell gap is kept constant, the optical path length difference (product of the birefringence rate and cell gap of the liquid crystal) of the liquid crystal layer changes and thereby, the contrast ratio and the chromaticity of a display screen are changed. Thus, problems occur that the uniformity of the screen cannot be kept or the display quality is deteriorated. Moreover, the spacers are brightened or coagulated, and the light from the backlight 68 is cut off by the coagulated spacers and thereby the screen is blackened by the degree of cut-off light. To solve these problems, various structures are

3:66 – 4:21

Moreover, the spacers are brightened or coagulated, and the light from the backlight 68 is cut off by the coagulated spacers and thereby the screen is blackened by the degree of cut-off light. To solve these problems, various structures are already disclosed which disuse transparent spherical spacers and instead, specify a cell gap by a pillar formed on the array substrate 12 and/or the facing substrate 14 (official gazettes of Japanese Patent Laid-Open Nos. 164723/1985, 105583/1986, 24230/1989, 134733/1986, 163428/1902, 250416/1987, and 196946/1993). However, any one of these disclosures does not show means for solving the problem of signal delay in a TFT-LCD using the H/com inversion driving method.

4:21-30

**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**  
**(cont’d):**

Moreover, as shown in FIG. 2, the existing TFT-LCD has a problem in the structure of supplying the potential of the common electrode 30 on the facing substrate 14 from a plurality of portions at the perimeter of a pixel area of the array substrate 12 side to the common electrode 30 on the facing substrate 14 through the transfer 62 using conductive paste. Because this structure requires a high-accuracy alignment of the transfer 62, it uses two or more transfers to prevent defectives from being produced due to a deviation of a transfer. However, the manufacturing yield is decreased due to defectives produced in a process for dotting a transfer. Moreover, there is the restriction on design that an area for dotting a transfer must be formed at the perimeter of a pixel area. That is, because an area independent of display must exclusively be formed on the array substrate 12 and the facing substrate 14, an effective display area to a substrate size is decreased. However, it is inevitable to use the above structure because it is indispensable for an existing liquid crystal display in view of design.

4:31-49

**SUMMARY OF THE INVENTION**

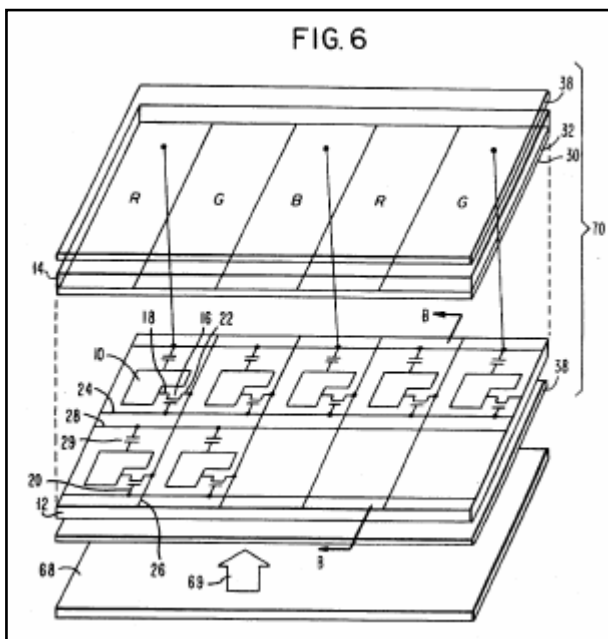
It is an object of the present invention to provide a TFT-LCD making it possible to prevent a signal delay from occurring even around the central portion of a common electrode and moreover prevent irregularity of a display screen and decrease of a contrast ration from occurring.

It is another object of the present invention to provide a TFT-LCD making it possible to keep a cell gap constant without using spacers.

It is still another object of the present invention to provide a TFT-LCD making it possible to supply a potential to a common electrode on a facing substrate without dotting a transfer.

4:51-64

**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**  
**(cont’d):**



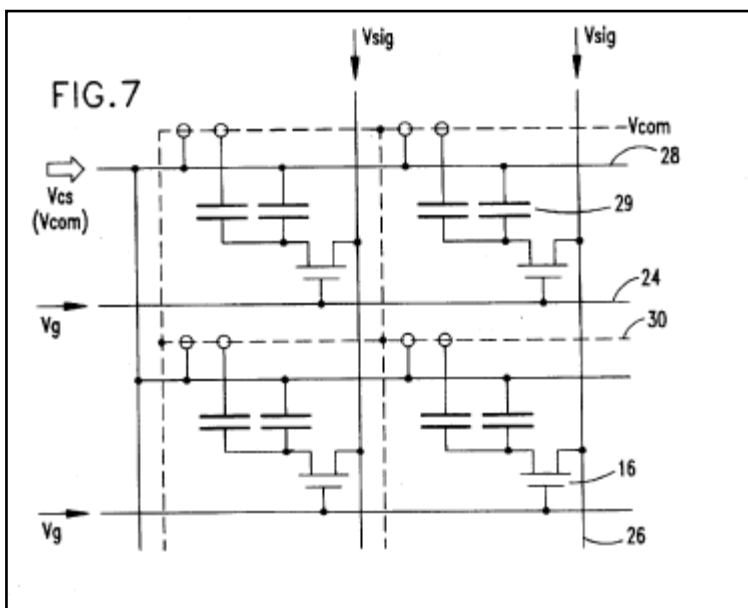
As shown in FIG. 8, the present invention uses a pillar 78 of a color filter 32 instead of a spacer in order to keep a cell gap between two substrates constant. Then, a signal delay of

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a common electrode 30 is prevented from occurring by forming a portion for electrically connecting a common electrode 30 covering the pillar 78 of the color filter 32 with a storage capacitance line 28 everywhere in a pixel area and supplying a potential of the common electrode 30 from the storage capacitance line 28.

4:65-5:6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**  
**(cont’d):**



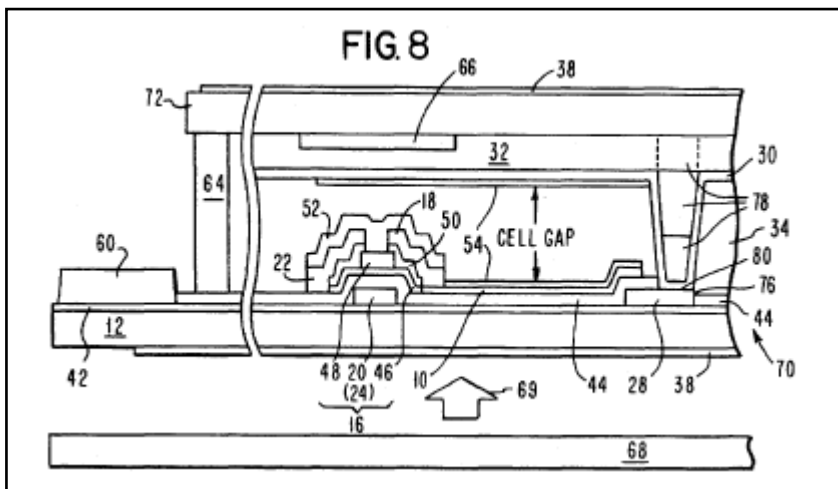
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4:65-5:6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**  
**(cont’d):**



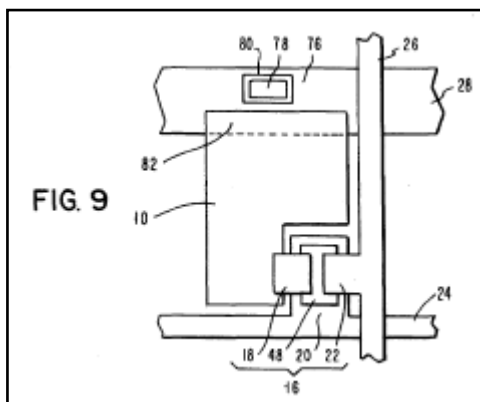
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4:65-5:6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED  
HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**  
**(cont’d):**



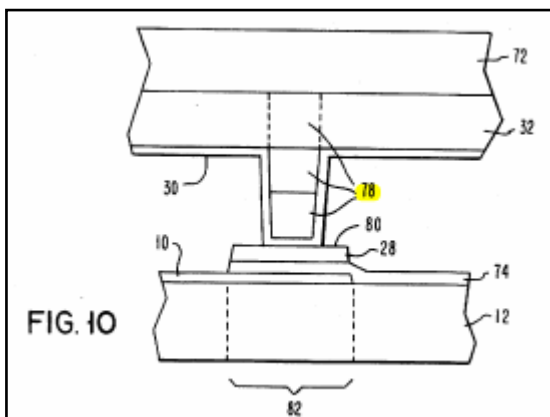
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4:65-5:6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**  
**(cont’d):**



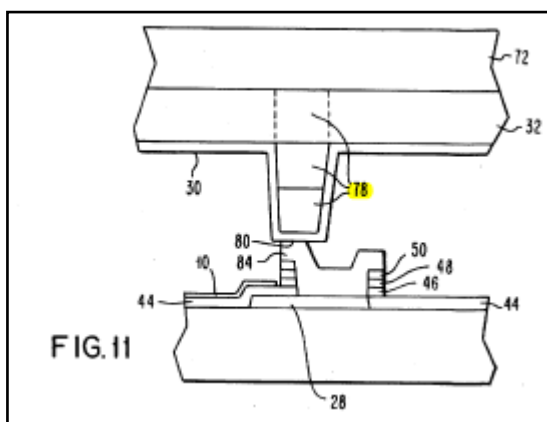
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4:65-5:6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**  
**(cont’d):**



As shown in FIG. 8, the present invention uses a pillar 78 of a color filter 32 instead of a spacer in order to keep a cell gap between two substrates constant. Then, a signal delay of

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a common electrode 30 is prevented from occurring by forming a portion for electrically connecting a common electrode 30 covering the pillar 78 of the color filter 32 with a storage capacitance line 28 everywhere in a pixel area and supplying a potential of the common electrode 30 from the storage capacitance line 28.

4:65-5:6

According to the present invention, the potential of the storage capacitance line 28 is supplied to the common electrode 30 on a facing substrate from joints formed everywhere in a pixel area. Originally, the common-

5:7-10

**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED  
HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”  
(cont’d):**

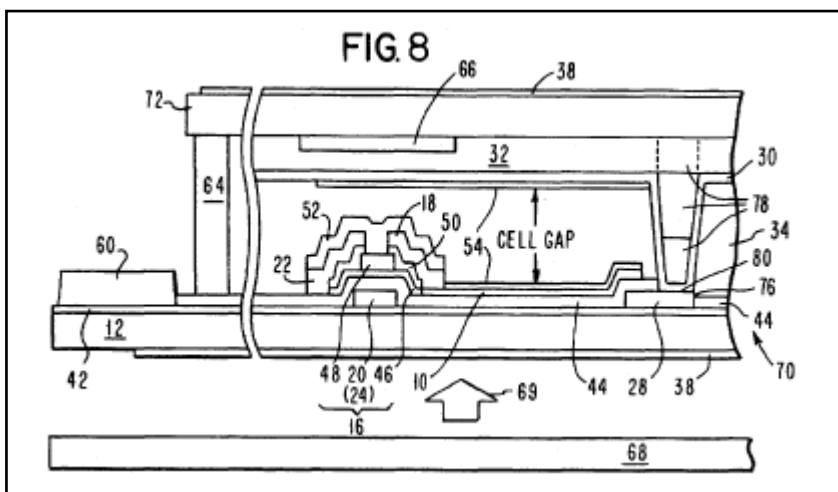
A pillar of a color filter on a facing substrate requires only change of mask patterns for the color filter but the number of processes does not increase. Moreover, it is possible to form a pillar by laminating red, green, and blue color filters or any two color filters of them. Furthermore, any sequence of colors to be laminated is not determined for a color-filter laminating portion. Furthermore, it is possible to fine-adjust a cell gap by forming a laminate structure containing a plurality of conductive materials at a position on an array substrate where a pillar is fitted on a facing substrate, connecting the laminate structure to a common electrode on

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the facing substrate through a conductive body layer electrically connected to a storage capacitance line, and specifying the cell gap by the sum of the height of the laminate structure on the array substrate and that of the pillar on the facing substrate.

5:57-6:5

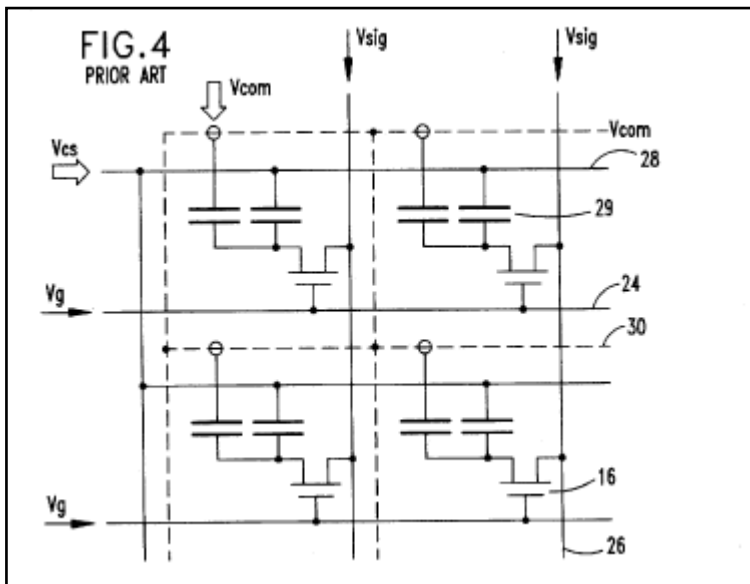
**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED  
HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**  
**(cont’d):**



Furthermore, as shown in FIG. 8, the embodiment 1 may have a structure in which the gate insulating film 44 is formed on the storage capacitance line 28 in a pixel area on the array substrate 12. That is, the embodiment 1 has a structure in which a hole 76 is formed at part of the gate insulating film 44 on the storage capacitance line 28, the common electrode 30 at a portion covering the pillar 78 of a color filter formed on the color filter substrate 72 is overlapped with the position of the hole 76, and the common electrode 30 contacts the storage capacitance line 28 so that they are electrically connected each other. Though the

7:4-13

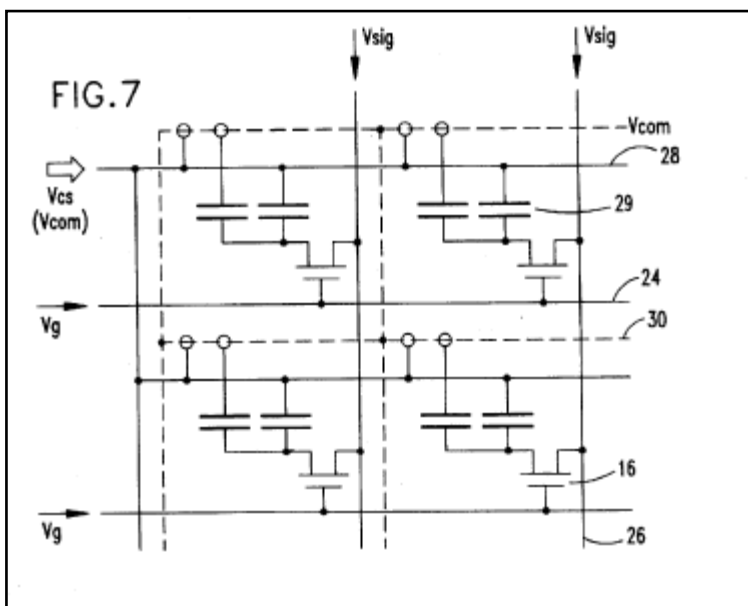
**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**  
**(cont’d):**



Moreover, the present invention does not require a spherical spacer for specifying a cell gap or transfer for supplying a potential to the common electrode 30 as shown in FIG. 8. However, there is no problem in using the spacer and transfer. The equivalent circuit of the TFT-LCD of the present invention is shown in FIG. 7 for comparison with the circuit in FIG. 4. As shown in FIG. 7, the advantages are obtained that the problem of signal delay of Vcom is solved because Vcom is equal to Vcs everywhere in a screen by applying the present invention and it is unnecessary to independently supply Vcom from the outside.

7:32-42

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**(cont’d):**



Moreover, the present invention does not require a spherical spacer for specifying a cell gap or transfer for supplying a potential to the common electrode 30 as shown in FIG. 8. However, there is no problem in using the spacer and transfer. The equivalent circuit of the TFT-LCD of the present invention is shown in FIG. 7 for comparison with the circuit in FIG. 4. As shown in FIG. 7, the advantages are obtained that the problem of signal delay of Vcom is solved because Vcom is equal to Vcs everywhere in a screen by applying the present invention and it is unnecessary to independently supply Vcom from the outside.

7:32-42

**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED  
HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”  
(cont’d):**

As another method for connecting a common electrode with a storage capacitance line, the storage capacitance line 28 may be formed on the pixel electrode 10 formed on the array substrate 12 through the insulating film 74. In this case, a joint 80 between the storage capacitance line 28 and the common electrode 30 covering the pillar 78 of a color filter is three-dimensionally superimposed on a storage capacitance area 82.

In the case of the third embodiment, a layer 84 made of a conductive body such as a metal formed simultaneously with the data line 26 is first formed on the storage capacitance line 28, and then it is connected with the common electrode 30 to constitute the joint 80 instead of directly connecting the common electrode 30 to the storage capacitance line 28 like the first and second embodiments. Therefore, it is possible to perform fine adjustment for realizing an optically-optimized cell gap by the formation of the conductive body.

7:44-61

**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER” (cont’d):**

Then, the process for manufacturing the liquid crystal display panel **70** of this embodiment is described below.

First, the process for manufacturing the array substrate **12** is described below.

In the first process, the undercoat layer **42** is formed on the array substrate **12**.

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In the second process, the gate electrode **20**, gate line **24**, and storage capacitance line **28** are formed on the undercoat layer **42**.

In the third process, the gate insulating film **44** is formed.

In the fourth process, the semiconductor layer **46** of the TFT **16** is formed.

In the fifth process, the pixel electrode **10** is formed.

In the sixth process, the hole **76** is formed on part of the gate insulating film **44** on the storage capacitance line **28**.

In the seventh process, the source electrode **18** and drain electrode **22** of the TFT **16** and the data line **26** are formed.

In the eighth process, the passivation film **52** covering the TFT **16** is formed.

In the ninth process, the alignment film **54** is formed and treated through rubbing.

Then, the method for manufacturing the color filter substrate **72** is described below.

In the first process, the color filter **32** is formed on the facing substrate **14**, and the pillar **78** of a color filter is formed at a position corresponding to the hole **76** on the array substrate **12**.

In the second process, the common electrode **30** is formed on the color filter **32**.

In the third process, the alignment film **54** is formed and treated through rubbing.

The array substrate **12** and the color filter substrate **77** finished through the above processes are made to face each other and the storage capacitance line **28** viewed through the hole **76** on the array substrate **12** is overlapped with the common electrode **30** at the portion covering the pillar **78** of a color filter on the facing substrate **14** to electrically connect them each other.

Then, the liquid crystal display panel **70** is finished by sealing the perimeter of the assembly with a sealant **64**, injecting liquid crystal into the assembly through an injection hole (not illustrated), and closing the injection hole.

7:62-8:39

**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED  
HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”  
(cont’d):**

The present invention provides a large high-definition liquid crystal display without causing a signal delay even around the central portion of a common electrode. Moreover, because the present invention disuses processes for scattering spacers and dotting transfers, the yield is improved and the cost is decreased.

8:39-45

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(cont’d):**

It is said to be unclear in Claims 1 and 5 which elements are “formed higher than other portions” and specify “a cell gap together with objects formed on the array substrate”. These elements are the pillars, which are now expressly identified. It is asked also which elements are electrically connected to the storage capacitance line. The answer is the portions of the common electrode covering at least some of the pillars. This has been clarified as well. The phrase “working on all pixels” is said to be not understood. This phrase merely refers to the fact that the common electrode is the common electrode for all of the pixels. This phrase has been deleted and the concept moved forward in Claims 1 and 5.

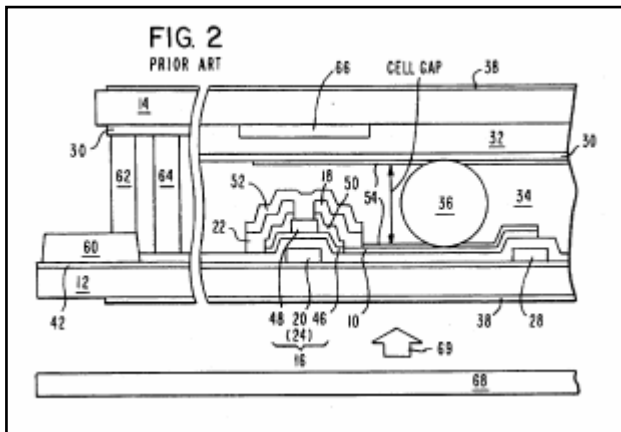
App. 08/615,012, 08/05/1997  
Amendment, pg. 6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE PILLARS ARE COVERED WITH THE COMMON ELECTRODE”:**

To prevent a signal delay of an active-matrix liquid crystal display from occurring in an active-matrix liquid crystal display having an active element for each pixel electrode, a potential is supplied to a common electrode from a storage capacitance line by forming a pillar of a color filter to specify a cell gap between an array substrate having the storage capacitance line and a facing substrate having the color filter and electrically connecting the common electrode covering the pillar of the color filter with the storage capacitance line on the array substrate. Thereby, it is possible to disuse a transfer dotting process which is a factor of decreasing the yield and also a factor of decreasing the effective display area. Moreover, because the potential is supplied to the common electrode from the storage capacitance line, it is possible to prevent a signal delay of the common electrode from occurring and moreover realize a high-image-quality screen even in a large and high-definition liquid crystal display without causing irregularity of a display screen or decrease of a contrast ratio.

Abstract

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE PILLARS ARE COVERED WITH THE COMMON ELECTRODE” (cont’d):**



Among these layers and films, the undercoat layer 42, channel protective layer 48, passivation film 52, and alignment film 54 may not be deposited. A common electrode 30 is formed at the facing substrate 14 side of the TFT-LCD correspondingly to an area in which pixel electrodes 10 on the array substrate 12 are arranged like a matrix. Input signals are supplied to an OLB (Outer Lead Bonding) electrode 60 extended from a pixel area in which the pixel electrode 10 on the array substrate 12 is formed up to the perimeter of the area. Among the potentials of these signals, the potential of the common electrode 30 on the facing substrate is supplied from a plurality of portions of electrodes on the array substrate through a transfer 62 using

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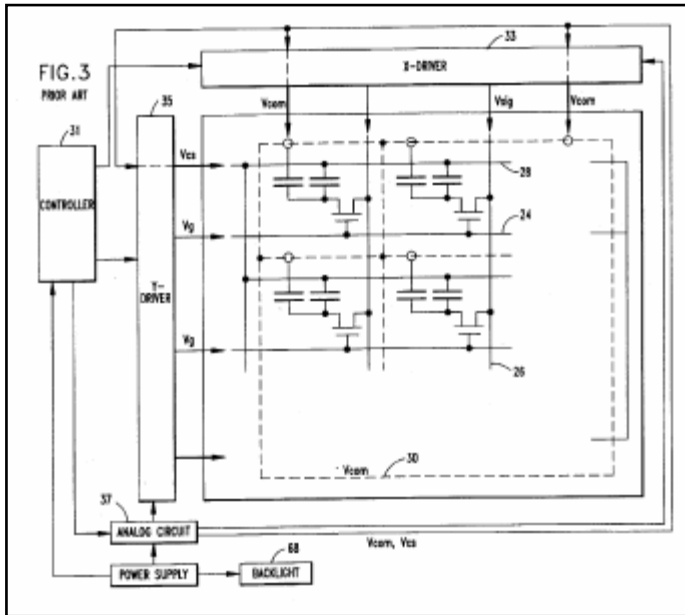
conductive paste at the outside of the pixel area. The common electrode 30 is made of a transparent material such as ITO (Indium Tin Oxide) because it is necessary to pass light through the electrode 30. However, because the material has a large electric resistance, the electric resistance

1:57 - 2:4

Furthermore, a black matrix 66 is formed like a lattice. In the case of an existing liquid crystal display, transparent spherical spacers 36 are scattered in a liquid crystal layer 34 held by the array substrate 12 and the facing substrate 14 in order to keep a predetermined interval between the two substrates 12 and 14. Moreover, liquid crystal is sealed between the two substrates by a sealant 64. Furthermore, a polarizing

2:13-19

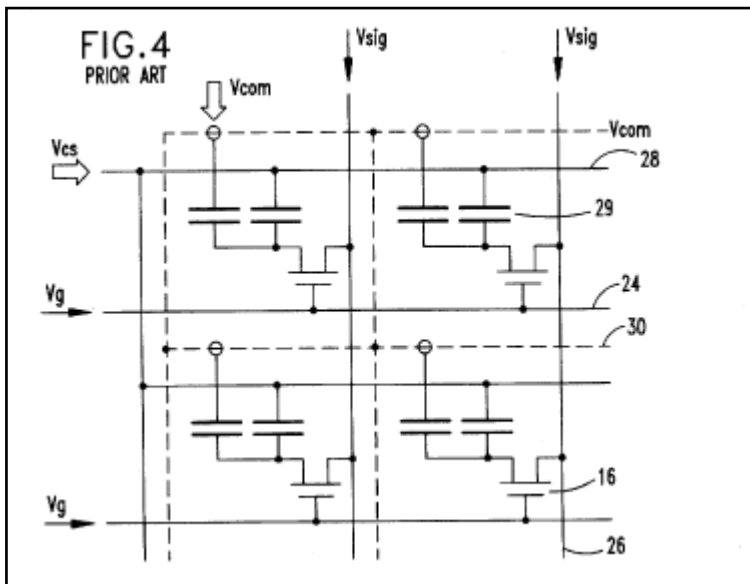
**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE PILLARS ARE COVERED WITH THE COMMON ELECTRODE” (cont’d):**



FIGS. 3 and 4 show an equivalent circuit of an existing TFT-LCD. An input signal supplied to the existing TFT-LCD is described below by referring to FIGS. 3 and 4. A controller 31 converts image data into a form to be supplied to an X-driver 33 and a Y-driver 35 of a driver IC. Moreover, an analog circuit 37 generates a voltage for each input signal. Input signals to be supplied to the TFT-LCD include a scanning signal (Vg) of a gate line 24 supplied from the Y-driver 35, a display signal (Vsig) of a data line 26 supplied from the X-driver 33, a common-electrode potential (Vcom) of a common electrode 30, and a storage capacitance line potential (Vcs) of a storage capacitance line 28. The potentials of these input signals are all supplied to the OLB electrode 60 extended from the pixel area in which the pixel electrodes 10 on the array substrate 12 are formed up to the perimeter of the area as shown in FIG. 2. Then, among the potentials of these input signals, the potential Vcom is supplied to the common electrode 30 through the transfer 62.

2:25-42

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE PILLARS ARE COVERED WITH THE COMMON ELECTRODE” (cont’d):**



FIGS. 3 and 4 show an equivalent circuit of an existing TFT-LCD. An input signal supplied to the existing TFT-LCD is described below by referring to FIGS. 3 and 4. A controller 31 converts image data into a form to be supplied to an X-driver 33 and a Y-driver 35 of a driver IC. Moreover, an analog circuit 37 generates a voltage for each input signal. Input signals to be supplied to the TFT-LCD include a scanning signal ( $V_g$ ) of a gate line 24 supplied from the Y-driver 35, a display signal ( $V_{sig}$ ) of a data line 26 supplied from the X-driver 33, a common-electrode potential ( $V_{com}$ ) of a common electrode 30, and a storage capacitance line potential ( $V_{cs}$ ) of a storage capacitance line 28. The potentials of these input signals are all supplied to the OLB electrode 60 extended from the pixel area in which the pixel electrodes 10 on the array substrate 12 are formed up to the perimeter of the area as shown in FIG. 2. Then, among the potentials of these input signals, the potential  $V_{com}$  is supplied to the common electrode 30 through the transfer 62.

2:25-42

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE PILLARS ARE COVERED WITH THE COMMON ELECTRODE” (cont’d):**

A driving method in which a polarity is inverted because the potential of a common electrode at the facing substrate side synchronizes with the display signal  $V_{sig}$  is referred to as common-voltage AC inversion driving ( $V_{com}$  inversion) which is distinguished from a method in which common voltage is constant. The  $V_{com}$  inversion driving has an advantage that the maximum voltage amplitude of the

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display signal  $V_{sig}$  can be decreased because the voltage amplitude of the common electrode biased to the voltage amplitude of the display signal  $V_{sig}$  is applied to a liquid crystal layer. It is requested from the market of the TFT-LCD

2:61 - 3:4

Moreover, as shown in FIG. 2, the transparent spherical spacers 36 (made of plastic and glass fiber) are hitherto

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scattered in the liquid crystal layer 34 held by the array substrate 12 and the facing substrate 14 constituting a liquid crystal display in order to keep the substrates 12 and 14 at a predetermined interval. However, under the spacers kept scattered, liquid crystal flows in a panel when an external force is applied to the panel, the spacers are moved in a cell plane due to the flowing of the liquid crystal, and thereby the spacers may scratch the surface of the thin alignment film 54 due to the movement of the spacers. Moreover, a cell gap (interval between electrodes of two substrates) may not be kept constant due to coagulation of the spacers. Unless the cell gap is kept constant, the optical path length difference (product of the birefringence rate and cell gap of the liquid crystal) of the liquid crystal layer changes and thereby, the contrast ratio and the chromaticity of a display screen are changed. Thus, problems occur that the uniformity of the screen cannot be kept or the display quality is deteriorated. Moreover, the spacers are brightened or coagulated, and the light from the backlight 68 is cut off by the coagulated spacers and thereby the screen is blackened by the degree of cut-off light. To solve these problems, various structures are

3:66 – 4:21

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE PILLARS ARE COVERED WITH THE COMMON ELECTRODE” (cont’d):**

Moreover, the spacers are brightened or coagulated, and the light from the backlight 68 is cut off by the coagulated spacers and thereby the screen is blackened by the degree of cut-off light. To solve these problems, various structures are already disclosed which disuse transparent spherical spacers and instead, specify a cell gap by a pillar formed on the array substrate 12 and/or the facing substrate 14 (official gazettes of Japanese Patent Laid-Open Nos. 164723/1985, 105583/1986, 24230/1989, 134733/1986, 163428/1902, 250416/1987, and 196946/1993). However, any one of these disclosures does not show means for solving the problem of signal delay in a TFT-LCD using the H/com inversion driving method.

4:21-30

Moreover, as shown in FIG. 2, the existing TFT-LCD has a problem in the structure of supplying the potential of the common electrode 30 on the facing substrate 14 from a plurality of portions at the perimeter of a pixel area of the array substrate 12 side to the common electrode 30 on the facing substrate 14 through the transfer 62 using conductive paste. Because this structure requires a high-accuracy alignment of the transfer 62, it uses two or more transfers to prevent defectives from being produced due to a deviation of a transfer. However, the manufacturing yield is decreased due to defectives produced in a process for dotting a transfer. Moreover, there is the restriction on design that an area for dotting a transfer must be formed at the perimeter of a pixel area. That is, because an area independent of display must exclusively be formed on the array substrate 12 and the facing substrate 14, an effective display area to a substrate size is decreased. However, it is inevitable to use the above structure because it is indispensable for an existing liquid crystal display in view of design.

4:31-49

**SUMMARY OF THE INVENTION**

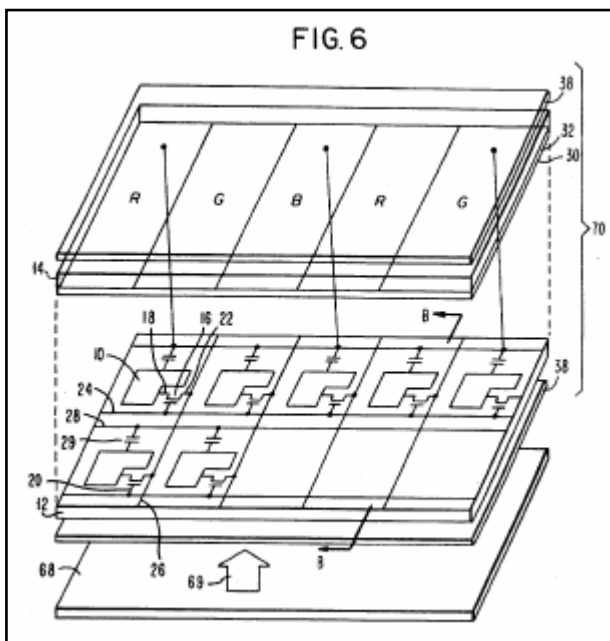
It is an object of the present invention to provide a TFT-LCD making it possible to prevent a signal delay from occurring even around the central portion of a common electrode and moreover prevent irregularity of a display screen and decrease of a contrast ration from occurring.

It is another object of the present invention to provide a TFT-LCD making it possible to keep a cell gap constant without using spacers.

It is still another object of the present invention to provide a TFT-LCD making it possible to supply a potential to a common electrode on a facing substrate without dotting a transfer.

4:51-64

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE PILLARS ARE COVERED WITH THE COMMON ELECTRODE” (cont’d):**



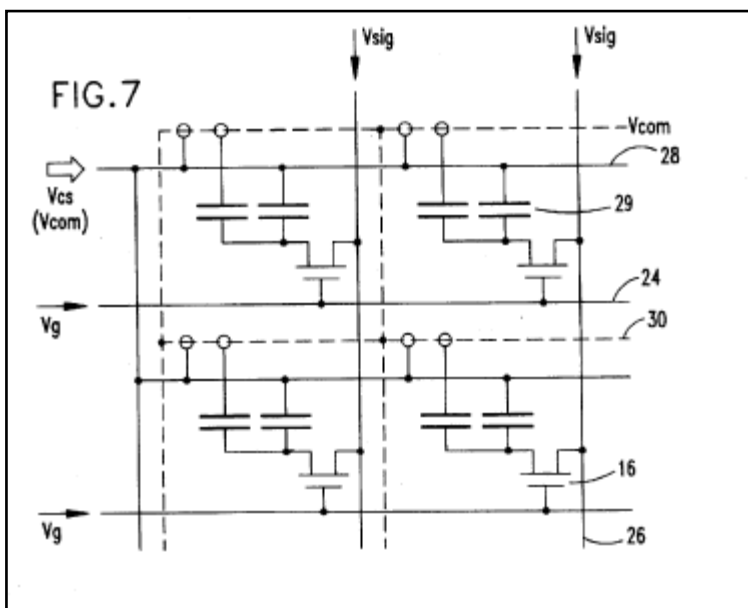
As shown in FIG. 8, the present invention uses a pillar 78 of a color filter 32 instead of a spacer in order to keep a cell gap between two substrates constant. Then, a signal delay of

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a common electrode 30 is prevented from occurring by forming a portion for electrically connecting a common electrode 30 covering the pillar 78 of the color filter 32 with a storage capacitance line 28 everywhere in a pixel area and supplying a potential of the common electrode 30 from the storage capacitance line 28.

4:65-5:6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE PILLARS ARE COVERED WITH THE COMMON ELECTRODE” (cont’d):**



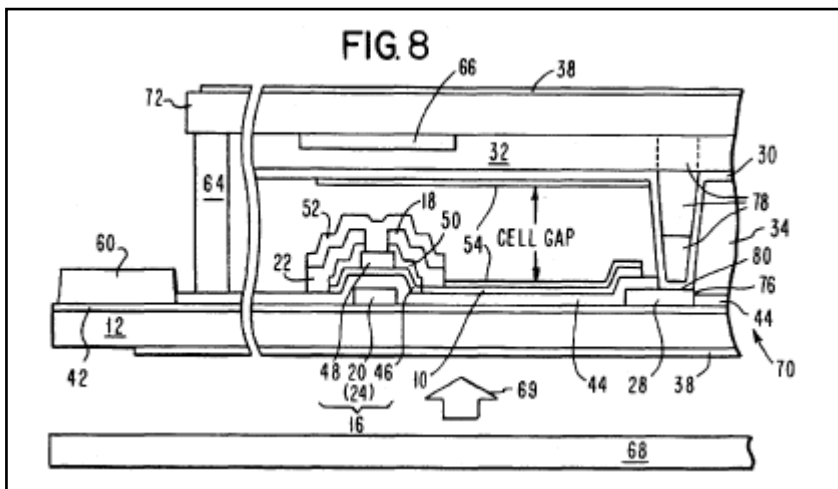
As shown in FIG. 8, the present invention uses a pillar 78 of a color filter 32 instead of a spacer in order to keep a cell gap between two substrates constant. Then, a signal delay of

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a common electrode 30 is prevented from occurring by forming a portion for electrically connecting a common electrode 30 covering the pillar 78 of the color filter 32 with a storage capacitance line 28 everywhere in a pixel area and supplying a potential of the common electrode 30 from the storage capacitance line 28.

4:65-5:6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE PILLARS ARE COVERED WITH THE COMMON ELECTRODE” (cont’d):**



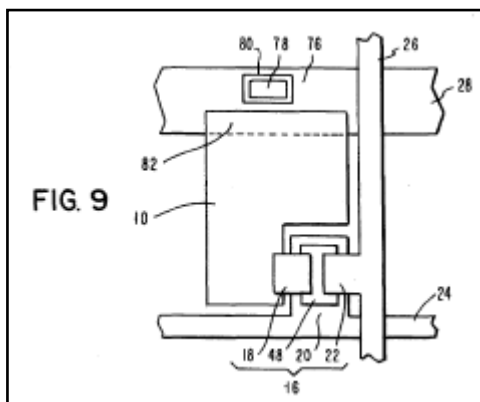
As shown in FIG. 8, the present invention uses a pillar 78 of a color filter 32 instead of a spacer in order to keep a cell gap between two substrates constant. Then, a signal delay of

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a common electrode 30 is prevented from occurring by forming a portion for electrically connecting a common electrode 30 covering the pillar 78 of the color filter 32 with a storage capacitance line 28 everywhere in a pixel area and supplying a potential of the common electrode 30 from the storage capacitance line 28.

4:65-5:6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE PILLARS ARE COVERED WITH THE COMMON ELECTRODE” (cont’d):**



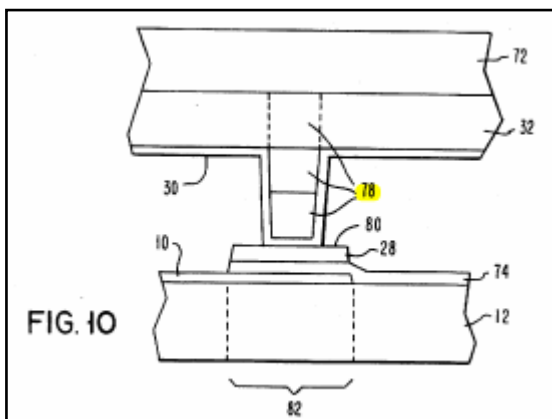
As shown in FIG. 8, the present invention uses a pillar 78 of a color filter 32 instead of a spacer in order to keep a cell gap between two substrates constant. Then, a signal delay of

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a common electrode 30 is prevented from occurring by forming a portion for electrically connecting a common electrode 30 covering the pillar 78 of the color filter 32 with a storage capacitance line 28 everywhere in a pixel area and supplying a potential of the common electrode 30 from the storage capacitance line 28.

4:65-5:6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE PILLARS ARE COVERED WITH THE COMMON ELECTRODE” (cont’d):**



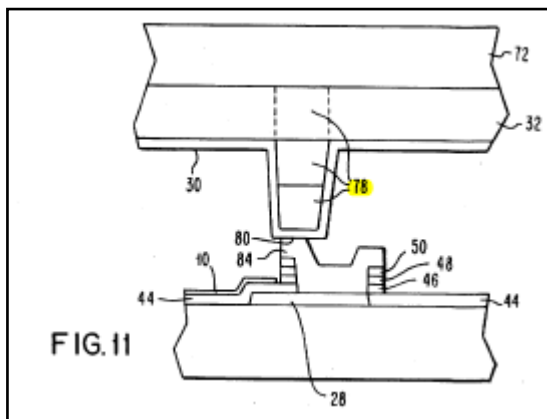
As shown in FIG. 8, the present invention uses a pillar 78 of a color filter 32 instead of a spacer in order to keep a cell gap between two substrates constant. Then, a signal delay of

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a common electrode 30 is prevented from occurring by forming a portion for electrically connecting a common electrode 30 covering the pillar 78 of the color filter 32 with a storage capacitance line 28 everywhere in a pixel area and supplying a potential of the common electrode 30 from the storage capacitance line 28.

4:65-5:6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE PILLARS ARE COVERED WITH THE COMMON ELECTRODE” (cont’d):**



As shown in FIG. 8, the present invention uses a pillar 78 of a color filter 32 instead of a spacer in order to keep a cell gap between two substrates constant. Then, a signal delay of

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a common electrode 30 is prevented from occurring by forming a portion for electrically connecting a common electrode 30 covering the pillar 78 of the color filter 32 with a storage capacitance line 28 everywhere in a pixel area and supplying a potential of the common electrode 30 from the storage capacitance line 28.

4:65-5:6

According to the present invention, the potential of the storage capacitance line 28 is supplied to the common electrode 30 on a facing substrate from joints formed everywhere in a pixel area. Originally, the common-

5:7-10

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE PILLARS ARE COVERED WITH THE COMMON ELECTRODE” (cont’d):**

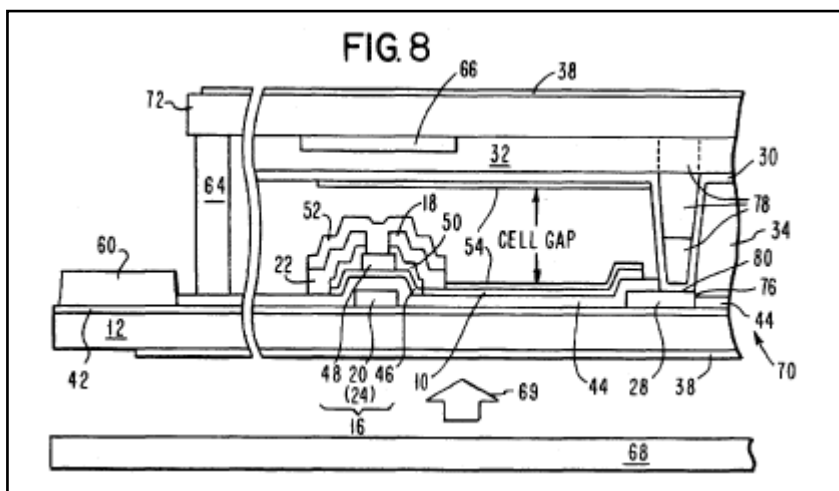
A pillar of a color filter on a facing substrate requires only change of mask patterns for the color filter but the number of processes does not increase. Moreover, it is possible to form a pillar by laminating red, green, and blue color filters or any two color filters of them. Furthermore, any sequence of colors to be laminated is not determined for a color-filter laminating portion. Furthermore, it is possible to fine-adjust a cell gap by forming a laminate structure containing a plurality of conductive materials at a position on an array substrate where a pillar is fitted on a facing substrate, connecting the laminate structure to a common electrode on

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the facing substrate through a conductive body layer electrically connected to a storage capacitance line, and specifying the cell gap by the sum of the height of the laminate structure on the array substrate and that of the pillar on the facing substrate.

5:57-6:5

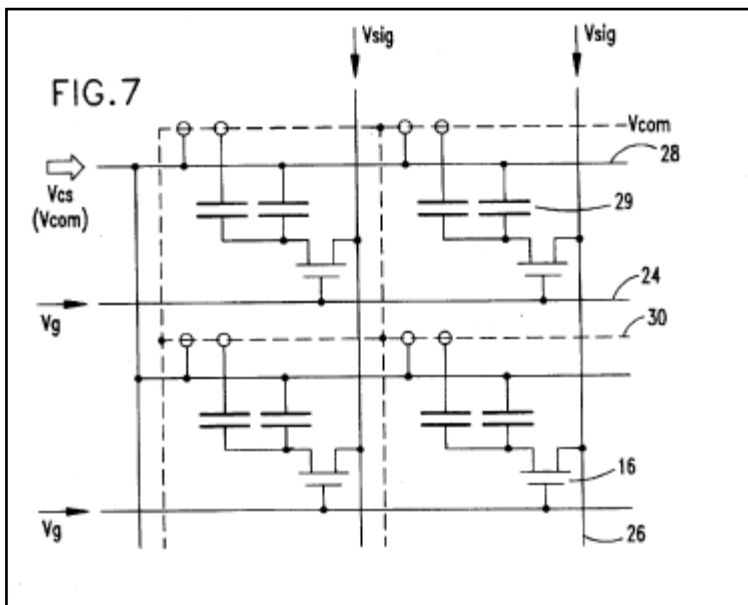
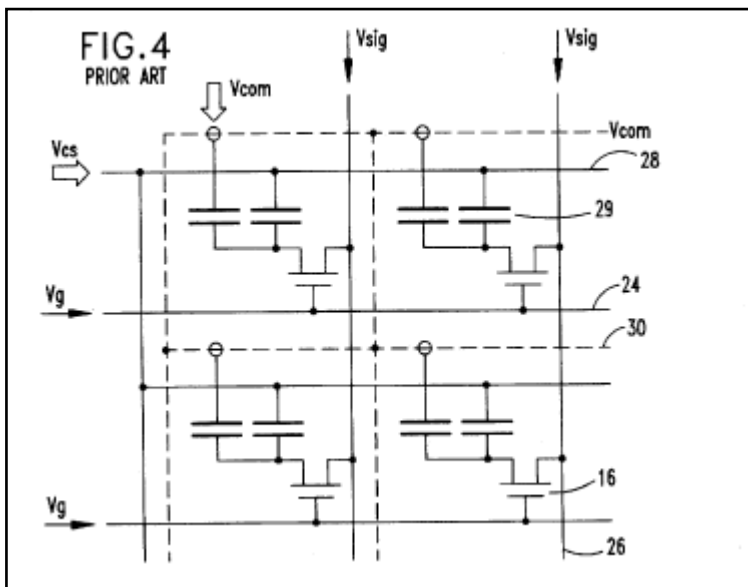
**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE PILLARS ARE COVERED WITH THE COMMON ELECTRODE” (cont’d):**



Furthermore, as shown in FIG. 8, the embodiment 1 may have a structure in which the gate insulating film 44 is formed on the storage capacitance line 28 in a pixel area on the array substrate 12. That is, the embodiment 1 has a structure in which a hole 76 is formed at part of the gate insulating film 44 on the storage capacitance line 28, the common electrode 30 at a portion covering the pillar 78 of a color filter formed on the color filter substrate 72 is overlapped with the position of the hole 76, and the common electrode 30 contacts the storage capacitance line 28 so that they are electrically connected each other. Though the

7:4-13

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE PILLARS ARE COVERED WITH THE COMMON ELECTRODE” (cont’d):**



Moreover, the present invention does not require a spherical spacer for specifying a cell gap or transfer for supplying a potential to the common electrode 30 as shown in FIG. 8. However, there is no problem in using the spacer and transfer. The equivalent circuit of the TFT-LCD of the present invention is shown in FIG. 7 for comparison with the circuit in FIG. 4. As shown in FIG. 7, the advantages are obtained that the problem of signal delay of Vcom is solved because Vcom is equal to Vcs everywhere in a screen by applying the present invention and it is unnecessary to independently supply Vcom from the outside.

7:32-42

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE PILLARS ARE COVERED WITH THE COMMON ELECTRODE” (cont’d):**

As another method for connecting a common electrode with a storage capacitance line, the storage capacitance line 28 may be formed on the pixel electrode 10 formed on the array substrate 12 through the insulating film 74. In this case, a joint 80 between the storage capacitance line 28 and the common electrode 30 covering the pillar 78 of a color filter is three-dimensionally superimposed on a storage capacitance area 82.

In the case of the third embodiment, a layer 84 made of a conductive body such as a metal formed simultaneously with the data line 26 is first formed on the storage capacitance line 28, and then it is connected with the common electrode 30 to constitute the joint 80 instead of directly connecting the common electrode 30 to the storage capacitance line 28 like the first and second embodiments. Therefore, it is possible to perform fine adjustment for realizing an optically-optimized cell gap by the formation of the conductive body.

7:44-61

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE PILLARS ARE COVERED WITH THE COMMON ELECTRODE” (cont’d):**

Then, the process for manufacturing the liquid crystal display panel 70 of this embodiment is described below.

First, the process for manufacturing the array substrate 12 is described below.

In the first process, the undercoat layer 42 is formed on the array substrate 12.

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In the second process, the gate electrode 20, gate line 24, and storage capacitance line 28 are formed on the undercoat layer 42.

In the third process, the gate insulating film 44 is formed.

In the fourth process, the semiconductor layer 46 of the TFT 16 is formed.

In the fifth process, the pixel electrode 10 is formed.

In the sixth process, the hole 76 is formed on part of the gate insulating film 44 on the storage capacitance line 28.

In the seventh process, the source electrode 18 and drain electrode 22 of the TFT 16 and the data line 26 are formed.

In the eighth process, the passivation film 52 covering the TFT 16 is formed.

In the ninth process, the alignment film 54 is formed and treated through rubbing.

Then, the method for manufacturing the color filter substrate 72 is described below.

In the first process, the color filter 32 is formed on the facing substrate 14, and the pillar 78 of a color filter is formed at a position corresponding to the hole 76 on the array substrate 12.

In the second process, the common electrode 30 is formed on the color filter 32.

In the third process, the alignment film 54 is formed and treated through rubbing.

The array substrate 12 and the color filter substrate 77 finished through the above processes are made to face each other and the storage capacitance line 28 viewed through the hole 76 on the array substrate 12 is overlapped with the common electrode 30 at the portion covering the pillar 78 of a color filter on the facing substrate 14 to electrically connect them each other.

Then, the liquid crystal display panel 70 is finished by sealing the perimeter of the assembly with a sealant 64, injecting liquid crystal into the assembly through an injection hole (not illustrated), and closing the injection hole.

7:62-8:39

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE PILLARS ARE COVERED WITH THE COMMON ELECTRODE” (cont’d):**

The present invention provides a large high-definition liquid crystal display without causing a signal delay even around the central portion of a common electrode. Moreover, because the present invention disuses processes for scattering spacers and dotting transfers, the yield is improved and the cost is decreased.

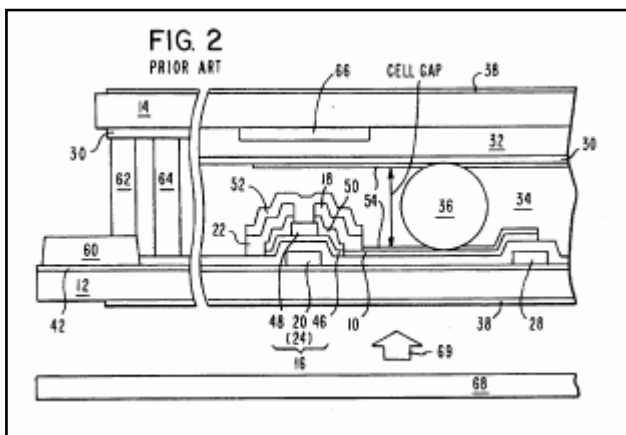
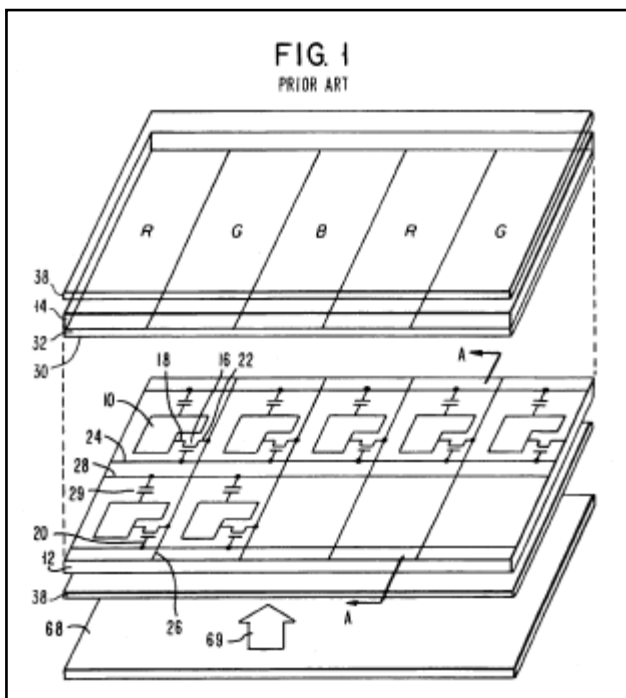
8:39-45

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “STORAGE CAPACITANCE LINE” AND “STORAGE CAPACITANCE LINE FOR OUTPUTTING THE REFERENCE POTENTIAL OF THE STORAGE CAPACITANCE”:**

To prevent a signal delay of an active-matrix liquid crystal display from occurring in an active-matrix liquid crystal display having an active element for each pixel electrode, a potential is supplied to a common electrode from a storage capacitance line by forming a pillar of a color filter to specify a cell gap between an array substrate having the storage capacitance line and a facing substrate having the color filter and electrically connecting the common electrode covering the pillar of the color filter with the storage capacitance line on the array substrate. Thereby, it is possible to disuse a transfer dotting process which is a factor of decreasing the yield and also a factor of decreasing the effective display area. Moreover, because the potential is supplied to the common electrode from the storage capacitance line, it is possible to prevent a signal delay of the common electrode from occurring and moreover realize a high-image-quality screen even in a large and high-definition liquid crystal display without causing irregularity of a display screen or decrease of a contrast ratio.

Abstract

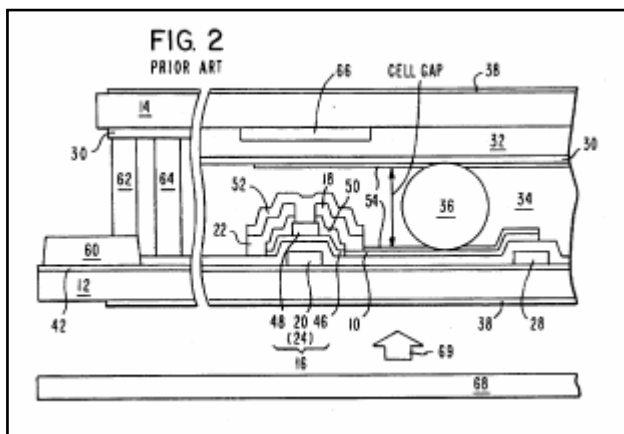
**INTRINSIC EVIDENCE FOR DISPUTED TERMS “STORAGE CAPACITANCE LINE” AND “STORAGE CAPACITANCE LINE FOR OUTPUTTING THE REFERENCE POTENTIAL OF THE STORAGE CAPACITANCE” (cont’d):**



perpendicular to each other. Moreover, each pixel electrode 10 has a necessary capacitance between the pixel electrode 10 and the storage capacitance line 28. This capacitance serves as a storage capacitance 29.

1:45-48

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “STORAGE CAPACITANCE LINE” AND “STORAGE CAPACITANCE LINE FOR OUTPUTTING THE REFERENCE POTENTIAL OF THE STORAGE CAPACITANCE” (cont’d):**

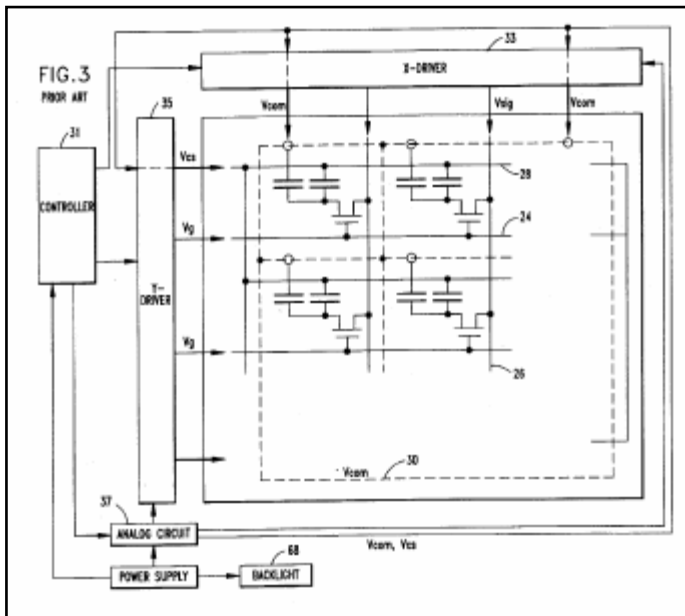


Among these layers and films, the undercoat layer 42, channel protective layer 48, passivation film 52, and alignment film 54 may not be deposited. A common electrode 30 is formed at the facing substrate 14 side of the TFT-LCD correspondingly to an area in which pixel electrodes 10 on the array substrate 12 are arranged like a matrix. Input signals are supplied to an OLB (Outer Lead Bonding) electrode 60 extended from a pixel area in which the pixel electrode 10 on the array substrate 12 is formed up to the perimeter of the area. Among the potentials of these signals, the potential of the common electrode 30 on the facing substrate is supplied from a plurality of portions of electrodes on the array substrate through a transfer 62 using

conductive paste at the outside of the pixel area. The common electrode 30 is made of a transparent material such as ITO (Indium Tin Oxide) because it is necessary to pass light through the electrode 30. However, because the material has a large electric resistance, the electric resistance

1:57 - 2:4

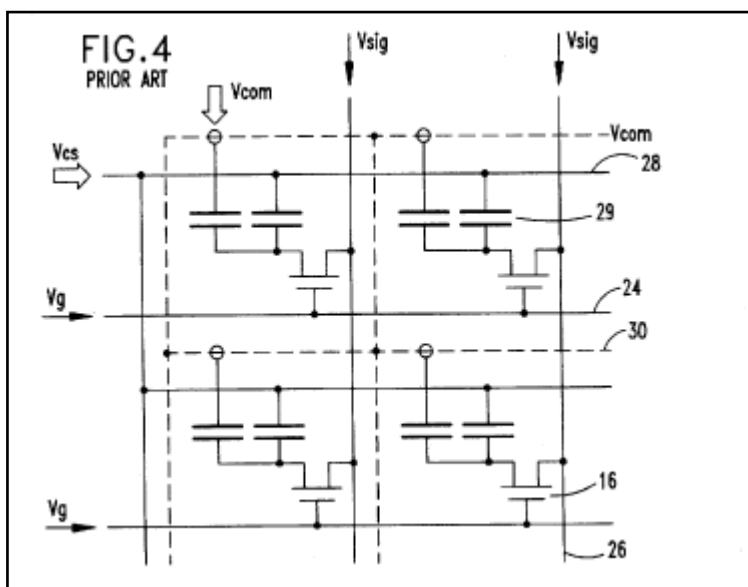
**INTRINSIC EVIDENCE FOR DISPUTED TERMS “STORAGE CAPACITANCE LINE” AND “STORAGE CAPACITANCE LINE FOR OUTPUTTING THE REFERENCE POTENTIAL OF THE STORAGE CAPACITANCE” (cont’d):**



**FIGS. 3 and 4 show an equivalent circuit of an existing TFT-LCD. An input signal supplied to the existing TFT-LCD is described below by referring to FIGS. 3 and 4. A controller 31 converts image data into a form to be supplied to an X-driver 33 and a Y-driver 35 of a driver IC. Moreover, an analog circuit 37 generates a voltage for each input signal. Input signals to be supplied to the TFT-LCD include a scanning signal ( $V_g$ ) of a gate line 24 supplied from the Y-driver 35, a display signal ( $V_{sig}$ ) of a data line 26 supplied from the X-driver 33, a common-electrode potential ( $V_{com}$ ) of a common electrode 30, and a storage capacitance line potential ( $V_{cs}$ ) of a storage capacitance line 28. The potentials of these input signals are all supplied to the OLB electrode 60 extended from the pixel area in which the pixel electrodes 10 on the array substrate 12 are formed up to the perimeter of the area as shown in FIG. 2. Then, among the potentials of these input signals, the potential  $V_{com}$  is supplied to the common electrode 30 through the transfer 62.**

2:25-42

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “STORAGE CAPACITANCE LINE” AND “STORAGE CAPACITANCE LINE FOR OUTPUTTING THE REFERENCE POTENTIAL OF THE STORAGE CAPACITANCE” (cont’d):**



FIGS. 3 and 4 show an equivalent circuit of an existing TFT-LCD. An input signal supplied to the existing TFT-LCD is described below by referring to FIGS. 3 and 4. A controller 31 converts image data into a form to be supplied to an X-driver 33 and a Y-driver 35 of a driver IC. Moreover, an analog circuit 37 generates a voltage for each input signal. Input signals to be supplied to the TFT-LCD include a scanning signal (Vg) of a gate line 24 supplied from the Y-driver 35, a display signal (Vsig) of a data line 26 supplied from the X-driver 33, a common-electrode potential (Vcom) of a common electrode 30, and a storage capacitance line potential (Vcs) of a storage capacitance line 28. The potentials of these input signals are all supplied to the OLB electrode 60 extended from the pixel area in which the pixel electrodes 10 on the array substrate 12 are formed up to the perimeter of the area as shown in FIG. 2. Then, among the potentials of these input signals, the potential Vcom is supplied to the common electrode 30 through the transfer 62.

2:25-42

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “STORAGE CAPACITANCE LINE” AND “STORAGE CAPACITANCE LINE FOR OUTPUTTING THE REFERENCE POTENTIAL OF THE STORAGE CAPACITANCE” (cont’d):**

A driving method in which a polarity is inverted because the potential of a common electrode at the facing substrate side synchronizes with the display signal Vsig is referred to as common-voltage AC inversion driving (Vcom inversion) which is distinguished from a method in which common voltage is constant. The Vcom inversion driving has an advantage that the maximum voltage amplitude of the

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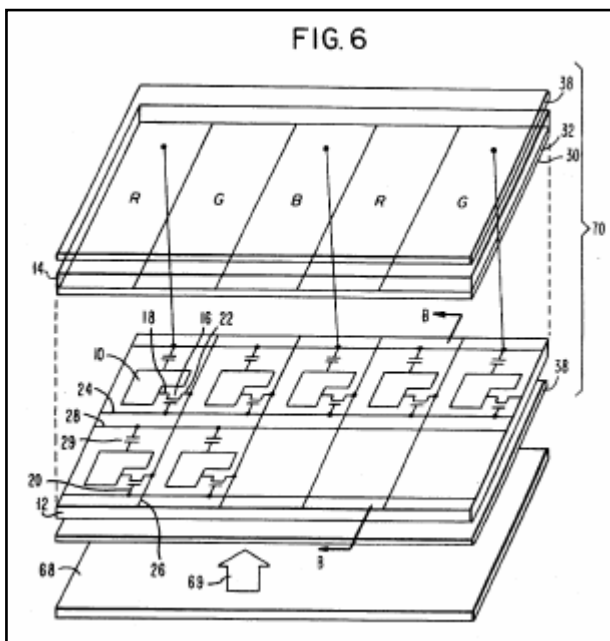
display signal Vsig can be decreased because the voltage amplitude of the common electrode biased to the voltage amplitude of the display signal Vsig is applied to a liquid crystal layer. It is requested from the market of the TFT-LCD

2:61 - 3:4

Moreover, as shown in FIG. 2, the existing TFT-LCD has a problem in the structure of supplying the potential of the common electrode 30 on the facing substrate 14 from a plurality of portions at the perimeter of a pixel area of the array substrate 12 side to the common electrode 30 on the facing substrate 14 through the transfer 62 using conductive paste. Because this structure requires a high-accuracy alignment of the transfer 62, it uses two or more transfers to prevent defectives from being produced due to a deviation of a transfer. However, the manufacturing yield is decreased due to defectives produced in a process for dotting a transfer. Moreover, there is the restriction on design that an area for dotting a transfer must be formed at the perimeter of a pixel area. That is, because an area independent of display must exclusively be formed on the array substrate 12 and the facing substrate 14, an effective display area to a substrate size is decreased. However, it is inevitable to use the above structure because it is indispensable for an existing liquid crystal display in view of design.

4:31-49

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “STORAGE CAPACITANCE LINE” AND “STORAGE CAPACITANCE LINE FOR OUTPUTTING THE REFERENCE POTENTIAL OF THE STORAGE CAPACITANCE” (cont’d):**

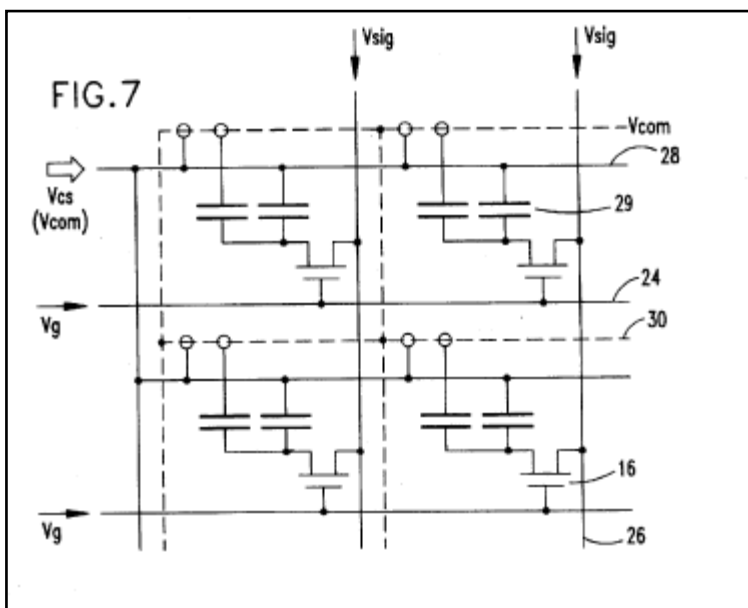


As shown in FIG. 8, the present invention uses a pillar 78 of a color filter 32 instead of a spacer in order to keep a cell gap between two substrates constant. Then, a signal delay of

a common electrode 30 is prevented from occurring by forming a portion for electrically connecting a common electrode 30 covering the pillar 78 of the color filter 32 with a storage capacitance line 28 everywhere in a pixel area and supplying a potential of the common electrode 30 from the storage capacitance line 28.

4:65-5:6

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “STORAGE CAPACITANCE LINE” AND “STORAGE CAPACITANCE LINE FOR OUTPUTTING THE REFERENCE POTENTIAL OF THE STORAGE CAPACITANCE” (cont’d):**



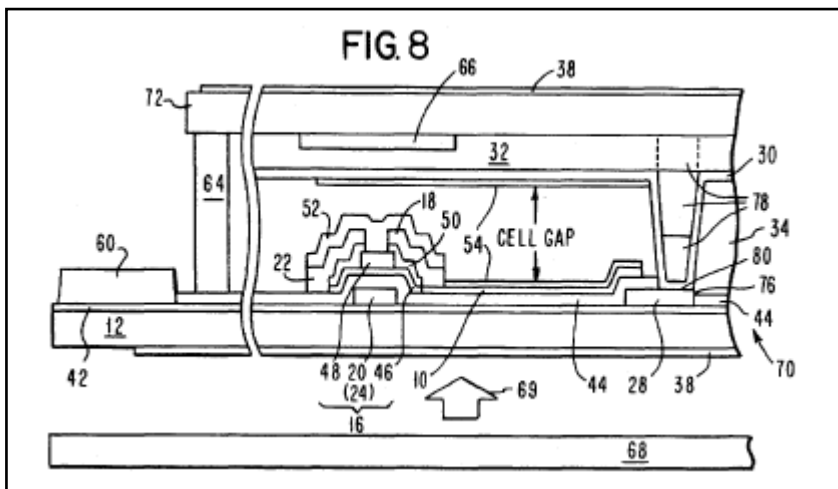
As shown in FIG. 8, the present invention uses a pillar 78 of a color filter 32 instead of a spacer in order to keep a cell gap between two substrates constant. Then, a signal delay of

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a common electrode 30 is prevented from occurring by forming a portion for electrically connecting a common electrode 30 covering the pillar 78 of the color filter 32 with a storage capacitance line 28 everywhere in a pixel area and supplying a potential of the common electrode 30 from the storage capacitance line 28.

4:65-5:6

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “STORAGE CAPACITANCE LINE” AND “STORAGE CAPACITANCE LINE FOR OUTPUTTING THE REFERENCE POTENTIAL OF THE STORAGE CAPACITANCE” (cont’d):**



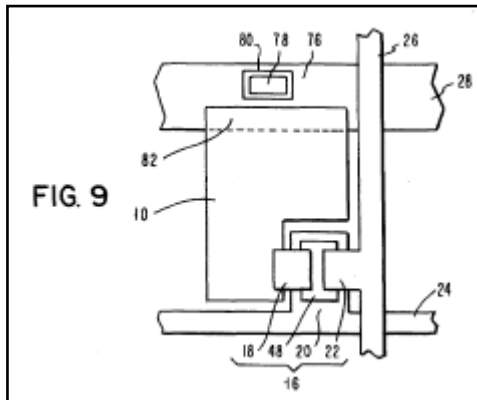
As shown in FIG. 8, the present invention uses a pillar 78 of a color filter 32 instead of a spacer in order to keep a cell gap between two substrates constant. Then, a signal delay of

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a common electrode 30 is prevented from occurring by forming a portion for electrically connecting a common electrode 30 covering the pillar 78 of the color filter 32 with a storage capacitance line 28 everywhere in a pixel area and supplying a potential of the common electrode 30 from the storage capacitance line 28.

4:65-5:6

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “STORAGE CAPACITANCE LINE” AND “STORAGE CAPACITANCE LINE FOR OUTPUTTING THE REFERENCE POTENTIAL OF THE STORAGE CAPACITANCE” (cont’d):**



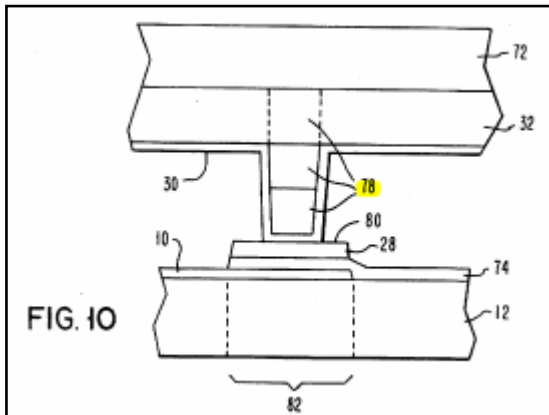
As shown in FIG. 8, the present invention uses a pillar 78 of a color filter 32 instead of a spacer in order to keep a cell gap between two substrates constant. Then, a signal delay of

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a common electrode 30 is prevented from occurring by forming a portion for electrically connecting a common electrode 30 covering the pillar 78 of the color filter 32 with a storage capacitance line 28 everywhere in a pixel area and supplying a potential of the common electrode 30 from the storage capacitance line 28.

4:65-5:6

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “STORAGE CAPACITANCE LINE” AND “STORAGE CAPACITANCE LINE FOR OUTPUTTING THE REFERENCE POTENTIAL OF THE STORAGE CAPACITANCE” (cont’d):**



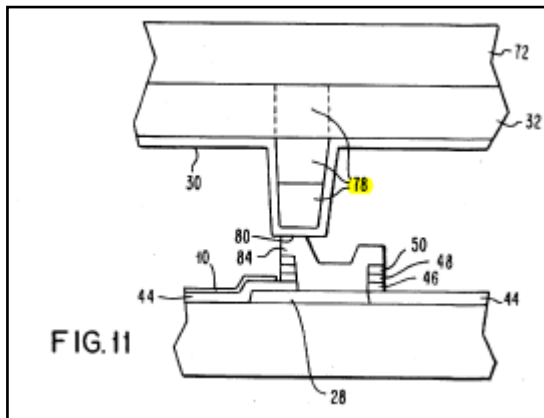
As shown in FIG. 8, the present invention uses a pillar 78 of a color filter 32 instead of a spacer in order to keep a cell gap between two substrates constant. Then, a signal delay of

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4:65-5:6

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “STORAGE CAPACITANCE LINE” AND “STORAGE CAPACITANCE LINE FOR OUTPUTTING THE REFERENCE POTENTIAL OF THE STORAGE CAPACITANCE” (cont’d):**



As shown in FIG. 8, the present invention uses a pillar 78 of a color filter 32 instead of a spacer in order to keep a cell gap between two substrates constant. Then, a signal delay of

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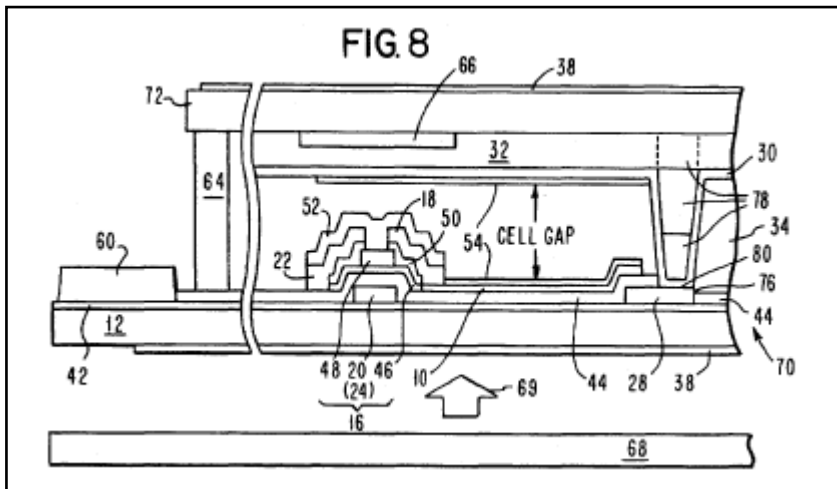
a common electrode 30 is prevented from occurring by forming a portion for electrically connecting a common electrode 30 covering the pillar 78 of the color filter 32 with a storage capacitance line 28 everywhere in a pixel area and supplying a potential of the common electrode 30 from the storage capacitance line 28.

4:65-5:6

According to the present invention, the potential of the storage capacitance line 28 is supplied to the common electrode 30 on a facing substrate from joints formed everywhere in a pixel area. Originally, the common-

5:6-9

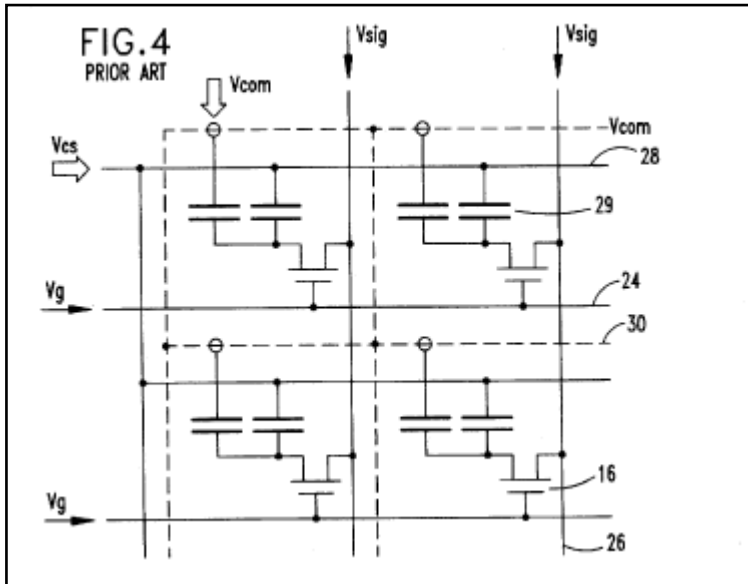
**INTRINSIC EVIDENCE FOR DISPUTED TERMS “STORAGE CAPACITANCE LINE” AND “STORAGE CAPACITANCE LINE FOR OUTPUTTING THE REFERENCE POTENTIAL OF THE STORAGE CAPACITANCE” (cont’d):**



Furthermore, as shown in FIG. 8, the embodiment 1 may have a structure in which the gate insulating film 44 is formed on the storage capacitance line 28 in a pixel area on the array substrate 12. That is, the embodiment 1 has a structure in which a hole 76 is formed at part of the gate insulating film 44 on the storage capacitance line 28, the common electrode 30 at a portion covering the pillar 78 of a color filter formed on the color filter substrate 72 is overlapped with the position of the hole 76, and the common electrode 30 contacts the storage capacitance line 28 so that they are electrically connected each other. Though the

7:4-13

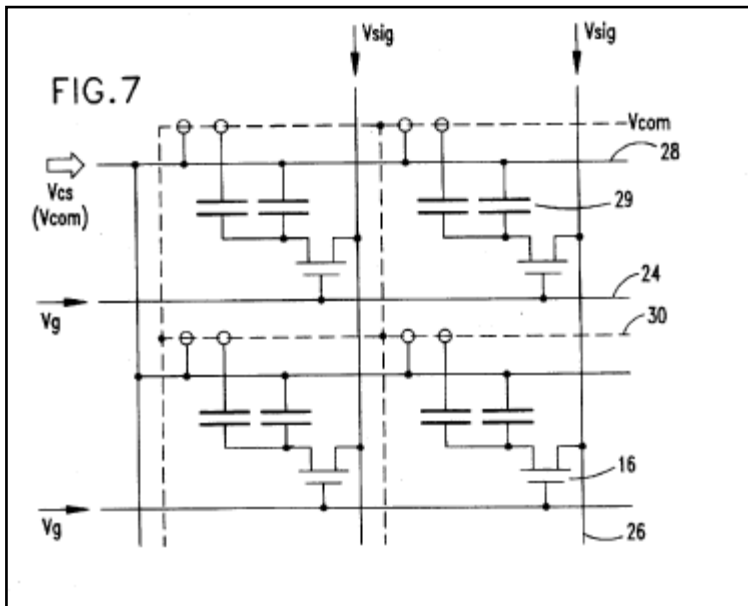
**INTRINSIC EVIDENCE FOR DISPUTED TERMS “STORAGE CAPACITANCE LINE” AND “STORAGE CAPACITANCE LINE FOR OUTPUTTING THE REFERENCE POTENTIAL OF THE STORAGE CAPACITANCE” (cont’d):**



Moreover, the present invention does not require a spherical spacer for specifying a cell gap or transfer for supplying a potential to the common electrode 30 as shown in FIG. 8. However, there is no problem in using the spacer and transfer. The equivalent circuit of the TFT-LCD of the present invention is shown in FIG. 7 for comparison with the circuit in FIG. 4. As shown in FIG. 7, the advantages are obtained that the problem of signal delay of Vcom is solved because Vcom is equal to Vcs everywhere in a screen by applying the present invention and it is unnecessary to independently supply Vcom from the outside.

7:32-42

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “STORAGE CAPACITANCE LINE” AND “STORAGE CAPACITANCE LINE FOR OUTPUTTING THE REFERENCE POTENTIAL OF THE STORAGE CAPACITANCE” (cont’d):**



Moreover, the present invention does not require a spherical spacer for specifying a cell gap or transfer for supplying a potential to the common electrode 30 as shown in FIG. 8. However, there is no problem in using the spacer and transfer. The equivalent circuit of the TFT-LCD of the present invention is shown in FIG. 7 for comparison with the circuit in FIG. 4. As shown in FIG. 7, the advantages are obtained that the problem of signal delay of Vcom is solved because Vcom is equal to Vcs everywhere in a screen by applying the present invention and it is unnecessary to independently supply Vcom from the outside.

7:32-42

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “STORAGE CAPACITANCE LINE” AND “STORAGE CAPACITANCE LINE FOR OUTPUTTING THE REFERENCE POTENTIAL OF THE STORAGE CAPACITANCE” (cont’d):**

As another method for connecting a common electrode with a storage capacitance line, the storage capacitance line 28 may be formed on the pixel electrode 10 formed on the array substrate 12 through the insulating film 74. In this case, a joint 80 between the storage capacitance line 28 and the common electrode 30 covering the pillar 78 of a color filter is three-dimensionally superimposed on a storage capacitance area 82.

In the case of the third embodiment, a layer 84 made of a conductive body such as a metal formed simultaneously with the data line 26 is first formed on the storage capacitance line 28, and then it is connected with the common electrode 30 to constitute the joint 80 instead of directly connecting the common electrode 30 to the storage capacitance line 28 like the first and second embodiments. Therefore, it is possible to perform fine adjustment for realizing an optically-optimized cell gap by the formation of the conductive body.

7:44-61

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “STORAGE CAPACITANCE LINE” AND “STORAGE CAPACITANCE LINE FOR OUTPUTTING THE REFERENCE POTENTIAL OF THE STORAGE CAPACITANCE” (cont’d):**

Then, the process for manufacturing the liquid crystal display panel 70 of this embodiment is described below.

First, the process for manufacturing the array substrate 12 is described below.

In the first process, the undercoat layer 42 is formed on the array substrate 12.

In the second process, the gate electrode 20, gate line 24, and storage capacitance line 28 are formed on the undercoat layer 42.

In the third process, the gate insulating film 44 is formed.

In the fourth process, the semiconductor layer 46 of the TFT 16 is formed.

In the fifth process, the pixel electrode 10 is formed.

In the sixth process, the hole 76 is formed on part of the gate insulating film 44 on the storage capacitance line 28.

In the seventh process, the source electrode 18 and drain electrode 22 of the TFT 16 and the data line 26 are formed.

In the eighth process, the passivation film 52 covering the TFT 16 is formed.

In the ninth process, the alignment film 54 is formed and treated through rubbing.

Then, the method for manufacturing the color filter substrate 72 is described below.

In the first process, the color filter 32 is formed on the facing substrate 14, and the pillar 78 of a color filter is formed at a position corresponding to the hole 76 on the array substrate 12.

In the second process, the common electrode 30 is formed on the color filter 32.

In the third process, the alignment film 54 is formed and treated through rubbing.

The array substrate 12 and the color filter substrate 77 finished through the above processes are made to face each other and the storage capacitance line 28 viewed through the hole 76 on the array substrate 12 is overlapped with the common electrode 30 at the portion covering the pillar 78 of a color filter on the facing substrate 14 to electrically connect them each other.

Then, the liquid crystal display panel 70 is finished by sealing the perimeter of the assembly with a sealant 64, injecting liquid crystal into the assembly through an injection hole (not illustrated), and closing the injection hole.

7:62-8:39

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “STORAGE CAPACITANCE LINE” AND “STORAGE CAPACITANCE LINE FOR OUTPUTTING THE REFERENCE POTENTIAL OF THE STORAGE CAPACITANCE” (cont’d):**

The present invention provides a large high-definition liquid crystal display without causing a signal delay even around the central portion of a common electrode. Moreover, because the present invention disuses processes for scattering spacers and dotting transfers, the yield is improved and the cost is decreased.

8:39-45

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “STORAGE CAPACITANCE LINE” AND “STORAGE CAPACITANCE LINE FOR OUTPUTTING THE REFERENCE POTENTIAL OF THE STORAGE CAPACITANCE” (cont’d):**

It is said to be unclear in Claims 1 and 5 which elements are “formed higher than other portions” and specify “a cell gap together with objects formed on the array substrate”. These elements are the pillars, which are now expressly identified. It is asked also which elements are electrically connected to the storage capacitance line. The answer is the portions of the common electrode covering at least some of the pillars. This has been clarified as well. The phrase “working on all pixels” is said to be not understood. This phrase merely refers to the fact that the common electrode is the common electrode for all of the pixels. This phrase has been deleted and the concept moved forward in Claims 1 and 5.

App. 08/615,012, 08/05/1997  
Amendment, pg. 6

**EXHIBIT \_\_\_\_\_**  
**U.S. PATENT NO. 5,748,266**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 1**

1. A color filter and common electrode carried by a facing substrate for assembly with an array substrate to form a liquid crystal display panel, the color filter comprising a plurality of pillars formed higher than other portions of the color filter for contact with **objects formed on the array substrate** to specify a cell gap, wherein the pillars are covered with the common electrode.

**ASSERTED CLAIM 3**

3. A liquid crystal display panel comprising:  
 an array substrate having pixel electrodes arranged like a matrix, an active element for each of the pixel electrodes, a storage capacitance provided at some of the pixel electrodes, and a storage capacitance line for outputting the reference potential of the storage capacitance;  
 a facing substrate having a plurality of pillars arranged so as to face the array substrate, the **pillars being formed higher than other portions of the facing substrate**, the pillars together with objects formed on the array substrate that face the pillars specifying a cell gap, and a common electrode for all pixels covering at least some of the pillars, the common electrode being electrically connected to the storage capacitance line at the portions of the common electrode covering the pillars; and  
 a liquid crystal layer held between the array substrate and the facing substrate.

**LGD's Claim Construction**

**objects formed on the array substrate<sup>1</sup>** - structures having one or more patterned layers in the pixel array

**pillars being formed higher than other portions of the facing substrate<sup>2</sup>** - patterned structures that protrude toward the pixel array beyond the height of non-pillar portions of the color filter substrate to act as a spacer

<sup>1</sup> Disputed Term "objects formed on the array substrate" also appears in asserted claim 7 in the same context.

<sup>2</sup> Disputed Term "pillars being formed higher than other portions of the facing substrate" also appears in asserted claim 7 in the same context.

**INTRINSIC EVIDENCE FOR DISPUTED TERM “OBJECTS  
FORMED ON THE ARRAY SUBSTRATE”:**

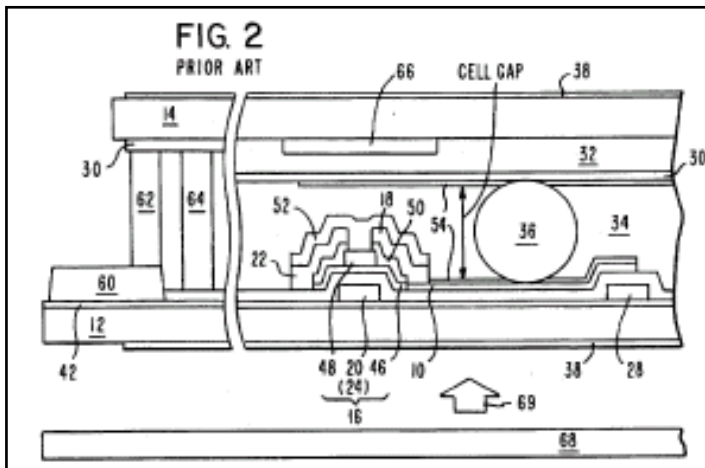
[57]

**ABSTRACT**

To prevent a signal delay of an active-matrix liquid crystal display from occurring in an active-matrix liquid crystal display having an active element for each pixel electrode, a potential is supplied to a common electrode from a storage capacitance line by forming a pillar of a color filter to specify a cell gap between an array substrate having the storage capacitance line and a facing substrate having the color filter and electrically connecting the common electrode covering the pillar of the color filter with the storage capacitance line on the array substrate. Thereby, it is possible to disuse a transfer dotting process which is a factor of decreasing the yield and also a factor of decreasing the effective display area. Moreover, because the potential is supplied to the common electrode from the storage capacitance line, it is possible to prevent a signal delay of the common electrode from occurring and moreover realize a high-image-quality screen even in a large and high-definition liquid crystal display without causing irregularity of a display screen or decrease of a contrast ratio. Furthermore, because it is possible to disuse a spacer scattering process and specify a cell gap by securing the pillar of the color filter, not only the cell gap is kept constant at any place and the uniformity of the screen is maintained but also spacers do not brighten or the screen is not blackened due to coagulation of the spacers and the image quality is improved. Furthermore, the cost can be decreased because the transfer dotting process and the spacer scattering process are unnecessary.

Abstract

**INTRINSIC EVIDENCE FOR DISPUTED TERM “OBJECTS FORMED ON THE ARRAY SUBSTRATE” (cont’d):**



substrate 14 and the common electrode 30 correspondingly to the pixel electrode 10 of the array substrate 12. Furthermore, a black matrix 66 is formed like a lattice. In the case of an existing liquid crystal display, transparent spherical spacers 36 are scattered in a liquid crystal layer 34 held by the array substrate 12 and the facing substrate 14 in order to keep a predetermined interval between the two substrates 12 and 14. Moreover, liquid crystal is sealed between the two substrates by a sealant 64. Furthermore, a polarizing film 38 is frequently set at the outer laterals of the array

2:11 –20

crystal display in order to keep the substrates 12 and 14 at a predetermined interval. However, under the spacers kept scattered, liquid crystal flows in a panel when an external force is applied to the panel, the spacers are moved in a cell plane due to the flowing of the liquid crystal, and thereby the spacers may scratch the surface of the thin alignment film 54 due to the movement of the spacers. Moreover, a cell gap (interval between electrodes of two substrates) may not be kept constant due to coagulation of the spacers. Unless the cell gap is kept constant, the optical path length difference (product of the birefringence rate and cell gap of the liquid crystal) of the liquid crystal layer changes and thereby, the contrast ratio and the chromaticity of a display screen are changed. Thus, problems occur that the uniformity of the screen cannot be kept or the display quality is deteriorated. Moreover, the spacers are brightened or coagulated, and the

4:3-18

**INTRINSIC EVIDENCE FOR DISPUTED TERM “OBJECTS FORMED ON THE ARRAY SUBSTRATE” (cont’d):**

spacers and thereby the screen is blackened by the degree of cut-off light. To solve these problems, various structures are already disclosed which disuse transparent spherical spacers and instead, specify a cell gap by a pillar formed on the array substrate 12 and/or the facing substrate 14 (official gazettes of Japanese Patent Laid-Open Nos. 164723/1985, 105583/1986, 24230/1989, 134733/1986, 163428/1902, 250416/1987, and 196946/1993). However, any one of these disclosures does not show means for solving the problem of signal delay in a TFT-LCD using the H/com inversion driving method.

4:20-30

Moreover, as shown in FIG. 2, the existing TFT-LCD has a problem in the structure of supplying the potential of the common electrode 30 on the facing substrate 14 from a plurality of portions at the perimeter of a pixel area of the array substrate 12 side to the common electrode 30 on the facing substrate 14 through the transfer 62 using conductive paste. Because this structure requires a high-accuracy alignment of the transfer 62, it uses two or more transfers to prevent defectives from being produced due to a deviation of a transfer. However, the manufacturing yield is decreased due to defectives produced in a process for dotting a transfer. Moreover, there is the restriction on design that an area for dotting a transfer must be formed at the perimeter of a pixel area. That is, because an area independent of display must exclusively be formed on the array substrate 12 and the facing substrate 14, an effective display area to a substrate size is decreased. However, it is inevitable to use the above structure because it is indispensable for an existing liquid crystal display in view of design.

4:31-49

**INTRINSIC EVIDENCE FOR DISPUTED TERM “OBJECTS FORMED ON THE ARRAY SUBSTRATE” (cont’d):**

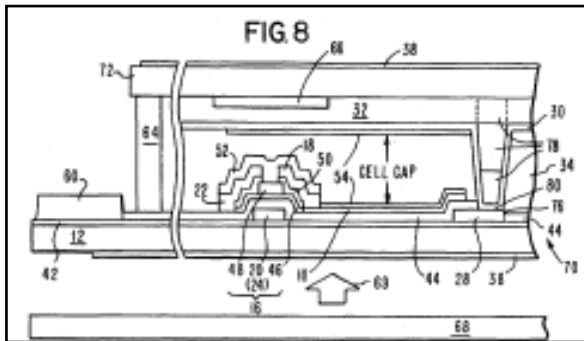
**SUMMARY OF THE INVENTION**

It is an object of the present invention to provide a TFT-LCD making it possible to prevent a signal delay from occurring even around the central portion of a common electrode and moreover prevent irregularity of a display screen and decrease of a contrast ration from occurring.

It is another object of the present invention to provide a TFT-LCD making it possible to keep a cell gap constant without using spacers.

It is still another object of the present invention to provide a TFT-LCD making it possible to supply a potential to a common electrode on a facing substrate without dotting a transfer.

4:53-64



common electrode on a facing substrate without dotting a transfer.

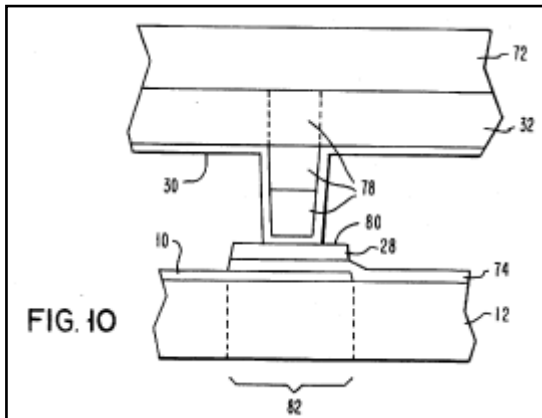
As shown in FIG. 8, the present invention uses a pillar 78 of a color filter 32 instead of a spacer in order to keep a cell gap between two substrates constant. Then, a signal delay of

a common electrode 30 is prevented from occurring by forming a portion for electrically connecting a common electrode 30 covering the pillar 78 of the color filter 32 with a storage capacitance line 28 everywhere in a pixel area and supplying a potential of the common electrode 30 from the storage capacitance line 28.

According to the present invention, the potential of the storage capacitance line 28 is supplied to the common

4:63 – 5:8

**INTRINSIC EVIDENCE FOR DISPUTED TERM “OBJECTS FORMED ON THE ARRAY SUBSTRATE” (cont’d):**



common electrode on a facing substrate without dotting a transfer.

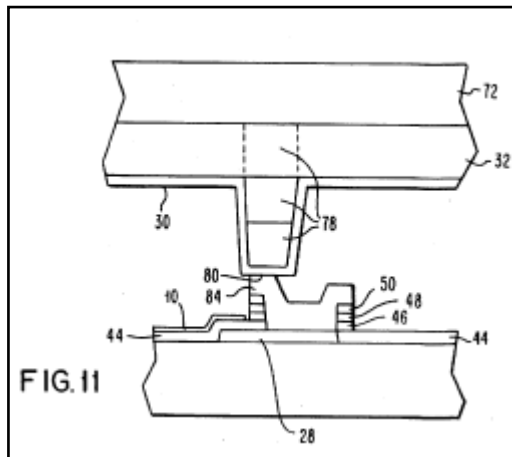
As shown in FIG. 8, the present invention uses a pillar 78 of a color filter 32 instead of a spacer in order to keep a cell gap between two substrates constant. Then, a signal delay of

a common electrode 30 is prevented from occurring by forming a portion for electrically connecting a common electrode 30 covering the pillar 78 of the color filter 32 with a storage capacitance line 28 everywhere in a pixel area and supplying a potential of the common electrode 30 from the storage capacitance line 28.

According to the present invention, the potential of the storage capacitance line 28 is supplied to the common

4:63 – 5:8

**INTRINSIC EVIDENCE FOR DISPUTED TERM “OBJECTS FORMED ON THE ARRAY SUBSTRATE” (cont’d):**



common electrode on a facing substrate without dotting a transfer.

As shown in FIG. 8, the present invention uses a pillar 78 of a color filter 32 instead of a spacer in order to keep a cell gap between two substrates constant. Then, a signal delay of

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a common electrode 30 is prevented from occurring by forming a portion for electrically connecting a common electrode 30 covering the pillar 78 of the color filter 32 with a storage capacitance line 28 everywhere in a pixel area and supplying a potential of the common electrode 30 from the storage capacitance line 28.

According to the present invention, the potential of the storage capacitance line 28 is supplied to the common

4:63 – 5:8

**INTRINSIC EVIDENCE FOR DISPUTED TERM “OBJECTS  
FORMED ON THE ARRAY SUBSTRATE” (cont’d):**

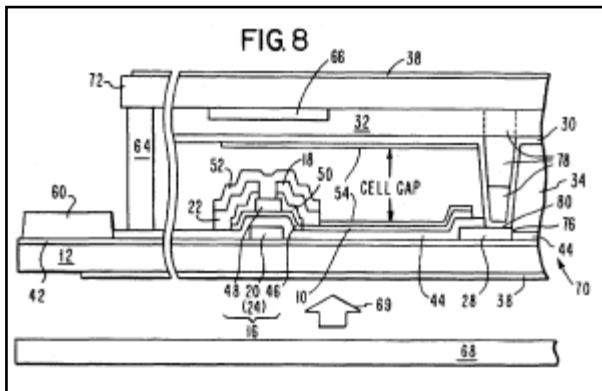
According to the present invention, the potential of the storage capacitance line 28 is supplied to the common electrode 30 on a facing substrate from joints formed everywhere in a pixel area. Originally, the common-electrode potential (Vcom) is frequently equalized with the

5:7-10

A pillar of a color filter on a facing substrate requires only change of mask patterns for the color filter but the number of processes does not increase. Moreover, it is possible to form a pillar by laminating red, green, and blue color filters or any two color filters of them. Furthermore, any sequence of colors to be laminated is not determined for a color-filter laminating portion. Furthermore, it is possible to fine-adjust a cell gap by forming a laminate structure containing a plurality of conductive materials at a position on an array substrate where a pillar is fitted on a facing substrate, connecting the laminate structure to a common electrode on the facing substrate through a conductive body layer electrically connected to a storage capacitance line, and specifying the cell gap by the sum of the height of the laminate structure on the array substrate and that of the pillar on the facing substrate.

5:57-6:5

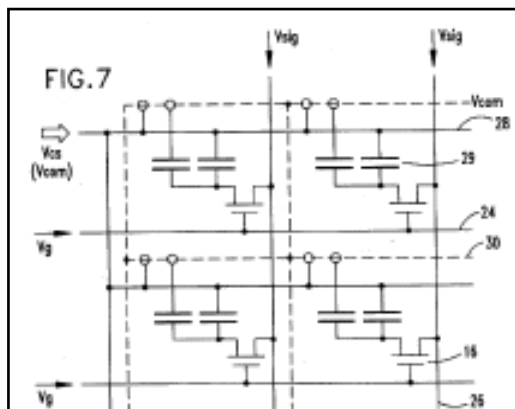
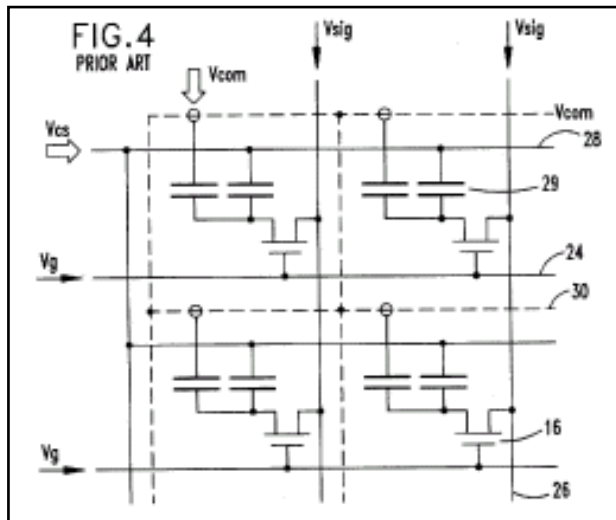
**INTRINSIC EVIDENCE FOR DISPUTED TERM “OBJECTS FORMED ON THE ARRAY SUBSTRATE” (cont’d):**



formed on the storage capacitance line 28 in a pixel area on the array substrate 12. That is, the embodiment 1 has a structure in which a hole 76 is formed at part of the gate insulating film 44 on the storage capacitance line 28, the common electrode 30 at a portion covering the pillar 78 of a color filter formed on the color filter substrate 72 is overlapped with the position of the hole 76, and the common electrode 30 contacts the storage capacitance line 28 so that they are electrically connected each other. Though the storage capacitance line 28 contacts the common electrode

7:6-15

**INTRINSIC EVIDENCE FOR DISPUTED TERM “OBJECTS FORMED ON THE ARRAY SUBSTRATE” (cont’d):**



However, there is no problem in using the spacer and transfer. The equivalent circuit of the TFT-LCD of the present invention is shown in FIG. 7 for comparison with the circuit in FIG. 4. As shown in FIG. 7, the advantages are obtained that the problem of signal delay of Vcom is solved

7:36-39

**INTRINSIC EVIDENCE FOR DISPUTED TERM “OBJECTS  
FORMED ON THE ARRAY SUBSTRATE” (cont’d):**

independently supply Vcom from the outside.

As another method for connecting a common electrode with a storage capacitance line, the storage capacitance line 28 may be formed on the pixel electrode 10 formed on the array substrate 12 through the insulating film 74. In this case, a joint 80 between the storage capacitance line 28 and the

4:42-47

**INTRINSIC EVIDENCE FOR DISPUTED TERM “OBJECTS FORMED ON THE ARRAY SUBSTRATE” (cont’d):**

Then, the process for manufacturing the liquid crystal display panel 70 of this embodiment is described below.

First, the process for manufacturing the array substrate 12 is described below.

In the first process, the undercoat layer 42 is formed on the array substrate 12.

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In the second process, the gate electrode 20, gate line 24, and storage capacitance line 28 are formed on the undercoat layer 42.

In the third process, the gate insulating film 44 is formed.

In the fourth process, the semiconductor layer 46 of the TFT 16 is formed.

In the fifth process, the pixel electrode 10 is formed.

In the sixth process, the hole 76 is formed on part of the gate insulating film 44 on the storage capacitance line 28.

In the seventh process, the source electrode 18 and drain electrode 22 of the TFT 16 and the data line 26 are formed.

In the eighth process, the passivation film 52 covering the TFT 16 is formed.

In the ninth process, the alignment film 54 is formed and treated through rubbing.

Then, the method for manufacturing the color filter substrate 72 is described below.

In the first process, the color filter 32 is formed on the facing substrate 14, and the pillar 78 of a color filter is formed at a position corresponding to the hole 76 on the array substrate 12.

In the second process, the common electrode 30 is formed on the color filter 32.

In the third process, the alignment film 54 is formed and treated through rubbing.

The array substrate 12 and the color filter substrate 77 finished through the above processes are made to face each other and the storage capacitance line 28 viewed through the hole 76 on the array substrate 12 is overlapped with the common electrode 30 at the portion covering the pillar 78 of a color filter on the facing substrate 14 to electrically connect them each other.

Then, the liquid crystal display panel 70 is finished by sealing the perimeter of the assembly with a sealant 64, injecting liquid crystal into the assembly through an injection hole (not illustrated), and closing the injection hole.

7:62-8:39

**INTRINSIC EVIDENCE FOR DISPUTED TERM “OBJECTS  
FORMED ON THE ARRAY SUBSTRATE” (cont’d):**

The present invention provides a large high-definition liquid crystal display without causing a signal delay even around the central portion of a common electrode. Moreover, because the present invention disuses processes for scattering spacers and dotting transfers, the yield is improved and the cost is decreased.

8:40-45

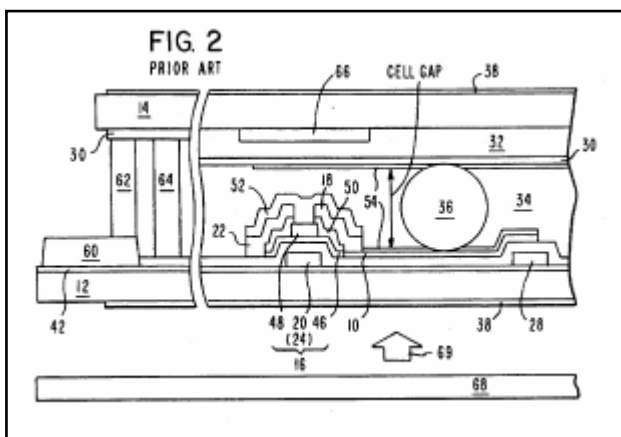
**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”:**

To prevent a signal delay of an active-matrix liquid crystal display from occurring in an active-matrix liquid crystal display having an active element for each pixel electrode, a potential is supplied to a common electrode from a storage capacitance line by forming a pillar of a color filter to specify a cell gap between an array substrate having the storage capacitance line and a facing substrate having the color filter and electrically connecting the common electrode covering the pillar of the color filter with the storage capacitance line on the array substrate. Thereby, it is possible to disuse a transfer dotting process which is a factor of decreasing the yield and also a factor of decreasing the effective display area. Moreover, because the potential is supplied to the common electrode from the storage capacitance line, it is possible to prevent a signal delay of the common electrode from occurring and moreover realize a high-image-quality screen even in a large and high-definition liquid crystal display without causing irregularity of a display screen or decrease of a contrast ratio.

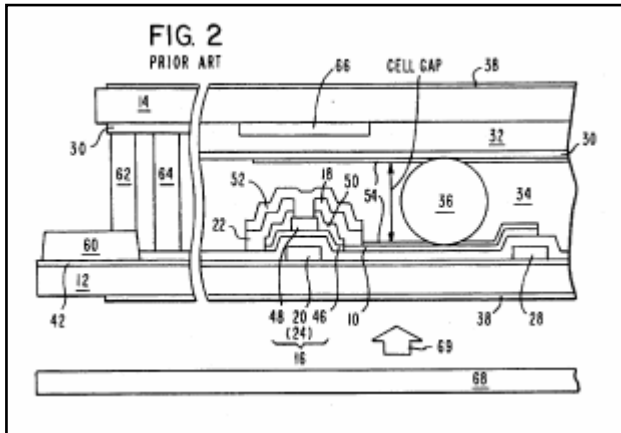
Abstract

Furthermore, because it is possible to disuse a spacer scattering process and specify a cell gap by securing the pillar of the color filter, not only the cell gap is kept constant at any place and the uniformity of the screen is maintained but also spacers do not brighten or the screen is not blackened due to coagulation of the spacers and the image quality is improved. Furthermore, the cost can be decreased because the transfer dotting process and the spacer scattering process are unnecessary.

Abstract



**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED  
HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”  
(cont’d):**



Furthermore, a black matrix 66 is formed like a lattice. In the case of an existing liquid crystal display, transparent spherical spacers 36 are scattered in a liquid crystal layer 34 held by the array substrate 12 and the facing substrate 14 in order to keep a predetermined interval between the two substrates 12 and 14. Moreover, liquid crystal is sealed between the two substrates by a sealant 64. Furthermore, a polarizing

2:13-19

**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**

**(cont’d):**

Moreover, as shown in FIG. 2, the transparent spherical spacers 36 (made of plastic and glass fiber) are hitherto

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scattered in the liquid crystal layer 34 held by the array substrate 12 and the facing substrate 14 constituting a liquid crystal display in order to keep the substrates 12 and 14 at a predetermined interval. However, under the spacers kept scattered, liquid crystal flows in a panel when an external force is applied to the panel, the spacers are moved in a cell plane due to the flowing of the liquid crystal, and thereby the spacers may scratch the surface of the thin alignment film 54 due to the movement of the spacers. Moreover, a cell gap (interval between electrodes of two substrates) may not be kept constant due to coagulation of the spacers. Unless the cell gap is kept constant, the optical path length difference (product of the birefringence rate and cell gap of the liquid crystal) of the liquid crystal layer changes and thereby, the contrast ratio and the chromaticity of a display screen are changed. Thus, problems occur that the uniformity of the screen cannot be kept or the display quality is deteriorated. Moreover, the spacers are brightened or coagulated, and the light from the backlight 68 is cut off by the coagulated spacers and thereby the screen is blackened by the degree of cut-off light. To solve these problems, various structures are

3:66 – 4:21

Moreover, the spacers are brightened or coagulated, and the light from the backlight 68 is cut off by the coagulated spacers and thereby the screen is blackened by the degree of cut-off light. To solve these problems, various structures are already disclosed which disuse transparent spherical spacers and instead, specify a cell gap by a pillar formed on the array substrate 12 and/or the facing substrate 14 (official gazettes of Japanese Patent Laid-Open Nos. 164723/1985, 105583/1986, 24230/1989, 134733/1986, 163428/1902, 250416/1987, and 196946/1993). However, any one of these disclosures does not show means for solving the problem of signal delay in a TFT-LCD using the H/com inversion driving method.

4:21-30

**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**  
**(cont’d):**

Moreover, as shown in FIG. 2, the existing TFT-LCD has a problem in the structure of supplying the potential of the common electrode 30 on the facing substrate 14 from a plurality of portions at the perimeter of a pixel area of the array substrate 12 side to the common electrode 30 on the facing substrate 14 through the transfer 62 using conductive paste. Because this structure requires a high-accuracy alignment of the transfer 62, it uses two or more transfers to prevent defectives from being produced due to a deviation of a transfer. However, the manufacturing yield is decreased due to defectives produced in a process for dotting a transfer. Moreover, there is the restriction on design that an area for dotting a transfer must be formed at the perimeter of a pixel area. That is, because an area independent of display must exclusively be formed on the array substrate 12 and the facing substrate 14, an effective display area to a substrate size is decreased. However, it is inevitable to use the above structure because it is indispensable for an existing liquid crystal display in view of design.

4:31-49

**SUMMARY OF THE INVENTION**

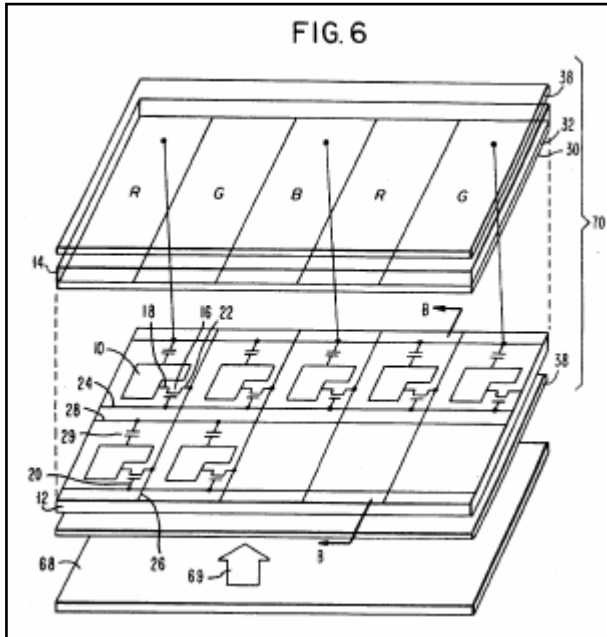
It is an object of the present invention to provide a TFT-LCD making it possible to prevent a signal delay from occurring even around the central portion of a common electrode and moreover prevent irregularity of a display screen and decrease of a contrast ration from occurring.

It is another object of the present invention to provide a TFT-LCD making it possible to keep a cell gap constant without using spacers.

It is still another object of the present invention to provide a TFT-LCD making it possible to supply a potential to a common electrode on a facing substrate without dotting a transfer.

4:51-64

**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**  
**(cont’d):**



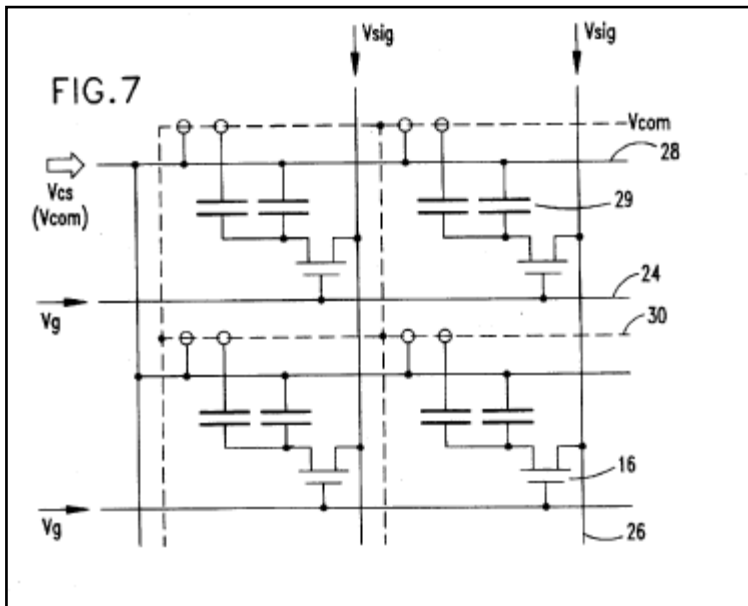
As shown in FIG. 8, the present invention uses a pillar 78 of a color filter 32 instead of a spacer in order to keep a cell gap between two substrates constant. Then, a signal delay of

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a common electrode 30 is prevented from occurring by forming a portion for electrically connecting a common electrode 30 covering the pillar 78 of the color filter 32 with a storage capacitance line 28 everywhere in a pixel area and supplying a potential of the common electrode 30 from the storage capacitance line 28.

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**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**  
**(cont’d):**



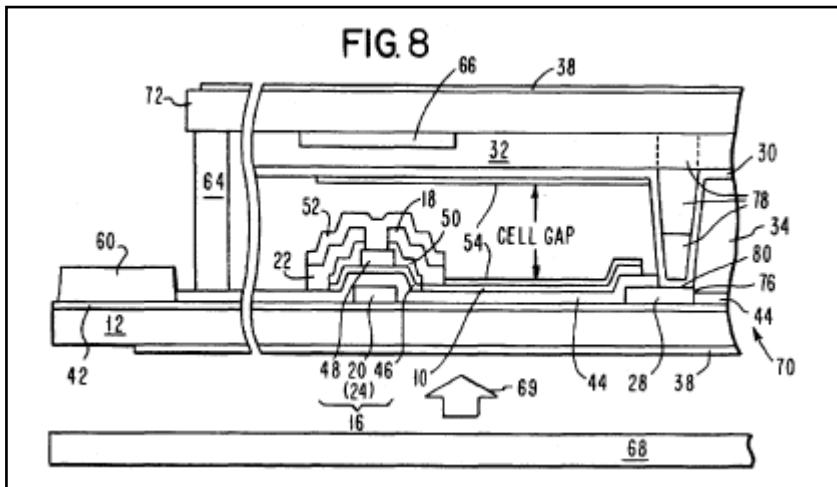
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**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**  
**(cont’d):**



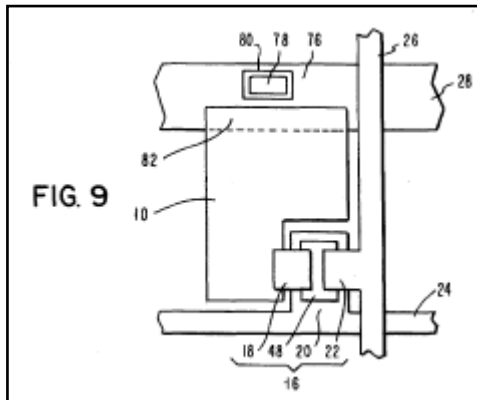
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**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**  
**(cont’d):**



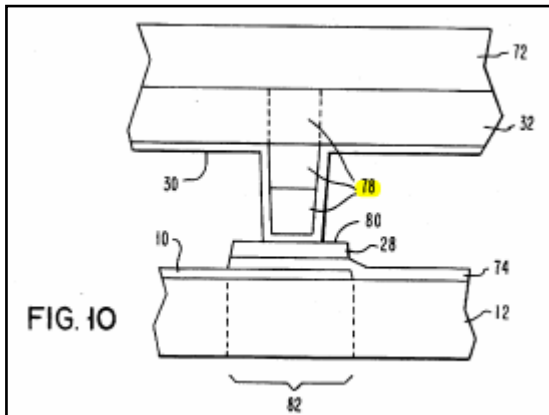
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4:65-5:6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**  
**(cont’d):**



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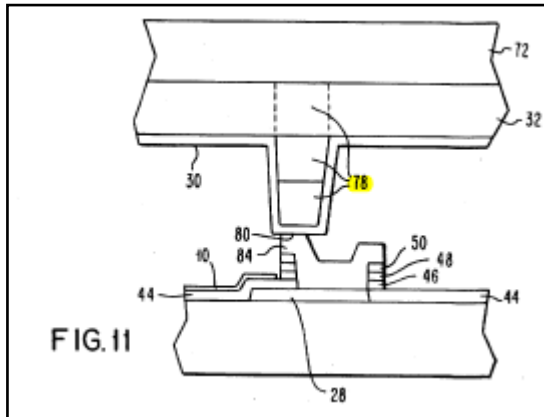
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4:65-5:6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**

**(cont'd):**



As shown in FIG. 8, the present invention uses a pillar 78 of a color filter 32 instead of a spacer in order to keep a cell gap between two substrates constant. Then, a signal delay of

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4:65-5:6

According to the present invention, the potential of the storage capacitance line 28 is supplied to the common electrode 30 on a facing substrate from joints formed everywhere in a pixel area. Originally, the common-

5:7-10

**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED  
HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”  
(cont’d):**

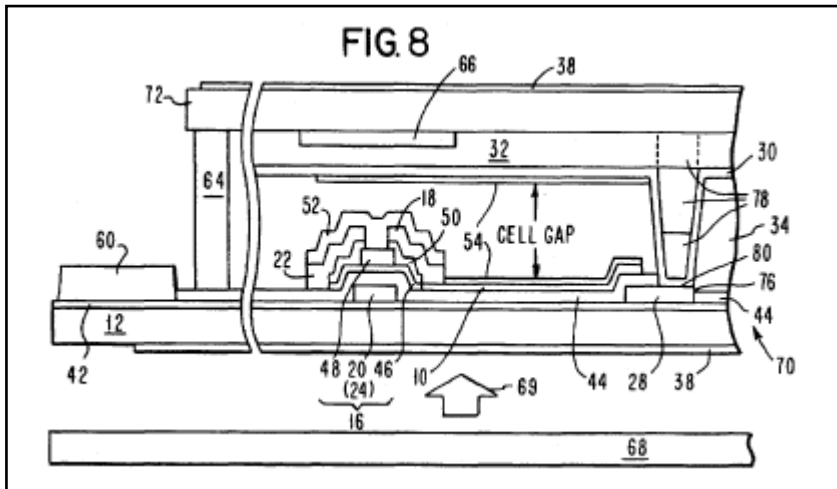
A pillar of a color filter on a facing substrate requires only change of mask patterns for the color filter but the number of processes does not increase. Moreover, it is possible to form a pillar by laminating red, green, and blue color filters or any two color filters of them. Furthermore, any sequence of colors to be laminated is not determined for a color-filter laminating portion. Furthermore, it is possible to fine-adjust a cell gap by forming a laminate structure containing a plurality of conductive materials at a position on an array substrate where a pillar is fitted on a facing substrate, connecting the laminate structure to a common electrode on

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the facing substrate through a conductive body layer electrically connected to a storage capacitance line, and specifying the cell gap by the sum of the height of the laminate structure on the array substrate and that of the pillar on the facing substrate.

5:57-6:5

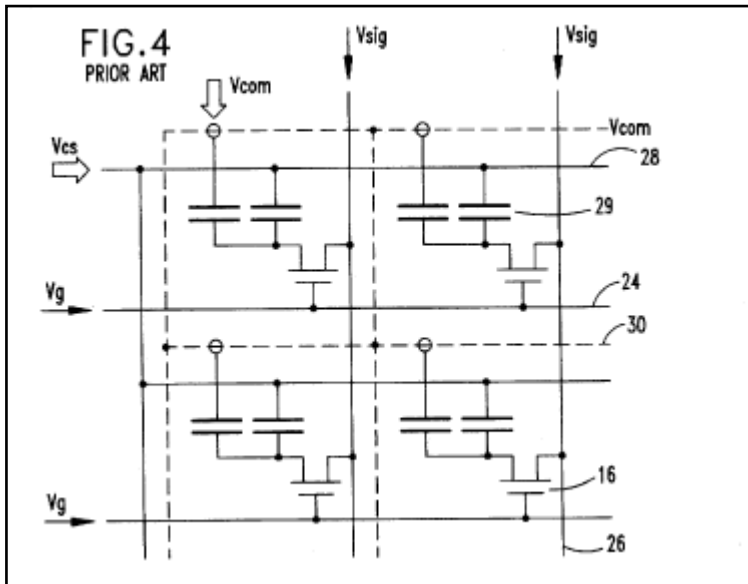
**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**  
**(cont’d):**



Furthermore, as shown in FIG. 8, the embodiment 1 may have a structure in which the gate insulating film 44 is formed on the storage capacitance line 28 in a pixel area on the array substrate 12. That is, the embodiment 1 has a structure in which a hole 76 is formed at part of the gate insulating film 44 on the storage capacitance line 28, the common electrode 30 at a portion covering the pillar 78 of a color filter formed on the color filter substrate 72 is overlapped with the position of the hole 76, and the common electrode 30 contacts the storage capacitance line 28 so that they are electrically connected each other. Though the

7:4-13

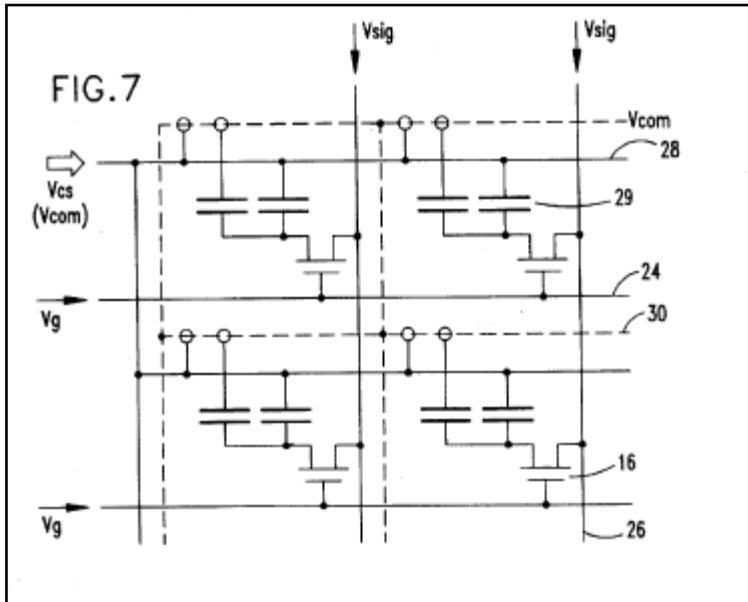
**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**  
**(cont’d):**



Moreover, the present invention does not require a spherical spacer for specifying a cell gap or transfer for supplying a potential to the common electrode 30 as shown in FIG. 8. However, there is no problem in using the spacer and transfer. The equivalent circuit of the TFT-LCD of the present invention is shown in FIG. 7 for comparison with the circuit in FIG. 4. As shown in FIG. 7, the advantages are obtained that the problem of signal delay of Vcom is solved because Vcom is equal to Vcs everywhere in a screen by applying the present invention and it is unnecessary to independently supply Vcom from the outside.

7:32-42

**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**  
**(cont’d):**



Moreover, the present invention does not require a spherical spacer for specifying a cell gap or transfer for supplying a potential to the common electrode 30 as shown in FIG. 8. However, there is no problem in using the spacer and transfer. The equivalent circuit of the TFT-LCD of the present invention is shown in FIG. 7 for comparison with the circuit in FIG. 4. As shown in FIG. 7, the advantages are obtained that the problem of signal delay of Vcom is solved because Vcom is equal to Vcs everywhere in a screen by applying the present invention and it is unnecessary to independently supply Vcom from the outside.

7:32-42

**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED  
HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”  
(cont’d):**

As another method for connecting a common electrode with a storage capacitance line, the storage capacitance line 28 may be formed on the pixel electrode 10 formed on the array substrate 12 through the insulating film 74. In this case, a joint 80 between the storage capacitance line 28 and the common electrode 30 covering the pillar 78 of a color filter is three-dimensionally superimposed on a storage capacitance area 82.

In the case of the third embodiment, a layer 84 made of a conductive body such as a metal formed simultaneously with the data line 26 is first formed on the storage capacitance line 28, and then it is connected with the common electrode 30 to constitute the joint 80 instead of directly connecting the common electrode 30 to the storage capacitance line 28 like the first and second embodiments. Therefore, it is possible to perform fine adjustment for realizing an optically-optimized cell gap by the formation of the conductive body.

7:44-61

**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER” (cont’d):**

Then, the process for manufacturing the liquid crystal display panel **70** of this embodiment is described below.

First, the process for manufacturing the array substrate **12** is described below.

In the first process, the undercoat layer **42** is formed on the array substrate **12**.

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In the second process, the gate electrode **20**, gate line **24**, and storage capacitance line **28** are formed on the undercoat layer **42**.

In the third process, the gate insulating film **44** is formed.

In the fourth process, the semiconductor layer **46** of the TFT **16** is formed.

In the fifth process, the pixel electrode **10** is formed.

In the sixth process, the hole **76** is formed on part of the gate insulating film **44** on the storage capacitance line **28**.

In the seventh process, the source electrode **18** and drain electrode **22** of the TFT **16** and the data line **26** are formed.

In the eighth process, the passivation film **52** covering the TFT **16** is formed.

In the ninth process, the alignment film **54** is formed and treated through rubbing.

Then, the method for manufacturing the color filter substrate **72** is described below.

In the first process, the color filter **32** is formed on the facing substrate **14**, and the pillar **78** of a color filter is formed at a position corresponding to the hole **76** on the array substrate **12**.

In the second process, the common electrode **30** is formed on the color filter **32**.

In the third process, the alignment film **54** is formed and treated through rubbing.

The array substrate **12** and the color filter substrate **77** finished through the above processes are made to face each other and the storage capacitance line **28** viewed through the hole **76** on the array substrate **12** is overlapped with the common electrode **30** at the portion covering the pillar **78** of a color filter on the facing substrate **14** to electrically connect them each other.

Then, the liquid crystal display panel **70** is finished by sealing the perimeter of the assembly with a sealant **64**, injecting liquid crystal into the assembly through an injection hole (not illustrated), and closing the injection hole.

7:62-8:39

**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED  
HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”  
(cont’d):**

The present invention provides a large high-definition liquid crystal display without causing a signal delay even around the central portion of a common electrode. Moreover, because the present invention disuses processes for scattering spacers and dotting transfers, the yield is improved and the cost is decreased.

8:39-45

**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED  
HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”  
(cont’d):**

It is said to be unclear in Claims 1 and 5 which elements are “formed higher than other portions” and specify “a cell gap together with objects formed on the array substrate”. These elements are the pillars, which are now expressly identified. It is asked also which elements are electrically connected to the storage capacitance line. The answer is the portions of the common electrode covering at least some of the pillars. This has been clarified as well. The phrase “working on all pixels” is said to be not understood. This phrase merely refers to the fact that the common electrode is the common electrode for all of the pixels. This phrase has been deleted and the concept moved forward in Claims 1 and 5.

App. 08/615,012, 08/05/1997  
Amendment, pg. 6

**EXHIBIT \_\_\_\_\_**  
**U.S. PATENT NO. 5,748,266**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 9**

**9. A liquid crystal display panel manufacturing method comprising the steps of:**

**determining the height of a laminate structure and storage capacitance line to be formed on an array substrate, the laminate structure including a plurality of conductive materials electrically connected with the storage capacitance line, and determining the height of pillars of a color filter to be formed on a color filter substrate so that the sum of these heights specifies the distance between the array substrate and the color filter substrate;**

**forming the storage capacitance line on the array substrate and the laminate structure on the storage capacitance line, the array substrate having pixel electrodes arranged like a matrix and active elements arranged in the vicinity of the pixel electrodes, so that the storage capacitance line and the laminate structure have the determined height thereof;**

**forming the color filter at positions corresponding to the pixel electrodes on the color filter substrate and also forming pillars of the color filter so that the pillars have the determined height thereof;**

**superimposing the array substrate and the color filter substrate so that the laminate structure and the pillars of the color filter butt each other and sealing the circumferences of the superimposed array substrate and color filter substrate; and**

**injecting liquid crystal between the array substrate and the color filter substrate whose circumferences are sealed.**

**LGD's Claim Construction**

**pillars of a color filter -**  
patterned structures that protrude toward the pixel array, to act as a spacer, and are made of color filter material

**injecting liquid crystal between the array substrate and the color filter substrate**  
- providing liquid crystal through an injection hole between the sealed array and color filter substrates

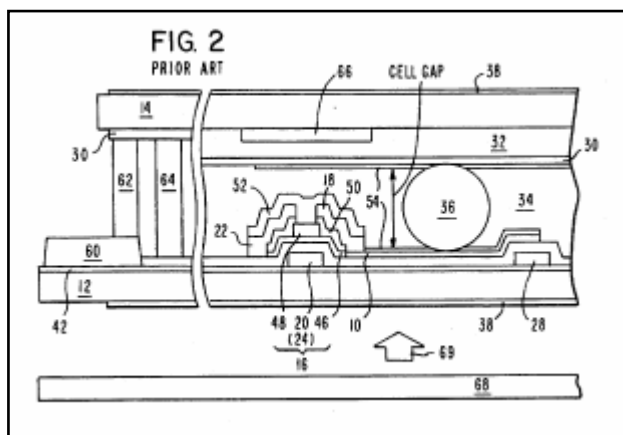
**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”:**

To prevent a signal delay of an active-matrix liquid crystal display from occurring in an active-matrix liquid crystal display having an active element for each pixel electrode, a potential is supplied to a common electrode from a storage capacitance line by forming a pillar of a color filter to specify a cell gap between an array substrate having the storage capacitance line and a facing substrate having the color filter and electrically connecting the common electrode covering the pillar of the color filter with the storage capacitance line on the array substrate. Thereby, it is possible to disuse a transfer dotting process which is a factor of decreasing the yield and also a factor of decreasing the effective display area. Moreover, because the potential is supplied to the common electrode from the storage capacitance line, it is possible to prevent a signal delay of the common electrode from occurring and moreover realize a high-image-quality screen even in a large and high-definition liquid crystal display without causing irregularity of a display screen or decrease of a contrast ratio.

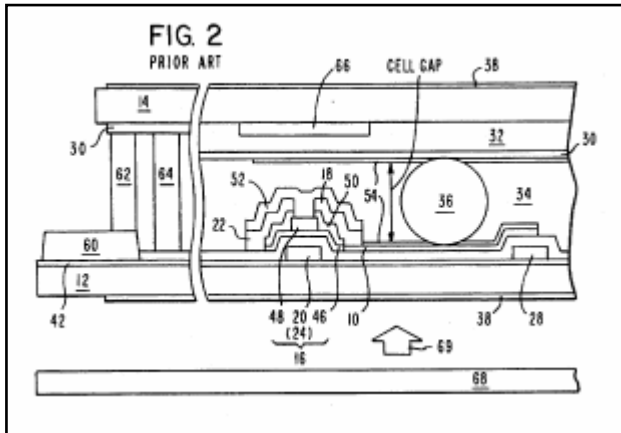
Abstract

Furthermore, because it is possible to disuse a spacer scattering process and specify a cell gap by securing the pillar of the color filter, not only the cell gap is kept constant at any place and the uniformity of the screen is maintained but also spacers do not brighten or the screen is not blackened due to coagulation of the spacers and the image quality is improved. Furthermore, the cost can be decreased because the transfer dotting process and the spacer scattering process are unnecessary.

Abstract



**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**  
**(cont’d):**



Furthermore, a black matrix 66 is formed like a lattice. In the case of an existing liquid crystal display, transparent spherical spacers 36 are scattered in a liquid crystal layer 34 held by the array substrate 12 and the facing substrate 14 in order to keep a predetermined interval between the two substrates 12 and 14. Moreover, liquid crystal is sealed between the two substrates by a sealant 64. Furthermore, a polarizing

2:13-19

**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**

**(cont’d):**

Moreover, as shown in FIG. 2, the transparent spherical spacers 36 (made of plastic and glass fiber) are hitherto

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scattered in the liquid crystal layer 34 held by the array substrate 12 and the facing substrate 14 constituting a liquid crystal display in order to keep the substrates 12 and 14 at a predetermined interval. However, under the spacers kept scattered, liquid crystal flows in a panel when an external force is applied to the panel, the spacers are moved in a cell plane due to the flowing of the liquid crystal, and thereby the spacers may scratch the surface of the thin alignment film 54 due to the movement of the spacers. Moreover, a cell gap (interval between electrodes of two substrates) may not be kept constant due to coagulation of the spacers. Unless the cell gap is kept constant, the optical path length difference (product of the birefringence rate and cell gap of the liquid crystal) of the liquid crystal layer changes and thereby, the contrast ratio and the chromaticity of a display screen are changed. Thus, problems occur that the uniformity of the screen cannot be kept or the display quality is deteriorated. Moreover, the spacers are brightened or coagulated, and the light from the backlight 68 is cut off by the coagulated spacers and thereby the screen is blackened by the degree of cut-off light. To solve these problems, various structures are

3:66 – 4:21

Moreover, the spacers are brightened or coagulated, and the light from the backlight 68 is cut off by the coagulated spacers and thereby the screen is blackened by the degree of cut-off light. To solve these problems, various structures are already disclosed which disuse transparent spherical spacers and instead, specify a cell gap by a pillar formed on the array substrate 12 and/or the facing substrate 14 (official gazettes of Japanese Patent Laid-Open Nos. 164723/1985, 105583/1986, 24230/1989, 134733/1986, 163428/1902, 250416/1987, and 196946/1993). However, any one of these disclosures does not show means for solving the problem of signal delay in a TFT-LCD using the H/com inversion driving method.

4:21-30

**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**  
**(cont’d):**

Moreover, as shown in FIG. 2, the existing TFT-LCD has a problem in the structure of supplying the potential of the common electrode 30 on the facing substrate 14 from a plurality of portions at the perimeter of a pixel area of the array substrate 12 side to the common electrode 30 on the facing substrate 14 through the transfer 62 using conductive paste. Because this structure requires a high-accuracy alignment of the transfer 62, it uses two or more transfers to prevent defectives from being produced due to a deviation of a transfer. However, the manufacturing yield is decreased due to defectives produced in a process for dotting a transfer. Moreover, there is the restriction on design that an area for dotting a transfer must be formed at the perimeter of a pixel area. That is, because an area independent of display must exclusively be formed on the array substrate 12 and the facing substrate 14, an effective display area to a substrate size is decreased. However, it is inevitable to use the above structure because it is indispensable for an existing liquid crystal display in view of design.

4:31-49

**SUMMARY OF THE INVENTION**

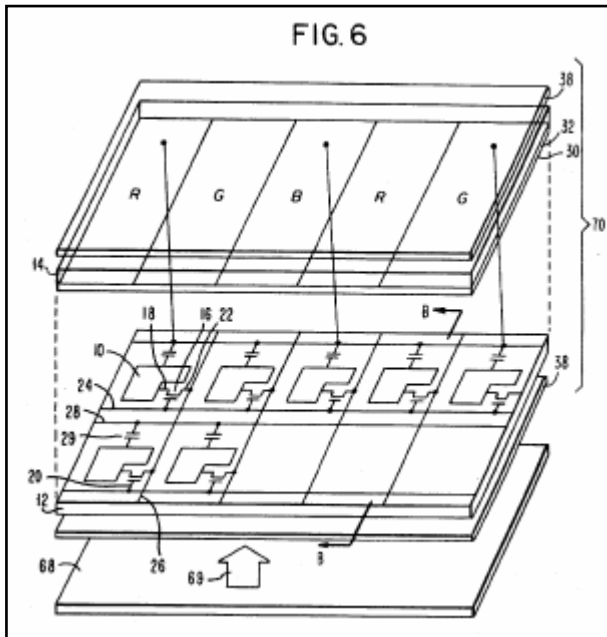
It is an object of the present invention to provide a TFT-LCD making it possible to prevent a signal delay from occurring even around the central portion of a common electrode and moreover prevent irregularity of a display screen and decrease of a contrast ration from occurring.

It is another object of the present invention to provide a TFT-LCD making it possible to keep a cell gap constant without using spacers.

It is still another object of the present invention to provide a TFT-LCD making it possible to supply a potential to a common electrode on a facing substrate without dotting a transfer.

4:51-64

**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED  
HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”  
(cont’d):**



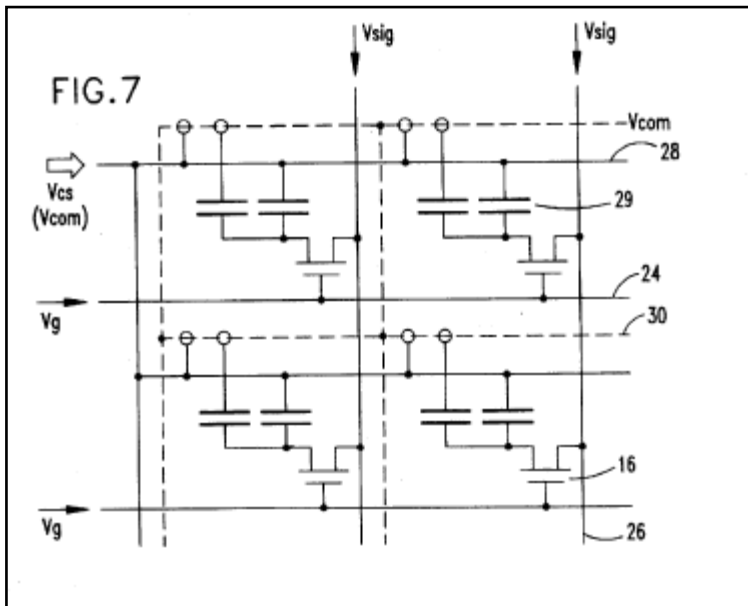
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**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**  
**(cont’d):**



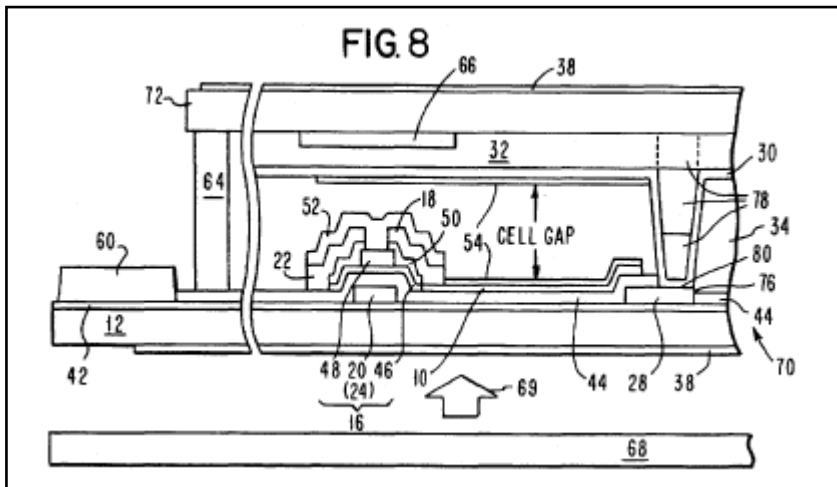
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**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**  
**(cont’d):**



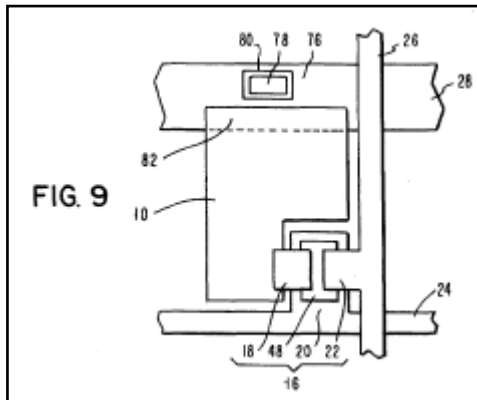
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**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**  
**(cont’d):**



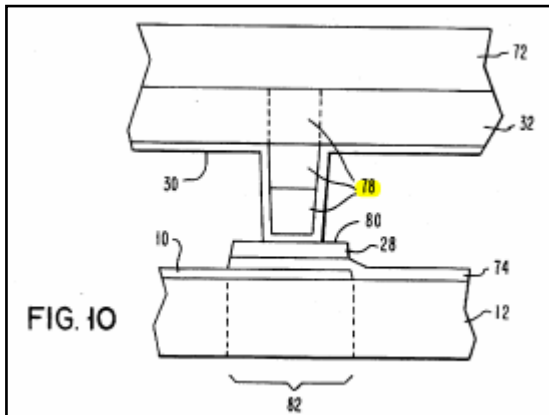
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**(cont’d):**



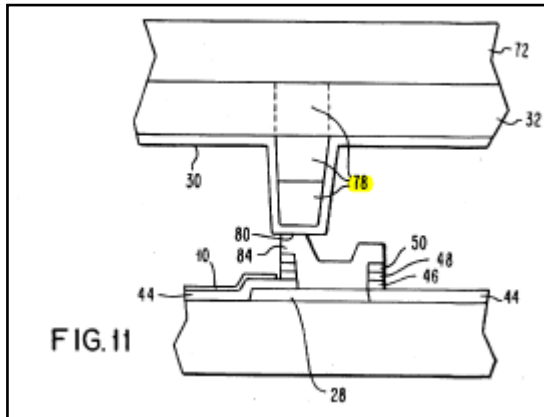
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**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**  
**(cont’d):**



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4:65-5:6

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5:7-10

**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED  
HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”  
(cont’d):**

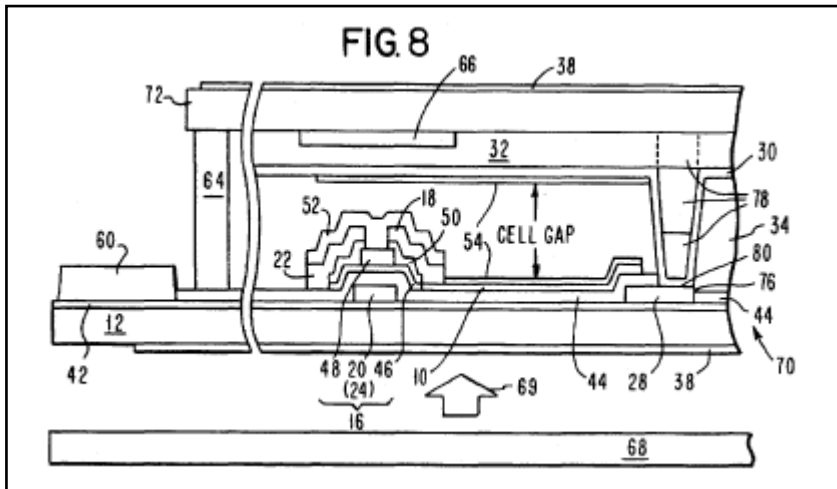
A pillar of a color filter on a facing substrate requires only change of mask patterns for the color filter but the number of processes does not increase. Moreover, it is possible to form a pillar by laminating red, green, and blue color filters or any two color filters of them. Furthermore, any sequence of colors to be laminated is not determined for a color-filter laminating portion. Furthermore, it is possible to fine-adjust a cell gap by forming a laminate structure containing a plurality of conductive materials at a position on an array substrate where a pillar is fitted on a facing substrate, connecting the laminate structure to a common electrode on

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the facing substrate through a conductive body layer electrically connected to a storage capacitance line, and specifying the cell gap by the sum of the height of the laminate structure on the array substrate and that of the pillar on the facing substrate.

5:57-6:5

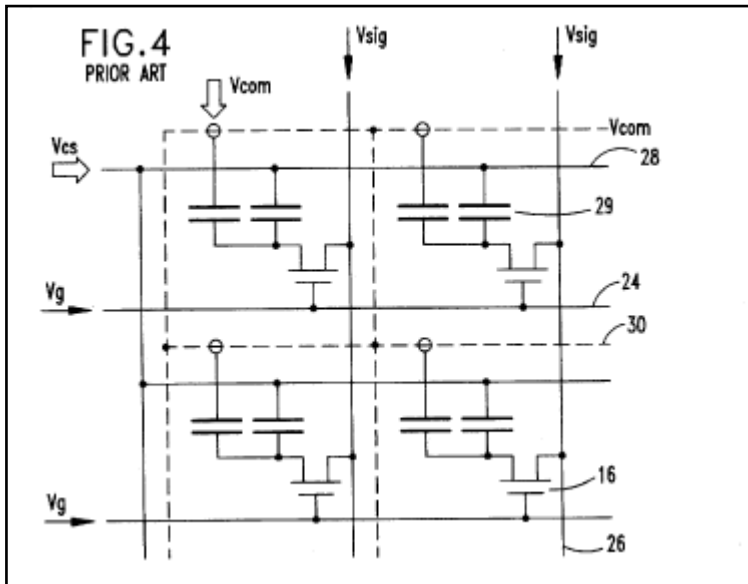
**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**  
**(cont’d):**



Furthermore, as shown in FIG. 8, the embodiment 1 may have a structure in which the gate insulating film 44 is formed on the storage capacitance line 28 in a pixel area on the array substrate 12. That is, the embodiment 1 has a structure in which a hole 76 is formed at part of the gate insulating film 44 on the storage capacitance line 28, the common electrode 30 at a portion covering the pillar 78 of a color filter formed on the color filter substrate 72 is overlapped with the position of the hole 76, and the common electrode 30 contacts the storage capacitance line 28 so that they are electrically connected each other. Though the

7:4-13

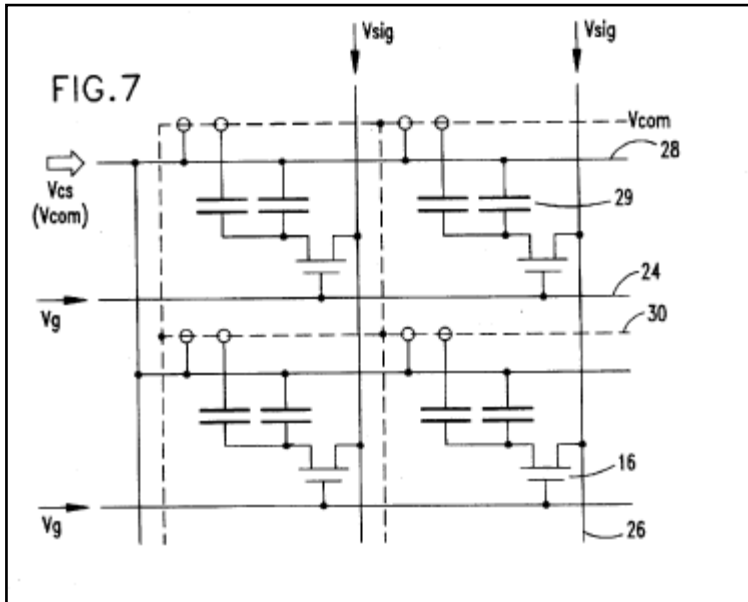
**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**  
**(cont’d):**



Moreover, the present invention does not require a spherical spacer for specifying a cell gap or transfer for supplying a potential to the common electrode 30 as shown in FIG. 8. However, there is no problem in using the spacer and transfer. The equivalent circuit of the TFT-LCD of the present invention is shown in FIG. 7 for comparison with the circuit in FIG. 4. As shown in FIG. 7, the advantages are obtained that the problem of signal delay of Vcom is solved because Vcom is equal to Vcs everywhere in a screen by applying the present invention and it is unnecessary to independently supply Vcom from the outside.

7:32-42

**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**  
**(cont’d):**



Moreover, the present invention does not require a spherical spacer for specifying a cell gap or transfer for supplying a potential to the common electrode 30 as shown in FIG. 8. However, there is no problem in using the spacer and transfer. The equivalent circuit of the TFT-LCD of the present invention is shown in FIG. 7 for comparison with the circuit in FIG. 4. As shown in FIG. 7, the advantages are obtained that the problem of signal delay of Vcom is solved because Vcom is equal to Vcs everywhere in a screen by applying the present invention and it is unnecessary to independently supply Vcom from the outside.

7:32-42

**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED  
HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”  
(cont’d):**

As another method for connecting a common electrode with a storage capacitance line, the storage capacitance line 28 may be formed on the pixel electrode 10 formed on the array substrate 12 through the insulating film 74. In this case, a joint 80 between the storage capacitance line 28 and the common electrode 30 covering the pillar 78 of a color filter is three-dimensionally superimposed on a storage capacitance area 82.

In the case of the third embodiment, a layer 84 made of a conductive body such as a metal formed simultaneously with the data line 26 is first formed on the storage capacitance line 28, and then it is connected with the common electrode 30 to constitute the joint 80 instead of directly connecting the common electrode 30 to the storage capacitance line 28 like the first and second embodiments. Therefore, it is possible to perform fine adjustment for realizing an optically-optimized cell gap by the formation of the conductive body.

7:44-61

**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”**  
**(cont’d):**

Then, the process for manufacturing the liquid crystal display panel **70** of this embodiment is described below.

First, the process for manufacturing the array substrate **12** is described below.

In the first process, the undercoat layer **42** is formed on the array substrate **12**.

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In the second process, the gate electrode **20**, gate line **24**, and storage capacitance line **28** are formed on the undercoat layer **42**.

In the third process, the gate insulating film **44** is formed.

In the fourth process, the semiconductor layer **46** of the TFT **16** is formed.

In the fifth process, the pixel electrode **10** is formed.

In the sixth process, the hole **76** is formed on part of the gate insulating film **44** on the storage capacitance line **28**.

In the seventh process, the source electrode **18** and drain electrode **22** of the TFT **16** and the data line **26** are formed.

In the eighth process, the passivation film **52** covering the TFT **16** is formed.

In the ninth process, the alignment film **54** is formed and treated through rubbing.

Then, the method for manufacturing the color filter substrate **72** is described below.

In the first process, the color filter **32** is formed on the facing substrate **14**, and the pillar **78** of a color filter is formed at a position corresponding to the hole **76** on the array substrate **12**.

In the second process, the common electrode **30** is formed on the color filter **32**.

In the third process, the alignment film **54** is formed and treated through rubbing.

The array substrate **12** and the color filter substrate **77** finished through the above processes are made to face each other and the storage capacitance line **28** viewed through the hole **76** on the array substrate **12** is overlapped with the common electrode **30** at the portion covering the pillar **78** of a color filter on the facing substrate **14** to electrically connect them each other.

Then, the liquid crystal display panel **70** is finished by sealing the perimeter of the assembly with a sealant **64**, injecting liquid crystal into the assembly through an injection hole (not illustrated), and closing the injection hole.

7:62-8:39

**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED  
HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”  
(cont’d):**

The present invention provides a large high-definition liquid crystal display without causing a signal delay even around the central portion of a common electrode. Moreover, because the present invention disuses processes for scattering spacers and dotting transfers, the yield is improved and the cost is decreased.

8:39-45

**INTRINSIC EVIDENCE FOR DISPUTED TERM “PILLARS FORMED  
HIGHER THAN OTHER PORTIONS OF THE COLOR FILTER”  
(cont’d):**

It is said to be unclear in Claims 1 and 5 which elements are “formed higher than other portions” and specify “a cell gap together with objects formed on the array substrate”. These elements are the pillars, which are now expressly identified. It is asked also which elements are electrically connected to the storage capacitance line. The answer is the portions of the common electrode covering at least some of the pillars. This has been clarified as well. The phrase “working on all pixels” is said to be not understood. This phrase merely refers to the fact that the common electrode is the common electrode for all of the pixels. This phrase has been deleted and the concept moved forward in Claims 1 and 5.

App. 08/615,012, 08/05/1997  
Amendment, pg. 6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “INJECTING LIQUID CRYSTAL BETWEEN THE ARRAY SUBSTRATE AND THE COLOR FILTER SUBSTRATE”:**

Then, the process for manufacturing the liquid crystal display panel **70** of this embodiment is described below.

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In the second process, the gate electrode **20**, gate line **24**, and storage capacitance line **28** are formed on the undercoat layer **42**.

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In the fifth process, the pixel electrode **10** is formed.

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In the seventh process, the source electrode **18** and drain electrode **22** of the TFT **16** and the data line **26** are formed.

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Then, the method for manufacturing the color filter substrate **72** is described below.

In the first process, the color filter **32** is formed on the facing substrate **14**, and the pillar **78** of a color filter is formed at a position corresponding to the hole **76** on the array substrate **12**.

In the second process, the common electrode **30** is formed on the color filter **32**.

In the third process, the alignment film **54** is formed and treated through rubbing.

The array substrate **12** and the color filter substrate **77** finished through the above processes are made to face each other and the storage capacitance line **28** viewed through the hole **76** on the array substrate **12** is overlapped with the common electrode **30** at the portion covering the pillar **78** of a color filter on the facing substrate **14** to electrically connect them each other.

Then, the liquid crystal display panel **70** is finished by sealing the perimeter of the assembly with a sealant **64**, injecting liquid crystal into the assembly through an injection hole (not illustrated), and closing the injection hole.

7:62-8:39

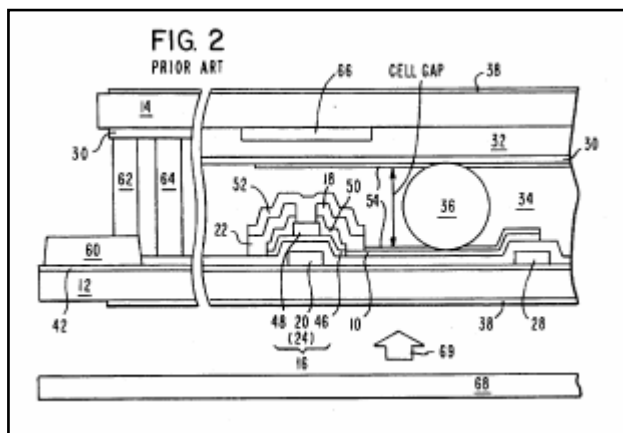
**INTRINSIC EVIDENCE FOR DISPUTED TERM “INJECTING LIQUID CRYSTAL BETWEEN THE ARRAY SUBSTRATE AND THE COLOR FILTER SUBSTRATE” (cont’d):**

## [57]

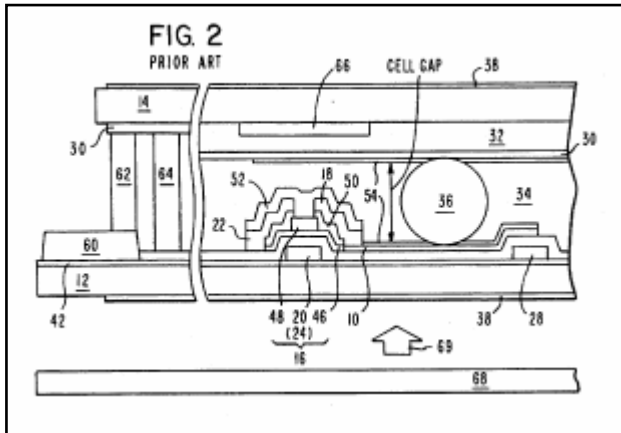
## ABSTRACT

To prevent a signal delay of an active-matrix liquid crystal display from occurring in an active-matrix liquid crystal display having an active element for each pixel electrode, a potential is supplied to a common electrode from a storage capacitance line by forming a pillar of a color filter to specify a cell gap between an array substrate having the storage capacitance line and a facing substrate having the color filter and electrically connecting the common electrode covering the pillar of the color filter with the storage capacitance line on the array substrate. Thereby, it is possible to disuse a transfer dotting process which is a factor of decreasing the yield and also a factor of decreasing the effective display area. Moreover, because the potential is supplied to the common electrode from the storage capacitance line, it is possible to prevent a signal delay of the common electrode from occurring and moreover realize a high-image-quality screen even in a large and high-definition liquid crystal display without causing irregularity of a display screen or decrease of a contrast ratio. Furthermore, because it is possible to disuse a spacer scattering process and specify a cell gap by securing the pillar of the color filter, not only the cell gap is kept constant at any place and the uniformity of the screen is maintained but also spacers do not brighten or the screen is not blackened due to coagulation of the spacers and the image quality is improved. Furthermore, the cost can be decreased because the transfer dotting process and the spacer scattering process are unnecessary.

## Abstract



**INTRINSIC EVIDENCE FOR DISPUTED TERM “INJECTING LIQUID CRYSTAL BETWEEN THE ARRAY SUBSTRATE AND THE COLOR FILTER SUBSTRATE” (cont’d):**



Furthermore, a black matrix 66 is formed like a lattice. In the case of an existing liquid crystal display, transparent spherical spacers 36 are scattered in a liquid crystal layer 34 held by the array substrate 12 and the facing substrate 14 in order to keep a predetermined interval between the two substrates 12 and 14. Moreover, liquid crystal is sealed between the two substrates by a sealant 64. Furthermore, a polarizing

2:13-19

**INTRINSIC EVIDENCE FOR DISPUTED TERM “INJECTING LIQUID CRYSTAL BETWEEN THE ARRAY SUBSTRATE AND THE COLOR FILTER SUBSTRATE” (cont’d):**

Moreover, as shown in FIG. 2, the transparent spherical spacers 36 (made of plastic and glass fiber) are hitherto

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scattered in the liquid crystal layer 34 held by the array substrate 12 and the facing substrate 14 constituting a liquid crystal display in order to keep the substrates 12 and 14 at a predetermined interval. However, under the spacers kept scattered, liquid crystal flows in a panel when an external force is applied to the panel, the spacers are moved in a cell plane due to the flowing of the liquid crystal, and thereby the spacers may scratch the surface of the thin alignment film 54 due to the movement of the spacers. Moreover, a cell gap (interval between electrodes of two substrates) may not be kept constant due to coagulation of the spacers. Unless the cell gap is kept constant, the optical path length difference (product of the birefringence rate and cell gap of the liquid crystal) of the liquid crystal layer changes and thereby, the contrast ratio and the chromaticity of a display screen are changed. Thus, problems occur that the uniformity of the screen cannot be kept or the display quality is deteriorated. Moreover, the spacers are brightened or coagulated, and the light from the backlight 68 is cut off by the coagulated spacers and thereby the screen is blackened by the degree of cut-off light. To solve these problems, various structures are

3:66 – 4:21

Moreover, the spacers are brightened or coagulated, and the light from the backlight 68 is cut off by the coagulated spacers and thereby the screen is blackened by the degree of cut-off light. To solve these problems, various structures are already disclosed which disuse transparent spherical spacers and instead, specify a cell gap by a pillar formed on the array substrate 12 and/or the facing substrate 14 (official gazettes of Japanese Patent Laid-Open Nos. 164723/1985, 105583/1986, 24230/1989, 134733/1986, 163428/1902, 250416/1987, and 196946/1993). However, any one of these disclosures does not show means for solving the problem of signal delay in a TFT-LCD using the H/com inversion driving method.

4:21-30

**INTRINSIC EVIDENCE FOR DISPUTED TERM “INJECTING LIQUID CRYSTAL BETWEEN THE ARRAY SUBSTRATE AND THE COLOR FILTER SUBSTRATE” (cont’d):**

Moreover, as shown in FIG. 2, the existing TFT-LCD has a problem in the structure of supplying the potential of the common electrode 30 on the facing substrate 14 from a plurality of portions at the perimeter of a pixel area of the array substrate 12 side to the common electrode 30 on the facing substrate 14 through the transfer 62 using conductive paste. Because this structure requires a high-accuracy alignment of the transfer 62, it uses two or more transfers to prevent defectives from being produced due to a deviation of a transfer. However, the manufacturing yield is decreased due to defectives produced in a process for dotting a transfer. Moreover, there is the restriction on design that an area for dotting a transfer must be formed at the perimeter of a pixel area. That is, because an area independent of display must exclusively be formed on the array substrate 12 and the facing substrate 14, an effective display area to a substrate size is decreased. However, it is inevitable to use the above structure because it is indispensable for an existing liquid crystal display in view of design.

4:31-49

**SUMMARY OF THE INVENTION**

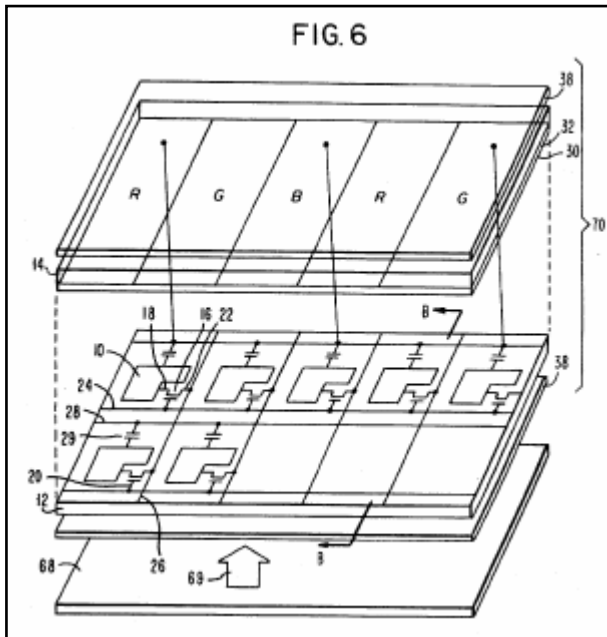
It is an object of the present invention to provide a TFT-LCD making it possible to prevent a signal delay from occurring even around the central portion of a common electrode and moreover prevent irregularity of a display screen and decrease of a contrast ration from occurring.

It is another object of the present invention to provide a TFT-LCD making it possible to keep a cell gap constant without using spacers.

It is still another object of the present invention to provide a TFT-LCD making it possible to supply a potential to a common electrode on a facing substrate without dotting a transfer.

4:51-64

**INTRINSIC EVIDENCE FOR DISPUTED TERM “INJECTING LIQUID CRYSTAL BETWEEN THE ARRAY SUBSTRATE AND THE COLOR FILTER SUBSTRATE” (cont’d):**



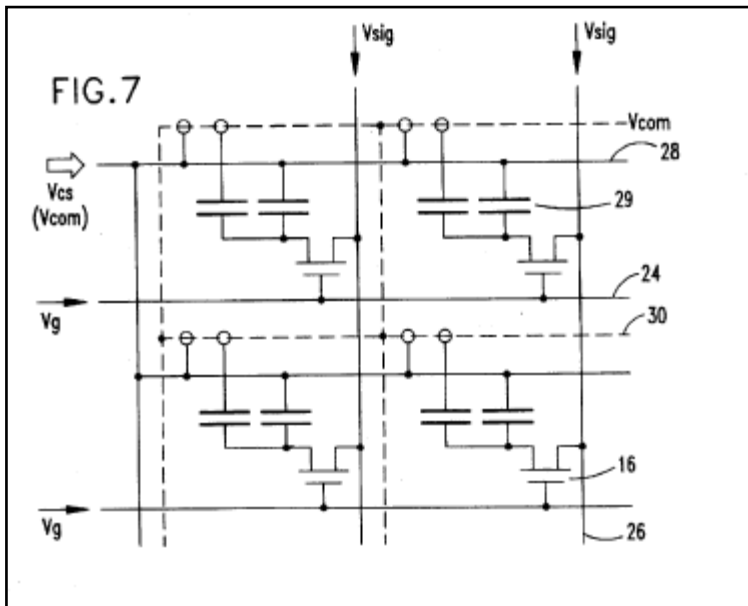
As shown in FIG. 8, the present invention uses a pillar 78 of a color filter 32 instead of a spacer in order to keep a cell gap between two substrates constant. Then, a signal delay of

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a common electrode 30 is prevented from occurring by forming a portion for electrically connecting a common electrode 30 covering the pillar 78 of the color filter 32 with a storage capacitance line 28 everywhere in a pixel area and supplying a potential of the common electrode 30 from the storage capacitance line 28.

4:65 - 5:6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “INJECTING LIQUID CRYSTAL BETWEEN THE ARRAY SUBSTRATE AND THE COLOR FILTER SUBSTRATE” (cont’d):**



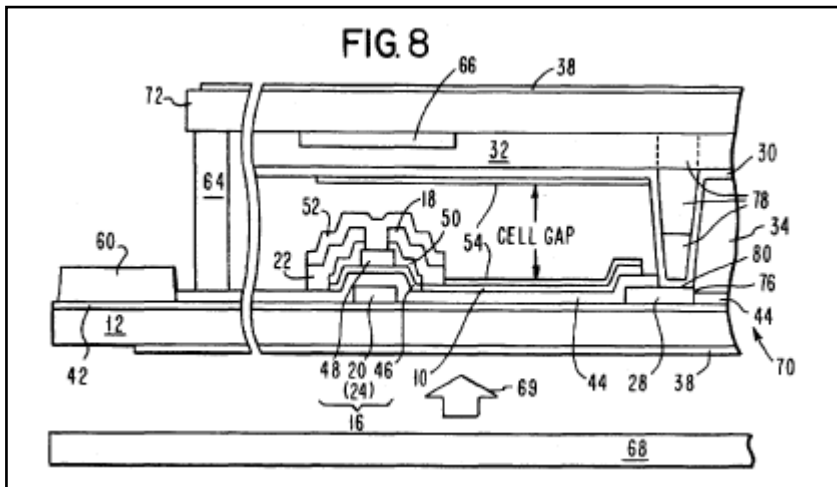
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4:65 - 5:6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “INJECTING LIQUID CRYSTAL BETWEEN THE ARRAY SUBSTRATE AND THE COLOR FILTER SUBSTRATE” (cont’d):**



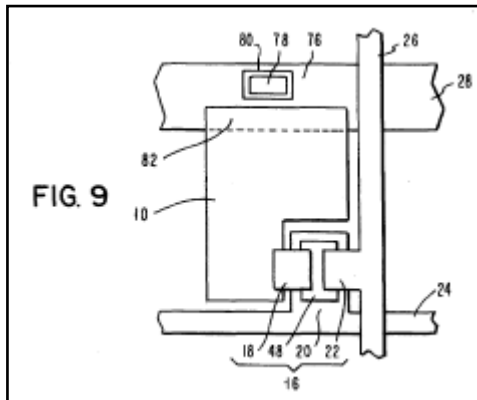
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4:65 - 5:6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “INJECTING LIQUID CRYSTAL BETWEEN THE ARRAY SUBSTRATE AND THE COLOR FILTER SUBSTRATE” (cont’d):**



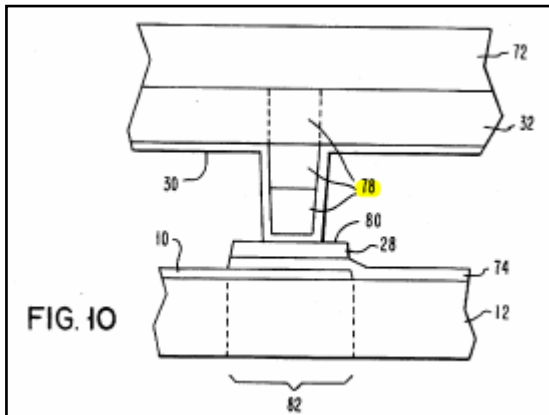
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4:65 - 5:6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “INJECTING LIQUID CRYSTAL BETWEEN THE ARRAY SUBSTRATE AND THE COLOR FILTER SUBSTRATE” (cont’d):**



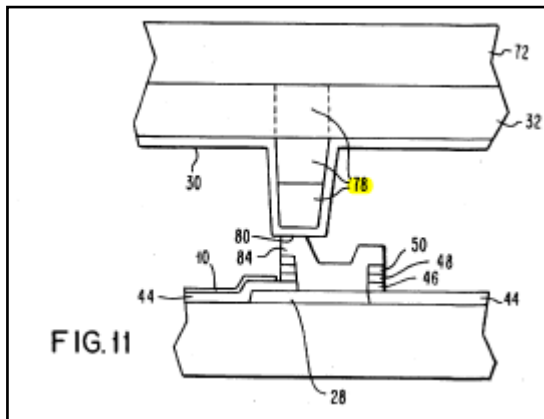
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4:65 - 5:6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “INJECTING LIQUID CRYSTAL BETWEEN THE ARRAY SUBSTRATE AND THE COLOR FILTER SUBSTRATE” (cont’d):**



As shown in FIG. 8, the present invention uses a pillar 78 of a color filter 32 instead of a spacer in order to keep a cell gap between two substrates constant. Then, a signal delay of

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4:65 - 5:6

According to the present invention, the potential of the storage capacitance line 28 is supplied to the common electrode 30 on a facing substrate from joints formed everywhere in a pixel area. Originally, the common-

5:7-10

**INTRINSIC EVIDENCE FOR DISPUTED TERM “INJECTING LIQUID CRYSTAL BETWEEN THE ARRAY SUBSTRATE AND THE COLOR FILTER SUBSTRATE” (cont’d):**

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4:65 - 5:6

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5:7-10

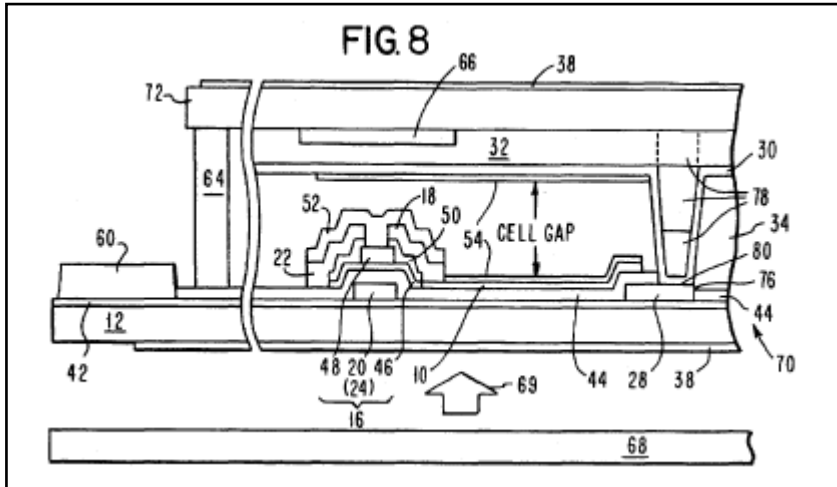
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the facing substrate through a conductive body layer electrically connected to a storage capacitance line, and specifying the cell gap by the sum of the height of the laminate structure on the array substrate and that of the pillar on the facing substrate.

5:57-6:5

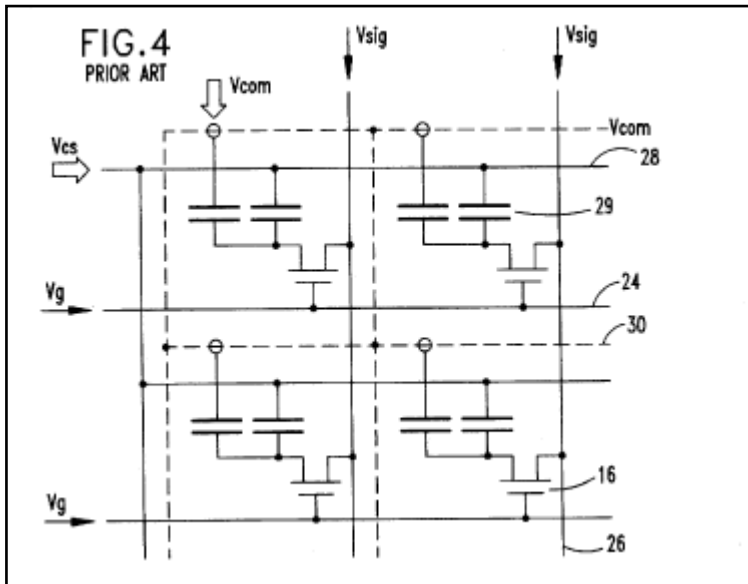
**INTRINSIC EVIDENCE FOR DISPUTED TERM “INJECTING LIQUID CRYSTAL BETWEEN THE ARRAY SUBSTRATE AND THE COLOR FILTER SUBSTRATE” (cont’d):**



Furthermore, as shown in FIG. 8, the embodiment 1 may have a structure in which the gate insulating film 44 is formed on the storage capacitance line 28 in a pixel area on the array substrate 12. That is, the embodiment 1 has a structure in which a hole 76 is formed at part of the gate insulating film 44 on the storage capacitance line 28, the common electrode 30 at a portion covering the pillar 78 of a color filter formed on the color filter substrate 72 is overlapped with the position of the hole 76, and the common electrode 30 contacts the storage capacitance line 28 so that they are electrically connected each other. Though the

7:4-13

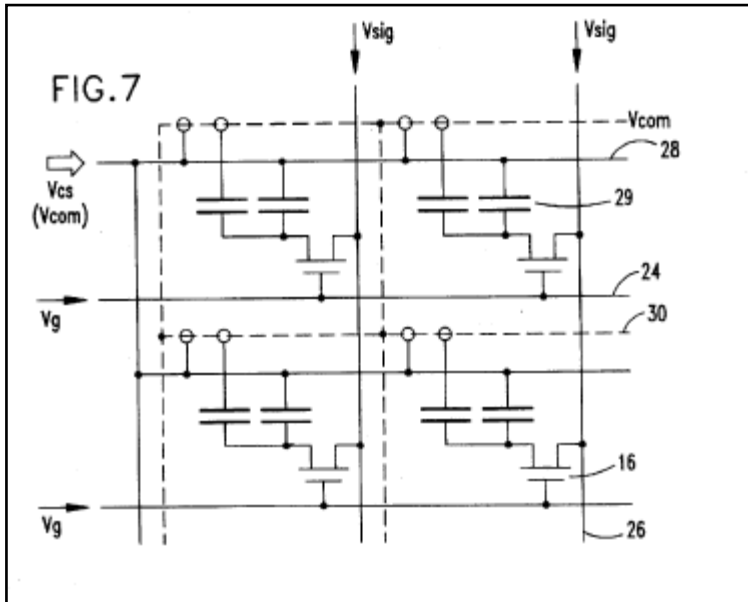
**INTRINSIC EVIDENCE FOR DISPUTED TERM “INJECTING LIQUID CRYSTAL BETWEEN THE ARRAY SUBSTRATE AND THE COLOR FILTER SUBSTRATE” (cont’d):**



Moreover, the present invention does not require a spherical spacer for specifying a cell gap or transfer for supplying a potential to the common electrode 30 as shown in FIG. 8. However, there is no problem in using the spacer and transfer. The equivalent circuit of the TFT-LCD of the present invention is shown in FIG. 7 for comparison with the circuit in FIG. 4. As shown in FIG. 7, the advantages are obtained that the problem of signal delay of Vcom is solved because Vcom is equal to Vcs everywhere in a screen by applying the present invention and it is unnecessary to independently supply Vcom from the outside.

7:32-42

**INTRINSIC EVIDENCE FOR DISPUTED TERM “INJECTING LIQUID CRYSTAL BETWEEN THE ARRAY SUBSTRATE AND THE COLOR FILTER SUBSTRATE” (cont’d):**



Moreover, the present invention does not require a spherical spacer for specifying a cell gap or transfer for supplying a potential to the common electrode 30 as shown in FIG. 8. However, there is no problem in using the spacer and transfer. The equivalent circuit of the TFT-LCD of the present invention is shown in FIG. 7 for comparison with the circuit in FIG. 4. As shown in FIG. 7, the advantages are obtained that the problem of signal delay of Vcom is solved because Vcom is equal to Vcs everywhere in a screen by applying the present invention and it is unnecessary to independently supply Vcom from the outside.

7:32-42

**INTRINSIC EVIDENCE FOR DISPUTED TERM “INJECTING LIQUID CRYSTAL BETWEEN THE ARRAY SUBSTRATE AND THE COLOR FILTER SUBSTRATE” (cont’d):**

As another method for connecting a common electrode with a storage capacitance line, the storage capacitance line 28 may be formed on the pixel electrode 10 formed on the array substrate 12 through the insulating film 74. In this case, a joint 80 between the storage capacitance line 28 and the common electrode 30 covering the pillar 78 of a color filter is three-dimensionally superimposed on a storage capacitance area 82.

In the case of the third embodiment, a layer 84 made of a conductive body such as a metal formed simultaneously with the data line 26 is first formed on the storage capacitance line 28, and then it is connected with the common electrode 30 to constitute the joint 80 instead of directly connecting the common electrode 30 to the storage capacitance line 28 like the first and second embodiments. Therefore, it is possible to perform fine adjustment for realizing an optically-optimized cell gap by the formation of the conductive body.

7:44-61

**INTRINSIC EVIDENCE FOR DISPUTED TERM “INJECTING LIQUID CRYSTAL BETWEEN THE ARRAY SUBSTRATE AND THE COLOR FILTER SUBSTRATE” (cont’d):**

Then, the process for manufacturing the liquid crystal display panel **70** of this embodiment is described below.

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In the second process, the gate electrode **20**, gate line **24**, and storage capacitance line **28** are formed on the undercoat layer **42**.

In the third process, the gate insulating film **44** is formed.

In the fourth process, the semiconductor layer **46** of the TFT **16** is formed.

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In the seventh process, the source electrode **18** and drain electrode **22** of the TFT **16** and the data line **26** are formed.

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The array substrate **12** and the color filter substrate **77** finished through the above processes are made to face each other and the storage capacitance line **28** viewed through the hole **76** on the array substrate **12** is overlapped with the common electrode **30** at the portion covering the pillar **78** of a color filter on the facing substrate **14** to electrically connect them each other.

Then, the liquid crystal display panel **70** is finished by sealing the perimeter of the assembly with a sealant **64**, injecting liquid crystal into the assembly through an injection hole (not illustrated), and closing the injection hole.

7:62-8:39

**INTRINSIC EVIDENCE FOR DISPUTED TERM “INJECTING  
LIQUID CRYSTAL BETWEEN THE ARRAY SUBSTRATE AND THE  
COLOR FILTER SUBSTRATE” (cont’d):**

The present invention provides a large high-definition liquid crystal display without causing a signal delay even around the central portion of a common electrode. Moreover, because the present invention disuses processes for scattering spacers and dotting transfers, the yield is improved and the cost is decreased.

8:39-45

**INTRINSIC EVIDENCE FOR DISPUTED TERM “INJECTING LIQUID CRYSTAL BETWEEN THE ARRAY SUBSTRATE AND THE COLOR FILTER SUBSTRATE” (cont’d):**

It is said to be unclear in Claims 1 and 5 which elements are “formed higher than other portions” and specify “a cell gap together with objects formed on the array substrate”. These elements are the pillars, which are now expressly identified. It is asked also which elements are electrically connected to the storage capacitance line. The answer is the portions of the common electrode covering at least some of the pillars. This has been clarified as well. The phrase “working on all pixels” is said to be not understood. This phrase merely refers to the fact that the common electrode is the common electrode for all of the pixels. This phrase has been deleted and the concept moved forward in Claims 1 and 5.

App. 08/615,012, 08/05/1997  
Amendment, pg. 6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “INJECTING LIQUID CRYSTAL BETWEEN THE ARRAY SUBSTRATE AND THE COLOR FILTER SUBSTRATE”:**

a color filter on the facing substrate 14 to electrically connect them each other.

Then, the liquid crystal display panel 70 is finished by sealing the perimeter of the assembly with a sealant 64, injecting liquid crystal into the assembly through an injection hole (not illustrated), and closing the injection hole.

8:39-45

# **EXHIBIT L-23**

**EX. L-23**  
**CMO US PATENT NO. 6,734,944**

**INDEX OF DISPUTED TERMS**

<b><u>CLAIM TERMS</u></b>	<b><u>PAGE</u></b>
at least one of the group consisting of .....	1
dynamic hardness value (DH).....	9
hardness value of plastic deformation (HV) .....	9
the length of one side of the upper spacer surface .....	11

**EXHIBIT L-23**  
**U.S. PATENT NO. 6,734,944**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 1**

**4.** A method for providing a liquid crystal display comprising the steps of:

disposing a first and second substrate facing each other, said first and second substrates having a display and a non-display region;

selecting a photosensitive resin to regulate a cell gap between the first and the second substrate;

wherein said selecting of a photosensitive resin comprises choosing a photosensitive resin based on **at least one of the group consisting of:**

(a) a dynamic hardness value from 26 to 30, which is obtained by the following formula:

$$DH = K \times P_{\max} / h_{\max}^2,$$

wherein DH is dynamic hardness, K is a constant value assigned to the indentator used to test the liquid crystal display, P<sub>max</sub> is maximum load, and h<sub>max</sub> is the total maximum variation obtained by adding the measured elastic deformation and plastic deformation under load;

(b) a hardness value of plastic deformation (HV) from 38 to 46, which is obtained by the following formula:

$$HV = K \times P_{\max} / h_r^2,$$

wherein HV is hardness of plastic deformation, K is a constant value assigned to the indentator used to test the liquid crystal display, P<sub>max</sub> is maximum

**cont'd on next page**

**LGD's Claim Construction**

**at least one of the group consisting of** – Indefinite, or, means one or more of the limitations selected from (a) to (e)

**the length of one side of the upper spacer surface** – Indefinite, or, the distance between two specific points on opposite side of the spacer (The location of the two points are determined by where a line that runs parallel to the one side and parallel to the substrate intersects the opposite sides. The location of the parallel line is determined by multiplying the height of the spacer by a constant. The height of the spacer is determined by the shortest perpendicular distance measured from the bottom of the spacer to a line tangent to the top of the spacer and parallel to the substrate)

**EXHIBIT L-22**  
**U.S. PATENT NO. 6,734,944**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 1 (cont'd)**

**LGD's Claim Construction**

load, and  $h_r$  is measured variation when the tangent in the maximum variation point of a curb has no load in the case of unloading;

- (c) an elastic coefficient from 100 to 500 kg/mm<sup>2</sup>; a linear expansion coefficient which is nearly equal to the coefficient of volume expansion per unit area of the liquid crystal;
- (d) wherein for rectangular spacers, the length of one side of the upper spacer surface is 50 to 90% smaller than the length of one side of the lower spacer surface and wherein for circular spacers, the diameter of the upper spacer surface is 50 to 90% smaller than the diameter of the lower spacer surface; and
- (e) a column occupancy ratio from 0.05 to 0.86%, which is expressed as follows:

Column occupancy ratio = (Lower bottom area of column × column density / pixel area) × 100

Column density: Total number of columns / total number of pixels;

placing spacers comprising said photosensitive resin between the first and second substrates, said spacers being placed in the non-display region of at least one of the first and the second substrates; and  
providing liquid crystal between the first and the second substrates.

**INTRINSIC EVIDENCE FOR DISPUTED TERM “AT LEAST ONE OF THE GROUP CONSISTING OF”:**

As material for forming the spacers **18**, photosensitive resin is employed and more preferably photosensitive resin that satisfies the following conditions is employed. Namely, a photosensitive resin for forming the spacers **18**, whose dynamic hardness value (DH) is between 26 and 30 evaluated by the following formula, is selectively used:

$$DH=K \times P_{\max} / h_{\max}^2$$

DH: dynamic hardness value (Kgf/mm<sup>2</sup>)

P<sub>max</sub>: maximum load (Kgf)

h<sub>max</sub>: total maximum variation (mm) obtained by adding elastic deformation and plastic deformation

wherein a constant K represents a value obtained by the variation of an indenter inherent to the liquid crystal

3:55-67

display. This formula is derived by conducting a dynamic hardness test. Dynamic hardness used herein means hardness obtained when the load is sequentially varied to be extrapolated to a zero load and parameter means a target load. This dynamic hardness represents a function of depth to the hardness because this dynamic hardness varies the load sequentially.

The spacers **18**, whose dynamic hardness value (DH) is in the range from 26 to 30, is neither hard nor soft. When the dynamic hardness value (DH) is below 26, there is a wide variation in the cell gaps after the force is applied from the outside of the liquid crystal display and this causes a problem that image quality is easily changed. Further, when the dynamic hardness value (DH) exceeds 30, undesired low-temperature bubbles are generated in the liquid crystal when the liquid crystal display is cooled down to a low temperature.

4:1-17

**INTRINSIC EVIDENCE FOR DISPUTED TERM “AT LEAST ONE OF THE GROUP CONSISTING OF” (cont’d):**

Also, the spacers **18** are preferably formed of photosensitive resin, which satisfies the following conditions: more specifically, photosensitive resin for forming the spacers **18**, whose plastic deformation hardness value (HV) is between 38 and 46 obtained by the following formula, is selectively used:

$$HV = K \times P_{\max} / h_r^2$$

HV: plastic deformation hardness (Kgf/mm<sup>2</sup>)

P<sub>max</sub>: maximum load (Kgf)

h<sub>r</sub>: variation (mm) when the tangent in the maximum variation point of a curb has no load in the case of unloading.

wherein a constant K represents a value obtained by the variation of an indentator inherent to the liquid crystal display.

4:18-32

Further, this formula determines a tangent in the maximum different point (same as the maximum different point in loading) of the curve when unloading and the hardness corresponding to Vickers' hardness by separating the plastic variation from its inclination. More specifically, this is led by the plastic hysteresis curve obtained by a compression variation measurement against the load. This plastic deformation hardness value (HV) may be a little different from actual Vickers' value due to the shape of the indentator or the like.

4:33-41

The plastic deformation hardness value (HV) of the spacers **18** are preferably in the range from 38 to 46. When their plastic deformation hardness value (HV) is below 38, permanent image quality defects occur because the dimensions of the spacers cannot return to the dimensions before deformation due to large plastic deformation variation caused by the small cell gaps when the external force is applied to the liquid crystal display. When the plastic deformation hardness value (HV) exceeds 46, undesired low-temperature bubbles can be generated.

If the spacers **18** meet either of the conditions of hardness value (DH) or plastic deformation hardness value (HV) evaluated by the above formula, certain effects can be obtained, but it is desirable to meet both conditions.

4:42-55

**INTRINSIC EVIDENCE FOR DISPUTED TERM “AT LEAST ONE OF THE GROUP CONSISTING OF” (cont’d):**

Since the spacers **18** are disposed in the nondisplay region on the array substrate **12**, it does not affect the image quality, however, when the spacers **18** are few in number, namely, when the total lower bottom area of the pillar-like spacers **18** is small, it is difficult to keep the cell gaps **16** nearly constant due to weak bearing capacity of the color filter substrate **14**. In addition, when a local load is imposed on the color filter substrate **14**, the spacers **18** can be easily broken. On the contrary, when the spacers **18** are large in number, the strong bearing capacity of the color filter substrate **14** allows the cell gaps **16** to keep constant, and therefore, the spacers **18** can sufficiently carry the local load imposed on the color

4:56-67

filter substrate **14**, however, when the liquid crystal **20** shrinks by exposing the liquid crystal display **10** to a low temperature, a vacuum portion (low-temperature bubbles) is generated. Therefore, it is important that the number of the spacers **18** is appropriate for the array substrate **12** or the color filter substrate **14**, namely, appropriate area, the occupancy ratio of the spacers **18** in the substrate is important.

5:1-7

Where the occupancy ratio (column occupancy ratio) is defined as the ratio of the pixel area that is made up by the lower bottom area of the column (spacers **18**) constituting the cell gaps **16** forms against the pixel area, the column occupancy ratio is expressed as follows:

$$\text{Column occupancy ratio} = (\text{Lower bottom area of column} \times \text{column density} / \text{pixel area}) \times 100$$

wherein column density means the number of the columns constituting the cell gaps per pixel can be represented by the following formula:

$$\text{Column density} = \text{total number of columns} / \text{total number of pixels}$$

When the study results of the inventors of the present invention show that the column occupancy ratio expressed by the above formula ranges from 0.05 to 0.86%, the pillar-like spacers **18** can sufficiently carry the local load without being crushed. Further, even if it is exposed to a low temperature, no low-temperature bubbles are generated inside the cell gaps **16** because the spacers **18** contract in response to a negative pressure generated in the cell gaps **16** as the liquid crystal contracts.

5:8-30

**INTRINSIC EVIDENCE FOR DISPUTED TERM “AT LEAST ONE OF THE GROUP CONSISTING OF” (cont’d):**

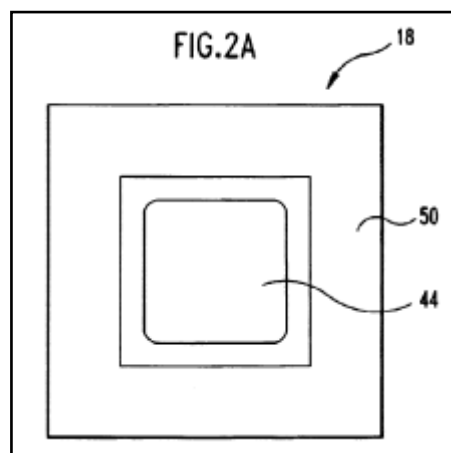
The spacers 18 having various properties have thus been described above, however, it is sufficient that the properties of the spacer applied to the liquid crystal display according to the present invention meet at least one of the requirements. The spacer which meets two or more requirements is most desirable. A JNPC-43 (manufactured by JSR) can be

6:47-51

The spacers of the liquid crystal display according to the present invention are not only formed on a predetermined portion by a photosensitive resin, but also have physical value or form, such as predetermined hardness value and plastic deformation hardness value, etc. Therefore, the spacers return to the previous state without being destroyed due to local load, so that the cell gaps can be kept nearly constant. Even if the liquid crystal display is exposed to a low temperature, neither vacuum portions inside the cell gaps nor low-temperature bubbles will be generated because the spacers get shrinked by external pressure or the like as the liquid crystal inside the cell gaps shrink.

8:9-21

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE LENGTH OF ONE SIDE OF THE UPPER SPACER SURFACE”:**



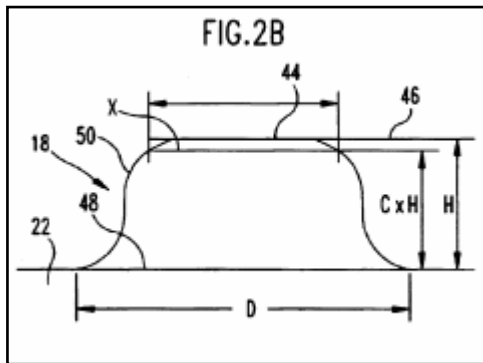
Measuring method is as follows: first, the tangent line 46 is drawn on the upper bottom 44 of the spacers 18 by using an enlarged cross-sectional photo of the spacers and then the length D of one side of a lower bottom 48 in the same direction as the tangent line 46 is measured. Next, the spacing (height) H between the lower bottom 48 (substrate

5:62-67

22) of the spacers 18 and the tangent line 46 of the upper bottom 44 is measured. The dimensions obtained by multiplying this height H by certain constant C below 1 such as 0.9 is defined as the height of the upper bottom ( $C \times H$ ). A line X parallel to the substrate 22 is drawn on that position, and the spacing between the two points of intersection of the line X and an outline 50 of the spacers 18 (side surface) is defined as the dimensions of the upper bottom. Etching is controlled, so that the ratio of the length of the upper bottom to that of the lower bottom obtained in this manner can be in the range of 50 to 90%. The ratio of the length of the upper bottom to that of the lower bottom varies according to the value of the constant C multiplying the height H of the upper bottom. The above range of 50 to 90% is the value to be obtained when the constant C is set at 0.9.

6:1-15

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE LENGTH OF ONE SIDE OF THE UPPER SPACER SURFACE” (cont’d):**



Measuring method is as follows: first, the tangent line 46 is drawn on the upper bottom 44 of the spacers 18 by using an enlarged cross-sectional photo of the spacers and then the length D of one side of a lower bottom 48 in the same direction as the tangent line 46 is measured. Next, the spacing (height) H between the lower bottom 48 (substrate

5:62-67

22) of the spacers 18 and the tangent line 46 of the upper bottom 44 is measured. The dimensions obtained by multiplying this height H by certain constant C below 1 such as 0.9 is defined as the height of the upper bottom ( $C \times H$ ). A line X parallel to the substrate 22 is drawn on that position, and the spacing between the two points of intersection of the line X and an outline 50 of the spacers 18 (side surface) is defined as the dimensions of the upper bottom. Etching is controlled, so that the ratio of the length of the upper bottom to that of the lower bottom obtained in this manner can be in the range of 50 to 90%. The ratio of the length of the upper bottom to that of the lower bottom varies according to the value of the constant C multiplying the height H of the upper bottom. The above range of 50 to 90% is the value to be obtained when the constant C is set at 0.9.

6:1-15

**EXHIBIT L-22**  
**U.S. PATENT NO. 6,734,944**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 1**

4. A method for providing a liquid crystal display comprising the steps of:

disposing a first and second substrate facing each other, said first and second substrates having a display and a non-display region;

selecting a photosensitive resin to regulate a cell gap between the first and the second substrate;

wherein said selecting of a photosensitive resin comprises choosing a photosensitive resin based on at least one of the group consisting of:

- (a) a **dynamic hardness value** from 26 to 30, which is obtained by the following formula:

$$DH = K \times P_{\max} / h_{\max}^2,$$

wherein DH is dynamic hardness, K is a constant value assigned to the indentator used to test the liquid crystal display,  $P_{\max}$  is maximum load, and  $h_{\max}$  is the total maximum variation obtained by adding the measured elastic deformation and plastic deformation under load;

- (b) a **hardness value of plastic deformation (HV)** from 38 to 46, which is obtained by the following formula:

$$HV = K \times P_{\max} / hr^2,$$

wherein HV is hardness of plastic deformation, K is a constant value assigned to the indentator used to test the liquid crystal display,  $P_{\max}$  is maximum

**cont'd on next page**

**LGD's Position**

**dynamic hardness value –**  
Indefinite

**hardness value of plastic deformation (HV) - Indefinite**

**EXHIBIT L-22**  
**U.S. PATENT NO. 6,734,944**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 1 (cont'd)**

load, and  $h_r$  is measured variation when the tangent<sup>1</sup> in the maximum variation point of a curb has no load in the case of unloading;

- (c) an elastic coefficient from 100 to 500 kg/mm<sup>2</sup>; a linear expansion coefficient which is nearly equal to the coefficient of volume expansion per unit area of the liquid crystal;
- (d) wherein for rectangular spacers, the length of one side of the upper spacer surface is 50 to 90% smaller than the length of one side of the lower spacer surface and wherein for circular spacers, the diameter of the upper spacer surface is 50 to 90% smaller than the diameter of the lower spacer surface; and
- (e) a column occupancy ratio from 0.05 to 0.86%, which is expressed as follows:

Column occupancy ratio = (Lower bottom area of column / column density / pixel area) × 100

Column density: Total number of columns / total number of pixels;

placing spacers comprising said photosensitive resin between the first and second substrates, said spacers being placed in the non-display region of at least one of the first and the second substrates; and  
providing liquid crystal between the first and the second substrates.

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “DYNAMIC HARDNESS VALUE (DH)” AND “HARDNESS VALUE OF PLASTIC DEFORMATION (HV)”:**

<i>Response to Arguments</i>
Applicant's arguments filed have been fully considered but they are not persuasive.
With regard to the value of k, it is still a concern that the value is variable so that the value of the equation is not set, that it is dependent upon the equipment testing, so determination of whether a reference such as the device of Shioda may actually be the same would be determined by the selection of the equipment used, making the value indefinite. Since the examiner cannot tell if the value is test equipment independent or not, the examiner has dropped the rejection. However, if the value is determined by the equipment used, the language would indeed be indefinite.

Office Action at 9

# **EXHIBIT L-24**

**Ex. L-24**  
**CMO US PATENT NO. 6,778,160**

**INDEX OF DISPUTED TERMS**

<b><u>CLAIM TERMS</u></b>	<b><u>PAGE</u></b>
video signal .....	39
a storage for storing the previous brightness level of the video signal input through said input logic.....	1
determinator for determining an output brightness level.....	1
brightness level .....	1
the next brightness level of the next video signal input to said input logic .....	39
so as to make a time integration quantity of a brightness change substantially equal to an ideal quantity of light in a stationary state with respect to the next brightness level .....	2
ideal quantity of light in a stationary state .....	66
image displaying liquid crystal cell .....	86
first brightness information for an input pixel .....	39
pixel.....	86
frame buffer .....	86
second brightness information for the next input pixel .....	39
an offset for making the time integration quantity of a brightness change substantially equal to an ideal light quantity which is the brightness in a stationary state to said second brightness information .....	66
time integration quantity of a brightness change .....	100
ideal light quantity which is the brightness in a stationary state.....	100
substantially equal.....	86

**EXHIBIT L-24**  
**U.S. PATENT NO. 6,778,160**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 1**

1. A liquid crystal display, comprising:  
an input logic for inputting a video signal from a host;  
a storage for storing the previous brightness level of the video signal input through said input logic;  
a determinator for determining an output brightness level based on the previous brightness level stored in said storage and the next brightness level of the next video signal input to said input logic so as to make a time integration quantity of a brightness change substantially equal to an ideal quantity of light in a stationary state with respect to the next brightness level; and  
a driver for driving an image displaying liquid crystal cell based on said output brightness level determined by said determination logic.

**LGD's Claim Construction**

**a storage for storing the previous brightness level of the video signal input through said input logic** - memory that temporarily holds the brightness level of the video signal received from the host through input logic for the previous time increment.

**determinator for determining an output brightness level** - circuit or logic that determines the output brightness level by applying an offset to the next brightness level that is predetermined based on a difference in quantity of light between the actual and ideal response characteristics of the liquid crystal cell.

**brightness level<sup>1</sup>** - gray scale value or luminance value.

<sup>1</sup> Disputed Term "brightness level" also appears in asserted Claim 2 in the same context.

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “A STORAGE FOR STORING THE PREVIOUS BRIGHTNESS LEVEL OF THE VIDEO SIGNAL INPUT THROUGH SAID INPUT LOGIC”:**

The “ideal quantity of light” herein is, to take an example, the quantity of light based on a response characteristic which provides a target brightness level at a time point at which the frame is turned on and provides a brightness level of zero at the time point at which the frame is turned off on a display device in which each pixel is driven for each frame. The brightness level can be represented as a target brightness value by a gray scale and considered as an indication of the characteristic of human visual sensation to brightness. In

4:41-50

The apparatus further comprises a frame buffer for storing the brightness information of the input wire-frame model as the previous brightness, and characterized by that the storage portion stores the offset as table information based on a relation between the previous brightness stored in the frame buffer and the brightness of the next input wire-frame model, thus, flicker in a moving state can be advantageously inhibited without providing separate determining units for moving and stationary states.

5:31-39

Viewing the present invention as a liquid crystal driving method, the liquid crystal driving method of the present invention is characterized by the steps of storing first brightness information for an input pixel in a frame buffer, and applying, based on second brightness information for the next input pixel and the first brightness information stored in the frame buffer, an offset for making the time integration quantity of a brightness change substantially equal to an ideal light quantity which is brightness in a stationary state to the second brightness information. The steps further include the outputting of the second brightness information to which the offset is applied to a driving circuit for driving an liquid crystal cell, and storing the second brightness information for the input pixel in a frame buffer. This liquid crystal driving method allows the inhibition of flicker by using a simple apparatus without globally determining whether a model is moving or stationary.

6:11:27

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “A STORAGE FOR STORING THE PREVIOUS BRIGHTNESS LEVEL OF THE VIDEO SIGNAL INPUT THROUGH SAID INPUT LOGIC” (cont'd):**

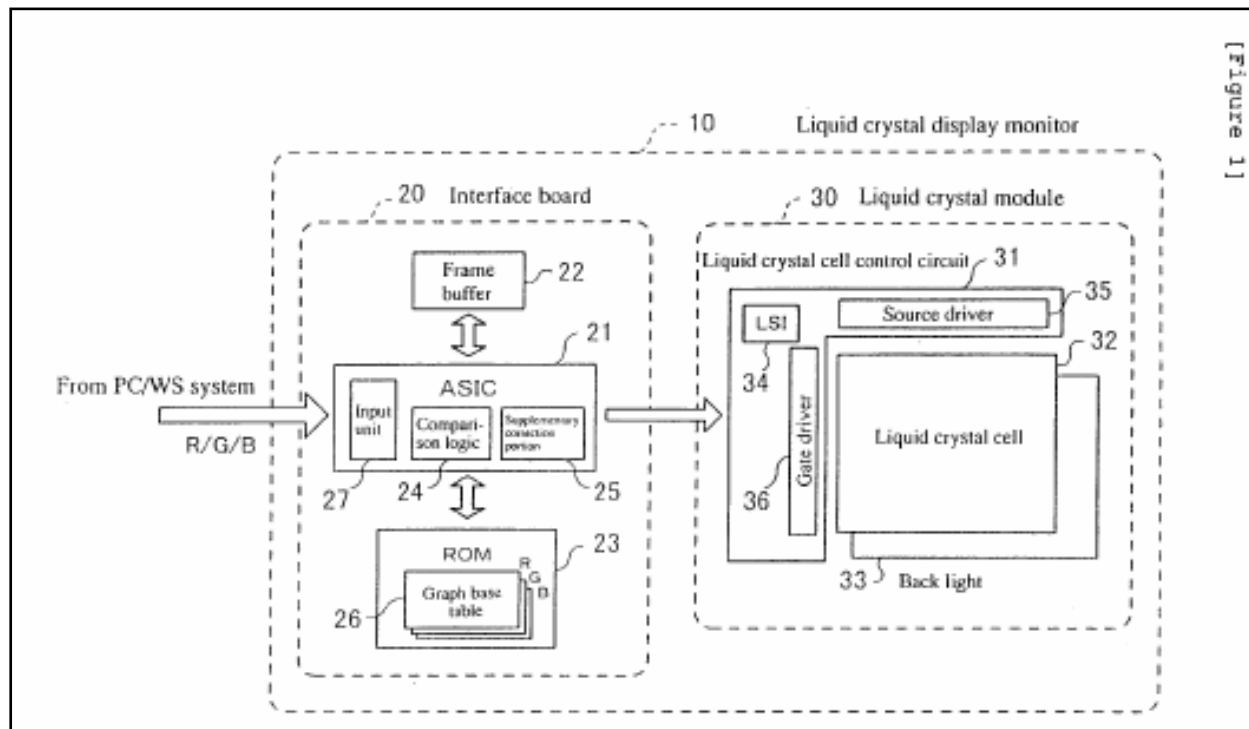


FIG. 1 is a drawing for showing the overall configuration of a liquid crystal display according to an embodiment of the present invention. Reference number 10 denotes a liquid

6:51-53

The I/F board 20 comprises a input unit 27 for inputting video data from a host such as a PC/WS system, a comparison logic 24 for comparing the previous brightness with the next brightness for an input video signal, and an Application-Specific Integrate Circuit (ASIC) 21 including a logic having units such as a supplementary correction portion 25 for performing a supplementary correction. The I/F board 20 also comprises a frame buffer 22 for temporarily storing the input video signal and read-only memory (ROM) 23 containing information needed for the operation of the ASIC 21. The frame buffer 22 stores input video signal value

6:66-7:9

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “A STORAGE FOR STORING THE PREVIOUS BRIGHTNESS LEVEL OF THE VIDEO SIGNAL INPUT THROUGH SAID INPUT LOGIC” (cont'd):**

[Figure 7]

26 (Graph base table)

Next brightness Previous brightness	0	10	20	30	40	50	60	70	80	90	100
0	0	28	48	63	74	83	88	93	96	98	100
10	0	10	30	45	56	65	70	75	80	90	100
20	0	10	20	35	46	55	60	70	80	90	100
30	0	10	20	30	41	50	60	70	80	90	100
40	0	10	20	30	40	50	60	70	80	90	100
50	0	10	20	30	40	50	60	70	80	90	100
60	0	10	20	30	40	50	60	70	80	90	100
70	0	10	20	30	40	50	59	70	80	90	100
80	0	10	20	30	40	45	54	65	80	90	100
90	0	10	20	25	30	35	44	55	70	90	100
100	0	2	4	7	12	17	26	38	52	72	100

FIG. 7 is a table showing a relation between brightness L1 and L2 and represents the content of the graph base table 26 stored in the ROM 23 shown in FIG. 1. The content of the graph base table 26 shown in FIG. 7 represents a relation between the previous brightness and the next brightness for the LC cell 32 having the characteristic shown in FIG. 2, by taking the effect shown in FIG. 6 into consideration. The previous brightness can be obtained from a video signal input through the ASIC21 shown in FIG. 1 and stored in the frame buffer 22. The next brightness can be obtained from the next video signal input to the ASIC 21. The graph base table 26 is constructed for each of the R, G, B color signals and the values in the table vary depending on the characteristic of the LC cell 32.

9:26-39

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “A STORAGE FOR STORING THE PREVIOUS BRIGHTNESS LEVEL OF THE VIDEO SIGNAL INPUT THROUGH SAID INPUT LOGIC” (cont'd):**

26 (Graph base table)

Next brightness Previous brightness	0	10	20	30	40	50	60	70	80	90	100
0	0	28	48	63	74	83	88	93	96	98	100
10	0	10	30	45	56	65	70	75	80	90	100
20	0	10	20	35	46	55	60	70	80	90	100
30	0	10	20	30	41	50	60	70	80	90	100
40	0	10	20	30	40	50	60	70	80	90	100
50	0	10	20	30	40	50	60	70	80	90	100
60	0	10	20	30	40	50	60	70	80	90	100
70	0	10	20	30	40	50	59	70	80	90	100
80	0	10	20	30	40	45	54	65	80	90	100
90	0	10	20	25	30	35	44	55	70	90	100
100	0	2	4	7	12	17	26	38	52	72	100

[Figure 7]

The first row of the graph base table 26 shown in FIG. 7 indicates brightness output for the next brightness when the previous brightness is 0 and match the readings of the R signal in the moving state line 50 in the graph shown in FIG. 2. For example, if the next brightness is “10”, find a value

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41. In this embodiment, if a difference between the previous brightness and the next brightness is greater than an offset, the next brightness is output without change. For example,

9:40-44

9:56-58

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “A STORAGE FOR STORING THE PREVIOUS BRIGHTNESS LEVEL OF THE VIDEO SIGNAL INPUT THROUGH SAID INPUT LOGIC” (cont'd):**

On the other hand, when brightness falls from a certain halftone to another halftone, the offset is subtracted from the previous brightness. The example in FIG. 7 shows a case where the characteristic of the LC cell 32 when brightness rises (the cell is turned on) is the same as that when the brightness falls (the cell is turned off). In this example, if the previous brightness is 100 and the next brightness is 10, the output value will be  $100 - 98 = 2$ . The value “98” is equal to the value when the previous brightness is 0 and the next brightness is 90 in FIG. 7. Similarly, if the previous brightness is 100 and the next brightness is 20, then  $100 - 96 = 4$ . If the previous brightness is 90 and the next brightness is 30, then  $100 - 75 = 25$ . The value “75” is equal to the value when the previous brightness is 10 and the next brightness is 70 in FIG. 7. Similarly, if the previous brightness is 90 and the next brightness is 40, then  $100 - 70 = 30$ . The value “70” is equal to the value when the previous brightness is 10 and the next brightness is 60 in FIG. 7.

9:64 - 10:3

As described above, the embodiment is configured to store offsets in table form based on the relation between a brightness level in a stationary state and that in a moving state in order to obtain an ideal quantity of light. Thus, even during the movement of a display image on the LCD screen, the image can be displayed virtually the same brightness to the eye as in its stationary state, thereby inhibiting flicker on the screen.

In addition, the embodiment is configured to store the previous brightness level (gray scale value) in the frame buffer 22 and a supplementary correction is made by the ASIC 21 using the data in the graph base table 26 based on the relation between the brightness level of the next video data and the previous brightness level. Thus, whether a wire-frame model is moving or stationary is not required to be determined. Instead, the movement of the model can be determined from a difference between the determined brightness and the previous brightness. As a result, flicker can be inhibited by a simple circuit configuration.

10:49-67

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DETERMINATOR  
FOR DETERMINING AN OUTPUT BRIGHTNESS LEVEL”**

In Published Unexamined Japanese Patent Application No. 2-153687, a LCD is provided which is configured to discriminate between a static image area having less motion and a fast-moving area and apply a signal process only to the moving area to emphasize time-based changes in an image, thereby improving response time in the image area where better response time is required to reduce visual persistence and noise.

In Published Unexamined Japanese Patent Application No. 4-365094, a LCD is provided which is configured to be driven by reading pre-stored optimum image data according to the direction and degree of a change when the image data changes, thereby allowing the LCD to rapidly follow the fast-changing image.

In Published Unexamined Japanese Patent Application No. 6-62355, a technology is disclosed which superposes a difference component between fields or frames on a video

1:50-67

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In Published Unexamined Japanese Patent Application No. 7-56532, a technology is disclosed which provides table memory containing a table of image increase/decrease values and drive a liquid crystal panel (liquid crystal cell) by performing an addition/subtraction in order to improve response changes due to changes in the gray scale in the liquid crystal panel. However, the amount to be added or subtracted is expressed only by the word “optimum” and no specific amount is disclosed.

2:4-12

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DETERMINATOR FOR DETERMINING AN OUTPUT BRIGHTNESS LEVEL” (cont'd)**

The “ideal quantity of light” herein is, to take an example, the quantity of light based on a response characteristic which provides a target brightness level at a time point at which the frame is turned on and provides a brightness level of zero at the time point at which the frame is turned off on a display device in which each pixel is driven for each frame. The brightness level can be represented as a target brightness value by a gray scale and considered as an indication of the characteristic of human visual sensation to brightness. In addition, a brightness change can be considered as a response characteristic depending on the types of liquid crystal cells (liquid crystal panels). Quantity of light is considered as a time integration quantity of a brightness change and can be expressed as brightness\_time, if the brightness is constant. The representation “substantially

4:42-56

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The determinator is characterized by comprising a table for storing a brightness level determined by the characteristic of a liquid crystal cell according to a relation between the previous brightness level and the next brightness level, and determining an output brightness level by modifying the next brightness level based on the brightness level read from the table. With this configuration, flicker due to changes in

4:50-67

2:4-12

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DETERMINATOR FOR DETERMINING AN OUTPUT BRIGHTNESS LEVEL” (cont'd)**

The offset set by the setting elements can be determined based on a time integration quantity, which is a change in brightness in the moving-state vide signal integrated with respect to time, and the quantity of light in stationary state, thus a difference in brightness can be preferably reduced in consideration of the human visual perception characteristic to inhibit flicker appropriately.

The moving-state video signal passed through the input consists of a plurality of color signals, the offset set by the setting elements is determined for each of the color signals, and the generator generates the output video signal for each color signal based on the offset determined for each color signal. Thus a difference in brightness between moving and stationary states can be corrected for each color signal to inhibit flicker on a color image display.

5:16-30

The apparatus further comprises a frame buffer for storing the brightness information of the input wire-frame model as the previous brightness, and characterized by that the storage portion stores the offset as table information based on a relation between the previous brightness stored in the frame buffer and the brightness of the next input wire-frame model, thus, flicker in a moving state can be advantageously inhibited without providing separate determining units for moving and stationary states.

5:31-39

In another category, the present invention is a flicker inhibition method for inhibiting flicker caused by a difference in brightness when an input wire-frame model is displayed by a liquid crystal cell. The method is characterized by storing a relation between brightness in a stationary state in which a wire-frame model having a predetermined gray scale is displayed on a particular pixel across a plurality of frames and brightness in a moving state in which the wire-frame model having the predetermined gray scale changes frame to frame with respect to the particular pixel, applying an offset based on the stored relation to the gray scale of the wire-frame model if the input wire-frame model is in a moving state, and driving the liquid crystal cell based on the gray scale to which the offset is applied to display the wire-frame model.

5:51-65

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DETERMINATOR  
FOR DETERMINING AN OUTPUT BRIGHTNESS LEVEL” (cont'd)**

Viewing the present invention as a liquid crystal driving method, the liquid crystal driving method of the present invention is characterized by the steps of storing first brightness information for an input pixel in a frame buffer, and applying, based on second brightness information for the next input pixel and the first brightness information stored in the frame buffer, an offset for making the time integration quantity of a brightness change substantially equal to an ideal light quantity which is brightness in a stationary state to the second brightness information. The steps further include the outputting of the second brightness information to which the offset is applied to a driving circuit for driving an liquid crystal cell, and storing the second brightness information for the input pixel in a frame buffer. This liquid crystal driving method allows the inhibition of flicker by using a simple apparatus without globally determining whether a model is moving or stationary.

6:11-27

The offset applying step is characterized by the step of reading a pre-stored offset based on the relation between the first and second brightness information and applying the read offset to the second brightness information.

6:37-40

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DETERMINATOR FOR DETERMINING AN OUTPUT BRIGHTNESS LEVEL” (cont'd)**

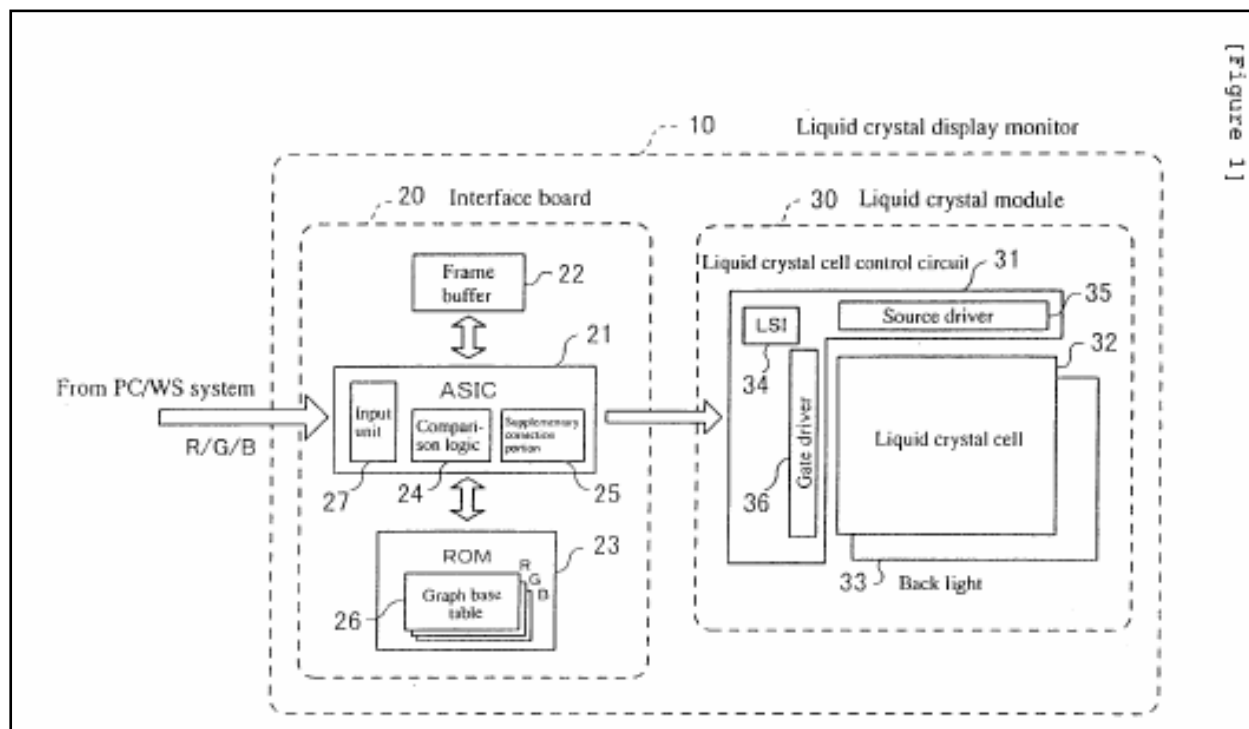


FIG. 1 is a drawing for showing the overall configuration of a liquid crystal display according to an embodiment of the present invention. Reference number 10 denotes a liquid

6:51-53

The I/F board 20 comprises a input unit 27 for inputting video data from a host such as a PC/WS system, a comparison logic 24 for comparing the previous brightness with the next brightness for an input video signal, and an Application-Specific Integrate Circuit (ASIC) 21 including a logic having units such as a supplementary correction portion 25 for performing a supplementary correction. The I/F board 20 also comprises a frame buffer 22 for temporarily storing the input video signal and read-only memory (ROM) 23 containing information needed for the operation of the ASIC 21. The frame buffer 22 stores input video signal value

6:66-67,  
7:1-9

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DETERMINATOR FOR DETERMINING AN OUTPUT BRIGHTNESS LEVEL” (cont'd)**

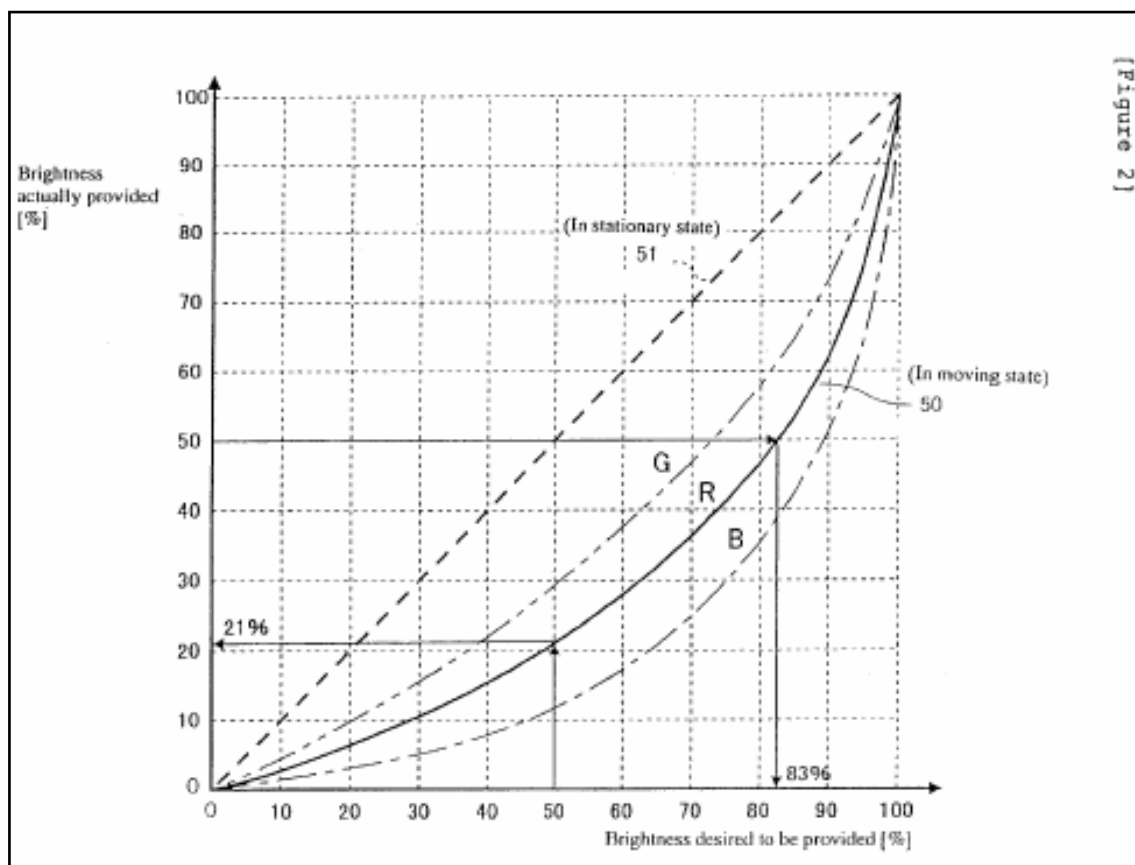


FIG. 2 is a graph showing an example of the brightness of a wire-frame model moving on the LCD panel used in this embodiment. The horizontal scale indicates brightness (%) desired to be provided and the vertical scale indicates brightness (%) actually provided in the Figure. The dashed line 51 indicates the relationship between the desired brightness and actual brightness of the model in a stationary state. The solid line 50 indicates the relationship between the desired brightness and actual brightness of the model in a moving state for an R (red) signal. The alternate long and short two dashes line indicates a G (green) signal in the moving state and the alternate long and short one dash line indicates a B (blue) signal in the moving state. The characteristics in the moving state vary from LCD panel to LCD panel.

7:31-45

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DETERMINATOR FOR DETERMINING AN OUTPUT BRIGHTNESS LEVEL” (cont'd)**

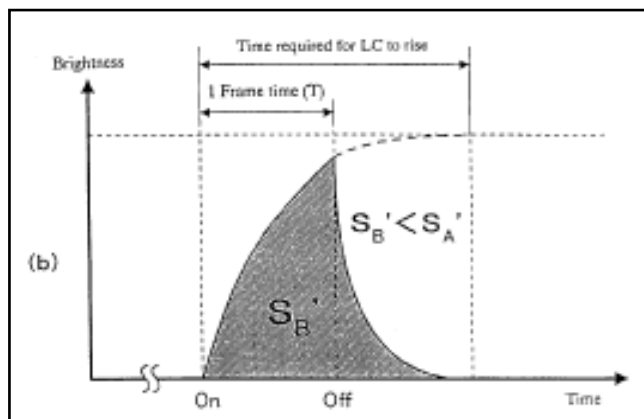
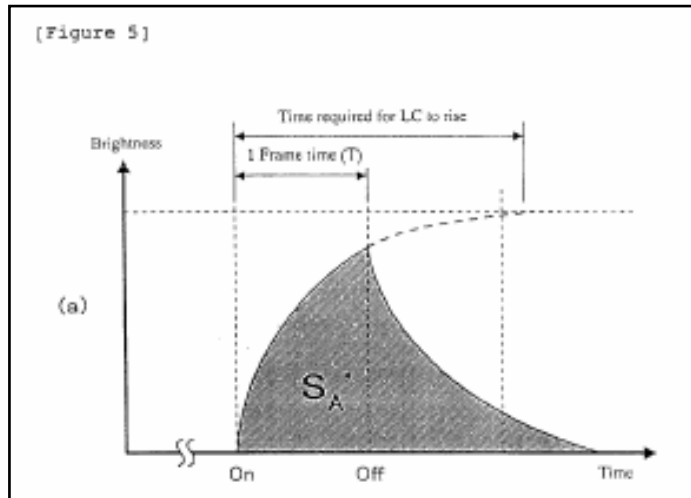
61 Model (Magnitude of flicker)	62 Response rising time	63 Response falling time	64 Light quantity ratio (to ideal LC)	65 Brightness ratio of drawing in moving state to that in stationary state
Model A (○)	20.3ms	21.6ms	1.02 : 1	1.0 : 1
Model B (×)	18.5ms	10.0ms	0.81 : 1	0.8 : 1
Model C (△)	10.0ms	4.5ms	0.85 : 1	0.9 : 1
Model D (×)	19.9ms	7.9ms	0.73 : 1	0.7 : 1
Model E (×)	43.2ms	34.3ms	0.53 : 1	0.3 : 1

[Figure 3]

FIGS. 5A and 5B show the response characteristic represented by brightness versus time when a pixel stays lit up for one frame time (On→Off) in models A, B shown in FIG. 3. Both of the rising and falling of the response of model A

8:41-44

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DETERMINATOR FOR DETERMINING AN OUTPUT BRIGHTNESS LEVEL” (cont'd)**



FIGS. 5A and 5B show the response characteristic represented by brightness versus time when a pixel stays lit up for one frame time (On→Off) in models A, B shown in FIG. 3. Both of the rising and falling of the response of model A

8:41-44

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DETERMINATOR FOR DETERMINING AN OUTPUT BRIGHTNESS LEVEL” (cont'd)**

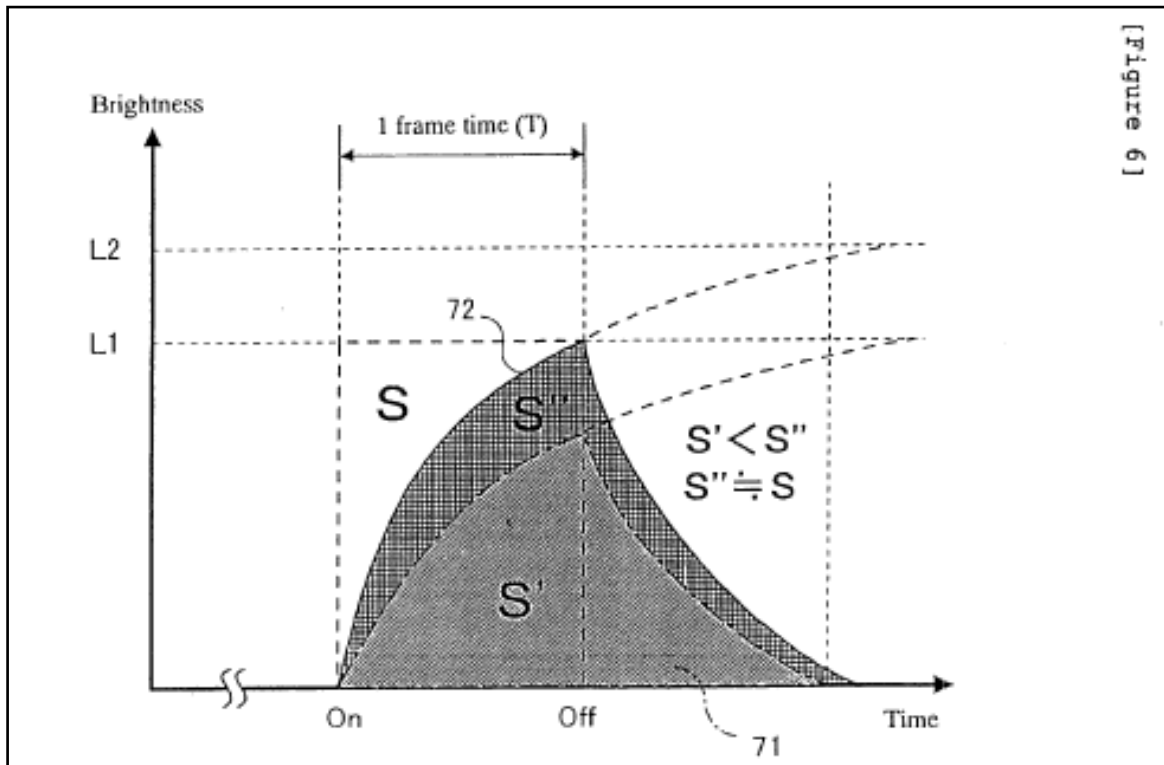


FIG. 6 shows an effect when brightness is set by taking a required offset into account. If the liquid crystal is driven trying to achieve desired brightness L1 as target, only the quantity of light (S') indicated by reference number 71 can be obtained due to the response time of the liquid crystal described above. The quantity of light (S') 71 is much smaller than the quantity of light (S) provided by the ideal response characteristic shown in FIG. 4. On the other hand, if the liquid crystal is driven with the aim of achieving brightness L2 which is larger than the desired brightness of L1, the quantity of light (S'') indicated by reference number 72 can be obtained. By overdriving the LC to brightness L2, the LC reaches L1 in a short response time and the quantity of light (S'') 72 can be obtained which is approximately the same as the quantity of light (S), which would be provided with the ideal response characteristic ( $S'' \approx S$ ). Here, optimum brightness L2 with respect to L1 can be obtained from the data shown in FIG. 2.

9:8-25

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DETERMINATOR FOR DETERMINING AN OUTPUT BRIGHTNESS LEVEL” (cont'd)**

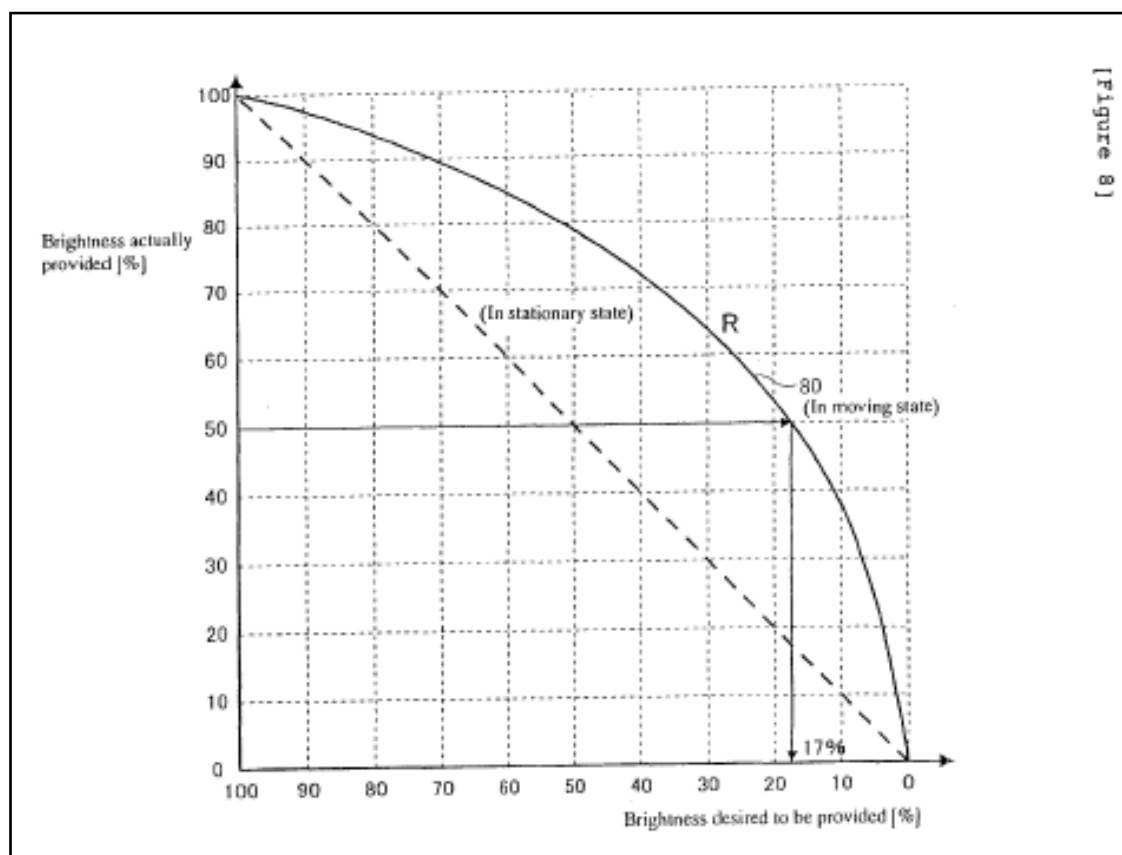


FIG. 8 is a graph showing brightness desired to be provided versus brightness provided actually when brightness falls. The liquid crystal in the example in FIG. 8 has brightness which falls with exhibiting a characteristic similar to the rising characteristic shown in FIG. 2. Accordingly, the line 80 indicating a moving state shown in FIG. 8 is the vertically-flipped curve of the line 50 in a moving state shown in FIG. 2. Tick mark labels on the horizontal scale are also inverted. As can be seen from the graph, when the brightness actually provided is 50%, the brightness desired to be provided is 17%. This matches the value when the previous brightness is 100 and the next brightness is 50 in the table in FIG. 7. That is, the moving state line 80 in FIG. 8 exactly indicates the fall of the previous brightness from 100% in FIG. 7.

10:26-40

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DETERMINATOR  
FOR DETERMINING AN OUTPUT BRIGHTNESS LEVEL” (cont'd)**

As described above, the embodiment is configured to store offsets in table form based on the relation between a brightness level in a stationary state and that in a moving state in order to obtain an ideal quantity of light. Thus, even during the movement of a display image on the LCD screen, the image can be displayed virtually the same brightness to the eye as in its stationary state, thereby inhibiting flicker on the screen.

In addition, the embodiment is configured to store the previous brightness level (gray scale value) in the frame buffer 22 and a supplementary correction is made by the ASIC 21 using the data in the graph base table 26 based on the relation between the brightness level of the next video data and the previous brightness level. Thus, whether a wire-frame model is moving or stationary is not required to be determined. Instead, the movement of the model can be determined from a difference between the determined brightness and the previous brightness. As a result, flicker can be inhibited by a simple circuit configuration.

10:49-67

## **INTRINSIC EVIDENCE FOR DISPUTED TERM “BRIGHTNESS LEVEL”**

The “ideal quantity of light” herein is, to take an example, the quantity of light based on a response characteristic which provides a target brightness level at a time point at which the frame is turned on and provides a brightness level of zero at the time point at which the frame is turned off on a display device in which each pixel is driven for each frame. The brightness level can be represented as a target brightness value by a gray scale and considered as an indication of the characteristic of human visual sensation to brightness. In addition, a brightness change can be considered as a response characteristic depending on the types of liquid

4:47-52

In another category, the present invention is a flicker inhibition method for inhibiting flicker caused by a difference in brightness when an input wire-frame model is displayed by a liquid crystal cell. The method is characterized by storing a relation between brightness in a stationary state in which a wire-frame model having a predetermined gray scale is displayed on a particular pixel across a plurality of frames and brightness in a moving state in which the wire-frame model having the predetermined gray scale changes frame to frame with respect to the particular pixel, applying an offset based on the stored relation to the gray scale of the wire-frame model if the input wire-frame model is in a moving state, and driving the liquid crystal cell based on the gray scale to which the offset is applied to display the wire-frame model.

5:51-65

# INTRINSIC EVIDENCE FOR DISPUTED TERM “BRIGHTNESS LEVEL” (cont'd)

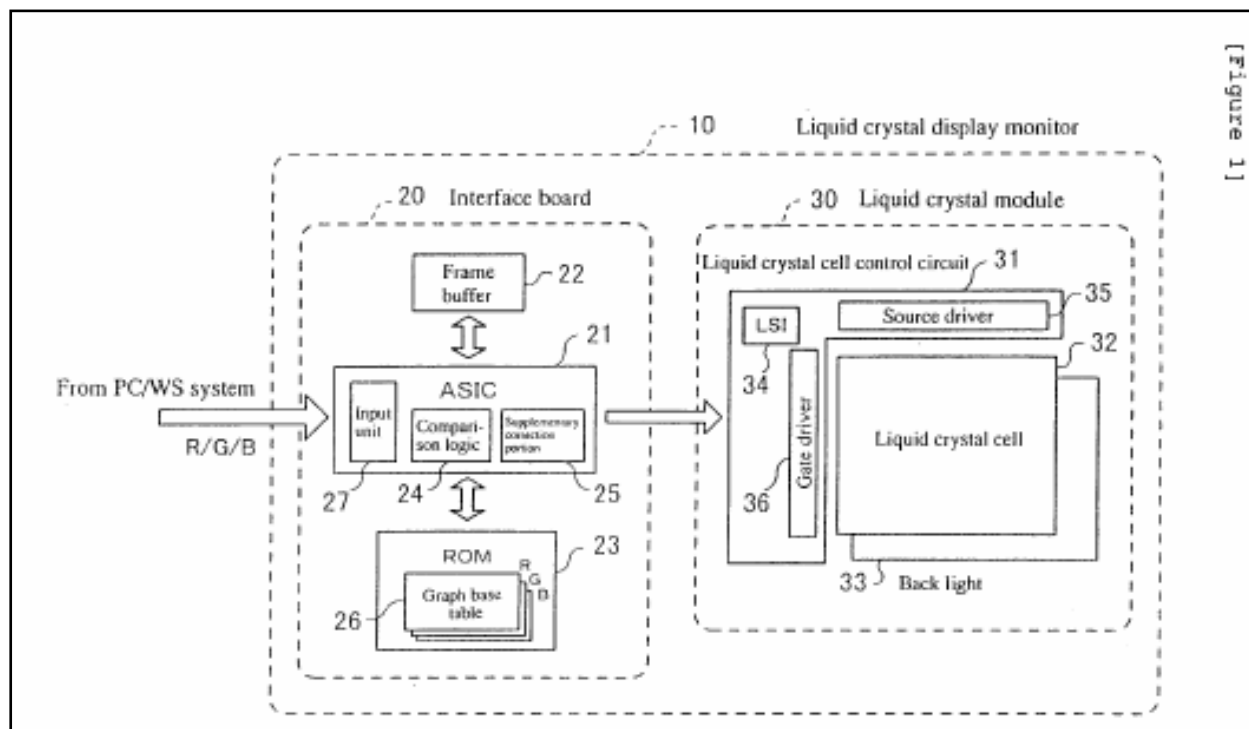


FIG. 1 is a drawing for showing the overall configuration of a liquid crystal display according to an embodiment of the present invention. Reference number 10 denotes a liquid

6:51-53

The I/F board 20 comprises a input unit 27 for inputting video data from a host such as a PC/WS system, a comparison logic 24 for comparing the previous brightness with the next brightness for an input video signal, and an Application-Specific Integrate Circuit (ASIC) 21 including a logic having units such as a supplementary correction portion 25 for performing a supplementary correction. The I/F board 20 also comprises a frame buffer 22 for temporarily storing the input video signal and read-only memory (ROM) 23 containing information needed for the operation of the ASIC 21. The frame buffer 22 stores input video signal value

6:66-67,  
7:1-9

## INTRINSIC EVIDENCE FOR DISPUTED TERM “BRIGHTNESS LEVEL” (cont'd)

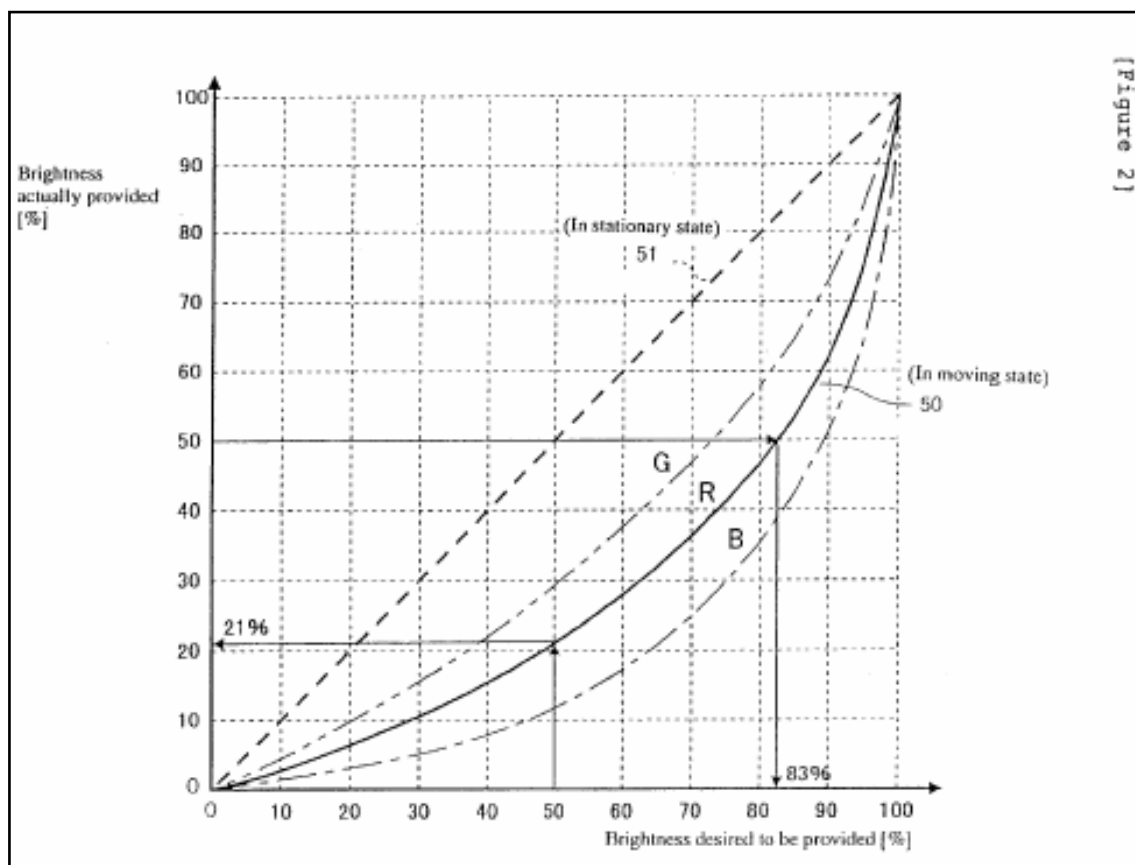


FIG. 2 is a graph showing an example of the brightness of a wire-frame model moving on the LCD panel used in this embodiment. The horizontal scale indicates brightness (%) desired to be provided and the vertical scale indicates brightness (%) actually provided in the Figure. The dashed line 51 indicates the relationship between the desired brightness and actual brightness of the model in a stationary state. The solid line 50 indicates the relationship between the desired brightness and actual brightness of the model in a moving state for an R (red) signal. The alternate long and short two dashes line indicates a G (green) signal in the moving state and the alternate long and short one dash line indicates a B (blue) signal in the moving state. The characteristics in the moving state vary from LCD panel to LCD panel.

7:31-45

## INTRINSIC EVIDENCE FOR DISPUTED TERM “BRIGHTNESS LEVEL” (cont'd)

[Figure 7]

26 (Graph base table)

Next brightness Previous brightness	0	10	20	30	40	50	60	70	80	90	100
0	0	28	48	63	74	83	88	93	96	98	100
10	0	10	30	45	56	65	70	75	80	90	100
20	0	10	20	35	46	55	60	70	80	90	100
30	0	10	20	30	41	50	60	70	80	90	100
40	0	10	20	30	40	50	60	70	80	90	100
50	0	10	20	30	40	50	60	70	80	90	100
60	0	10	20	30	40	50	60	70	80	90	100
70	0	10	20	30	40	50	59	70	80	90	100
80	0	10	20	30	40	45	54	65	80	90	100
90	0	10	20	25	30	35	44	55	70	90	100
100	0	2	4	7	12	17	26	38	52	72	100

FIG. 7 is a table showing a relation between brightness L1 and L2 and represents the content of the graph base table 26 stored in the ROM 23 shown in FIG. 1. The content of the graph base table 26 shown in FIG. 7 represents a relation between the previous brightness and the next brightness for the LC cell 32 having the characteristic shown in FIG. 2, by taking the effect shown in FIG. 6 into consideration. The previous brightness can be obtained from a video signal input through the ASIC21 shown in FIG. 1 and stored in the frame buffer 22. The next brightness can be obtained from the next video signal input to the ASIC 21. The graph base table 26 is constructed for each of the R, G, B color signals and the values in the table vary depending on the characteristic of the LC cell 32.

9:26-39

# INTRINSIC EVIDENCE FOR DISPUTED TERM “BRIGHTNESS LEVEL” (cont'd)

[Figure 7]

26 (Graph base table)

Next brightness Previous brightness	0	10	20	30	40	50	60	70	80	90	100
0	0	28	48	63	74	83	88	93	96	98	100
10	0	10	30	45	56	65	70	75	80	90	100
20	0	10	20	35	46	55	60	70	80	90	100
30	0	10	20	30	41	50	60	70	80	90	100
40	0	10	20	30	40	50	60	70	80	90	100
50	0	10	20	30	40	50	60	70	80	90	100
60	0	10	20	30	40	50	60	70	80	90	100
70	0	10	20	30	40	50	59	70	80	90	100
80	0	10	20	30	40	45	54	65	80	90	100
90	0	10	20	25	30	35	44	55	70	90	100
100	0	2	4	7	12	17	26	38	52	72	100

The first row of the graph base table 26 shown in FIG. 7 indicates brightness output for the next brightness when the previous brightness is 0 and match the readings of the R signal in the moving state line 50 in the graph shown in FIG. 2. For example, if the next brightness is “10”, find a value

9:40-44

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41. In this embodiment, if a difference between the previous brightness and the next brightness is greater than an offset, the next brightness is output without change. For example,

9:56-58

**INTRINSIC EVIDENCE FOR DISPUTED TERM “BRIGHTNESS LEVEL” (cont'd)**

On the other hand, when brightness falls from a certain halftone to another halftone, the offset is subtracted from the previous brightness. The example in FIG. 7 shows a case where the characteristic of the LC cell 32 when brightness rises (the cell is turned on) is the same as that when the brightness falls (the cell is turned off). In this example, if the previous brightness is 100 and the next brightness is 10, the output value will be  $100 - 98 = 2$ . The value “98” is equal to the value when the previous brightness is 0 and the next brightness is 90 in FIG. 7. Similarly, if the previous brightness is 100 and the next brightness is 20, then  $100 - 96 = 4$ . If the previous brightness is 90 and the next brightness is 30, then  $100 - 75 = 25$ . The value “75” is equal to the value when the previous brightness is 10 and the next brightness is 70 in FIG. 7. Similarly, if the previous brightness is 90 and the next brightness is 40, then  $100 - 70 = 30$ . The value “70” is equal to the value when the previous brightness is 10 and the next brightness is 60 in FIG. 7.

9:64-67,  
10:1-13

## INTRINSIC EVIDENCE FOR DISPUTED TERM “BRIGHTNESS LEVEL” (cont'd)

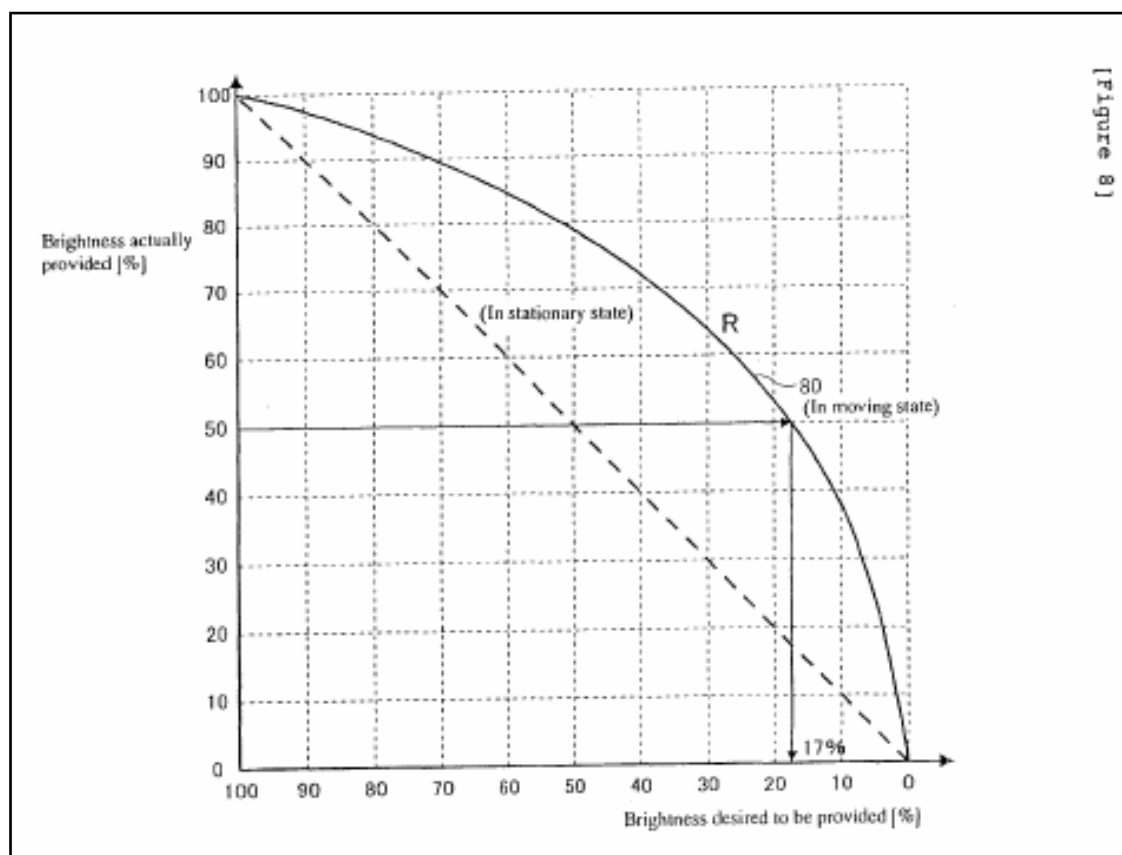


FIG. 8 is a graph showing brightness desired to be provided versus brightness provided actually when brightness falls. The liquid crystal in the example in FIG. 8 has brightness which falls with exhibiting a characteristic similar to the rising characteristic shown in FIG. 2. Accordingly, the line 80 indicating a moving state shown in FIG. 8 is the vertically-flipped curve of the line 50 in a moving state shown in FIG. 2. Tick mark labels on the horizontal scale are also inverted. As can be seen from the graph, when the brightness actually provided is 50%, the brightness desired to be provided is 17%. This matches the value when the previous brightness is 100 and the next brightness is 50 in the table in FIG. 7. That is, the moving state line 80 in FIG. 8 exactly indicates the fall of the previous brightness from 100% in FIG. 7.

10:26-40

**INTRINSIC EVIDENCE FOR DISPUTED TERM “BRIGHTNESS  
LEVEL” (cont'd)**

In addition, the embodiment is configured to store the previous brightness level (gray scale value) in the frame buffer 22 and a supplementary correction is made by the ASIC 21 using the data in the graph base table 26 based on the relation between the brightness level of the next video data and the previous brightness level. Thus, whether a

10:57-62

**EXHIBIT \_\_\_\_\_**  
**U.S. PATENT NO. 6,778,160**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 1**

1. A liquid crystal display, comprising:  
an input logic for inputting a video signal from a host;  
a storage for storing the previous brightness level of the video signal input through said input logic;  
a determinator for determining an output brightness level based on the previous brightness level stored in said storage and the next brightness level of the next video signal input to said input logic so as to make a time integration quantity of a brightness change substantially equal to an ideal quantity of light in a stationary state with respect to the next brightness level; and  
a driver for driving an image displaying liquid crystal cell based on said output brightness level determined by said determination logic.

**LGD's Claim Construction**

**so as to make a time integration quantity of a brightness change substantially equal to an ideal quantity of light in a stationary state with respect to the next brightness level<sup>1</sup>**  
- so that the quantity of light based on the actual response characteristic of the liquid crystal cell is substantially equal to the quantity of light based on the ideal response characteristic of the liquid crystal cell when the liquid crystal cell is provided with the next brightness level during the next time increment and the previous brightness level before and after the next time increment.

<sup>1</sup> Disputed Term "brightness level" also appears in asserted Claim 2 in the same context.

**INTRINSIC EVIDENCE FOR DISPUTED TERM “SO AS TO MAKE  
A TIME INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE  
SUBSTANTIALLY EQUAL TO AN IDEAL QUANTITY OF LIGHT  
IN A STATIONARY STATE WITH RESPECT TO THE NEXT  
BRIGHTNESS LEVEL ”**

The term “response time” used in the industry refers to the sum of (1) time required to reverse color by applying a voltage to a liquid crystal cell and (2) time required to restore the original color by the removal of the applied voltage. The term “frame” used in the industry represents the

1:39-43

In Published Unexamined Japanese Patent Application No. 2-153687, a LCD is provided which is configured to discriminate between a static image area having less motion and a fast-moving area and apply a signal process only to the moving area to emphasize time-based changes in an image, thereby improving response time in the image area where better response time is required to reduce visual persistence and noise.

In Published Unexamined Japanese Patent Application No. 4-365094, a LCD is provided which is configured to be driven by reading pre-stored optimum image data according to the direction and degree of a change when the image data changes, thereby allowing the LCD to rapidly follow the fast-changing image.

In Published Unexamined Japanese Patent Application No. 6-62355, a technology is disclosed which superposes a difference component between fields or frames on a video

1:50-67

In Published Unexamined Japanese Patent Application No. 7-56532, a technology is disclosed which provides table memory containing a table of image increase/decrease values and drive a liquid crystal panel (liquid crystal cell) by performing an addition/subtraction in order to improve response changes due to changes in the gray scale in the liquid crystal panel. However, the amount to be added or subtracted is expressed only by the word “optimum” and no specific amount is disclosed.

2:4-12

**INTRINSIC EVIDENCE FOR DISPUTED TERM “SO AS TO MAKE A TIME INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE SUBSTANTIALLY EQUAL TO AN IDEAL QUANTITY OF LIGHT IN A STATIONARY STATE WITH RESPECT TO THE NEXT BRIGHTNESS LEVEL ” (cont'd)**

The “ideal quantity of light” herein is, to take an example, the quantity of light based on a response characteristic which provides a target brightness level at a time point at which the frame is turned on and provides a brightness level of zero at the time point at which the frame is turned off on a display device in which each pixel is driven for each frame. The brightness level can be represented as a target brightness value by a gray scale and considered as an indication of the characteristic of human visual sensation to brightness. In addition, a brightness change can be considered as a response characteristic depending on the types of liquid crystal cells (liquid crystal panels). Quantity of light is considered as a time integration quantity of a brightness change and can be expressed as brightness\_time, if the brightness is constant. The representation “substantially

4:42-56

The determinant is characterized by comprising a table for storing a brightness level determined by the characteristic of a liquid crystal cell according to a relation between the previous brightness level and the next brightness level, and determining an output brightness level by modifying the next brightness level based on the brightness level read from the table. With this configuration, flicker due to changes in

4:50-67

**INTRINSIC EVIDENCE FOR DISPUTED TERM “SO AS TO MAKE A TIME INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE SUBSTANTIALLY EQUAL TO AN IDEAL QUANTITY OF LIGHT IN A STATIONARY STATE WITH RESPECT TO THE NEXT BRIGHTNESS LEVEL ” (cont'd)**

The offset set by the setting elements can be determined based on a time integration quantity, which is a change in brightness in the moving-state vide signal integrated with respect to time, and the quantity of light in stationary state, thus a difference in brightness can be preferably reduced in consideration of the human visual perception characteristic to inhibit flicker appropriately.

The moving-state video signal passed through the input consists of a plurality of color signals, the offset set by the setting elements is determined for each of the color signals, and the generator generates the output video signal for each color signal based on the offset determined for each color signal. Thus a difference in brightness between moving and stationary states can be corrected for each color signal to inhibit flicker on a color image display.

5:16-30

The moving state brightness used for storing the relation is the brightness when the particular pixel changes back to the off state one frame after it is driven from the off state to the on state during the passage of the wire-frame model over the particular pixel.

Furthermore, the brightness in the moving state which is used when the relation is stored is the quantity of light equal to the brightness change integrated with respect to time.

5:66-67,  
6:1-6

Viewing the present invention as a liquid crystal driving method, the liquid crystal driving method of the present invention is characterized by the steps of storing first brightness information for an input pixel in a frame buffer, and applying, based on second brightness information for the next input pixel and the first brightness information stored in the frame buffer, an offset for making the time integration quantity of a brightness change substantially equal to an ideal light quantity which is brightness in a stationary state to the second brightness information. The steps further include the outputting of the second brightness information to which the offset is applied to a driving circuit for driving an liquid crystal cell, and storing the second brightness information for the input pixel in a frame buffer. This liquid crystal driving method allows the inhibition of flicker by using a simple apparatus without globally determining whether a model is moving or stationary.

6:11-27

**INTRINSIC EVIDENCE FOR DISPUTED TERM “SO AS TO MAKE A TIME INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE SUBSTANTIALLY EQUAL TO AN IDEAL QUANTITY OF LIGHT IN A STATIONARY STATE WITH RESPECT TO THE NEXT BRIGHTNESS LEVEL ” (cont'd)**

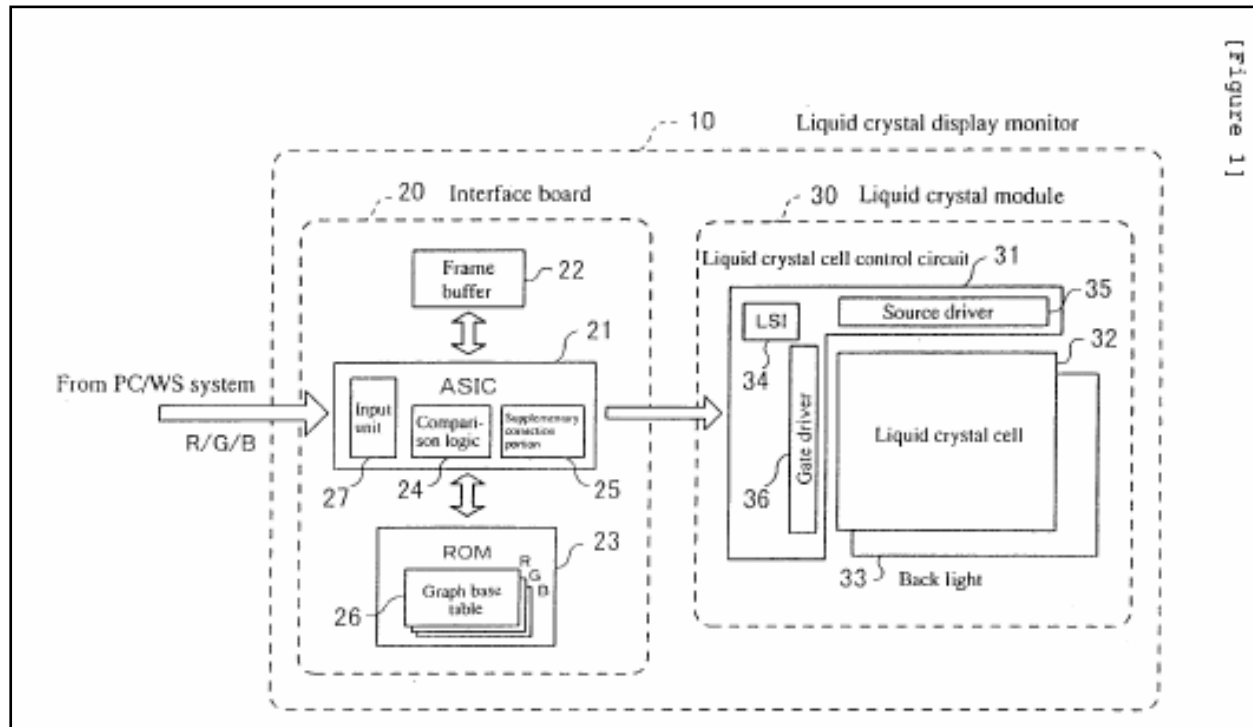


FIG. 1 is a drawing for showing the overall configuration of a liquid crystal display according to an embodiment of the present invention. Reference number 10 denotes a liquid

The I/F board 20 comprises a input unit 27 for inputting video data from a host such as a PC/WS system, a comparison logic 24 for comparing the previous brightness with the next brightness for an input video signal, and an Application-Specific Integrate Circuit (ASIC) 21 including a logic having units such as a supplementary correction portion 25 for performing a supplementary correction. The I/F board 20 also comprises a frame buffer 22 for temporarily storing the input video signal and read-only memory (ROM) 23 containing information needed for the operation of the ASIC 21. The frame buffer 22 stores input video signal value

**INTRINSIC EVIDENCE FOR DISPUTED TERM “SO AS TO MAKE A TIME INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE SUBSTANTIALLY EQUAL TO AN IDEAL QUANTITY OF LIGHT IN A STATIONARY STATE WITH RESPECT TO THE NEXT BRIGHTNESS LEVEL ” (cont'd)**

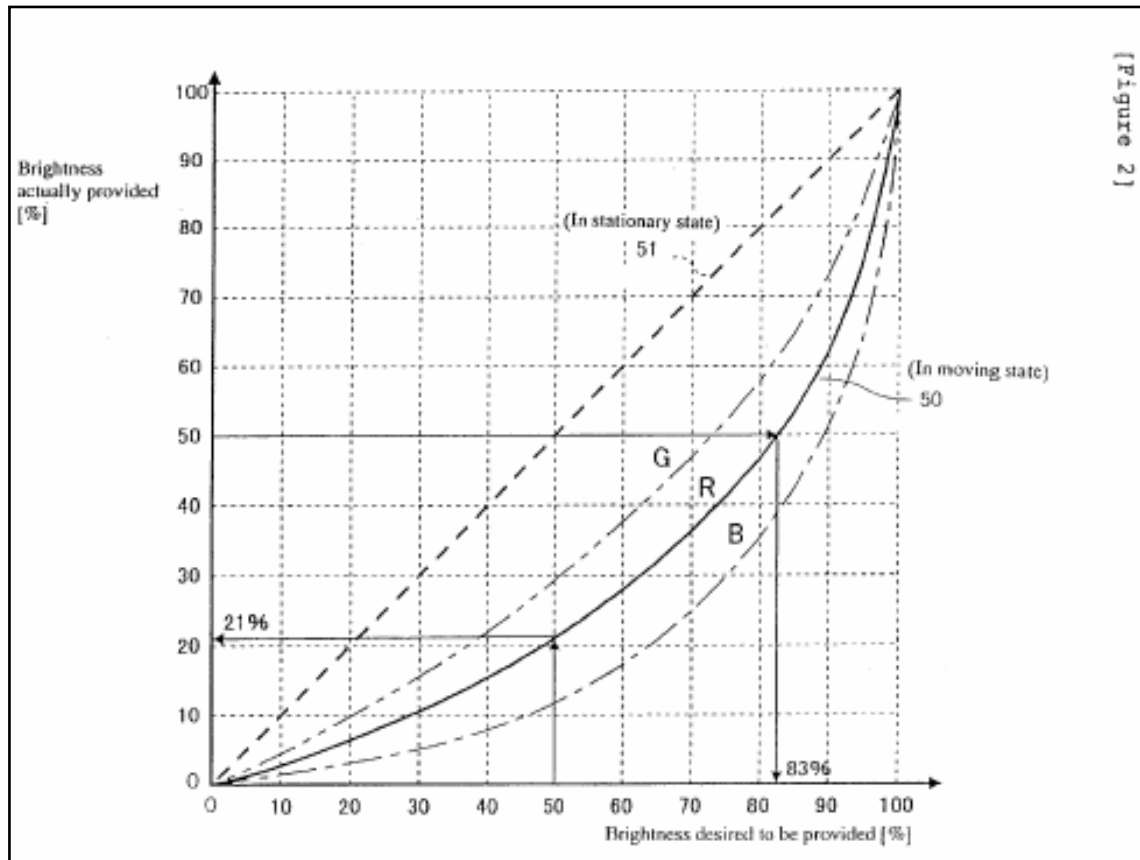


FIG. 2 is a graph showing an example of the brightness of a wire-frame model moving on the LCD panel used in this embodiment. The horizontal scale indicates brightness (%) desired to be provided and the vertical scale indicates brightness (%) actually provided in the Figure. The dashed line 51 indicates the relationship between the desired brightness and actual brightness of the model in a stationary state. The solid line 50 indicates the relationship between the desired brightness and actual brightness of the model in a moving state for an R (red) signal. The alternate long and short two dashes line indicates a G (green) signal in the moving state and the alternate long and short one dash line indicates a B (blue) signal in the moving state. The characteristics in the moving state vary from LCD panel to LCD panel.

**INTRINSIC EVIDENCE FOR DISPUTED TERM “SO AS TO MAKE A TIME INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE SUBSTANTIALLY EQUAL TO AN IDEAL QUANTITY OF LIGHT IN A STATIONARY STATE WITH RESPECT TO THE NEXT BRIGHTNESS LEVEL ” (cont'd)**

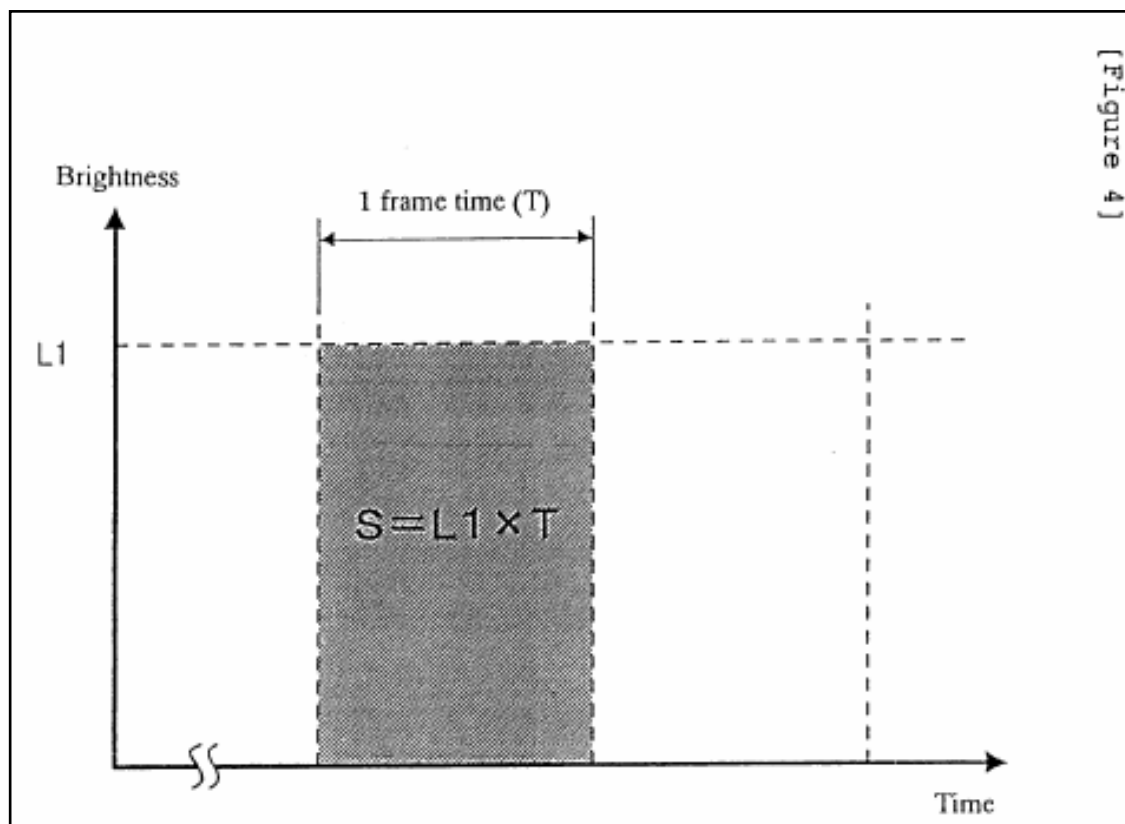


FIG. 4 shows the response characteristic of an ideal liquid crystal and indicates the state in which a particular pixel is kept lit up at a brightness of L1, that is in a stationary state. Here, the quantity of light (S) emitted in one frame time (T) is equal to  $L1 \times T$  (i.e. brightness  $\times$  time) as shown in the shaded area in FIG. 4.

8:35-40

**INTRINSIC EVIDENCE FOR DISPUTED TERM “SO AS TO MAKE A TIME INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE SUBSTANTIALLY EQUAL TO AN IDEAL QUANTITY OF LIGHT IN A STATIONARY STATE WITH RESPECT TO THE NEXT BRIGHTNESS LEVEL ” (cont'd)**

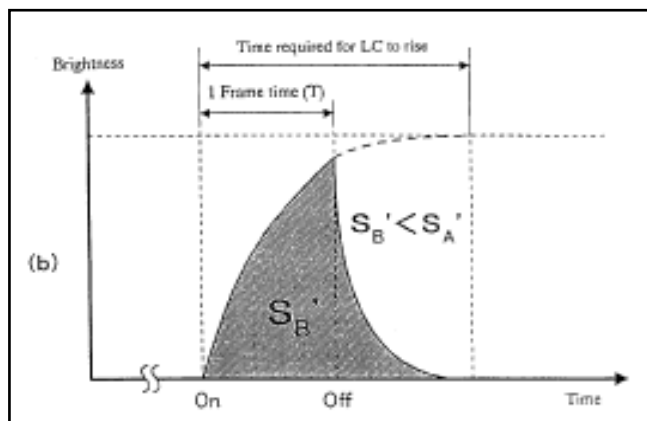
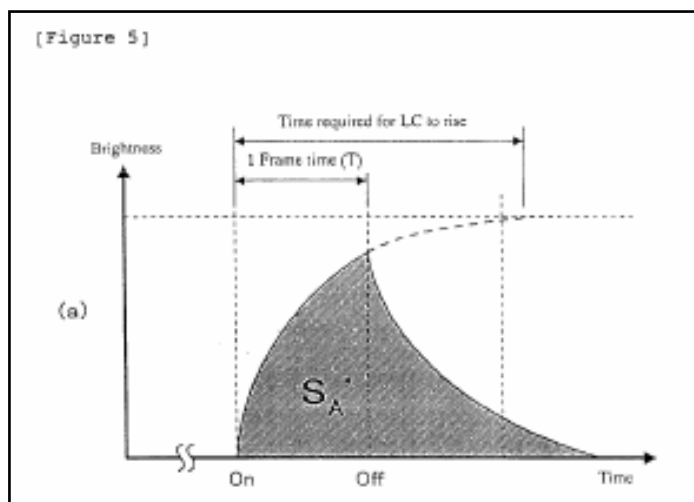
61 Model (Magnitude of flicker)	62 Response rising time	63 Response falling time	64 Light quantity ratio (to ideal LC)	65 Brightness ratio of drawing in moving state to that in stationary state
Model A (○)	20.3ms	21.6ms	1.02 : 1	1.0 : 1
Model B (×)	18.5ms	10.0ms	0.81 : 1	0.8 : 1
Model C (△)	10.0ms	4.5ms	0.85 : 1	0.9 : 1
Model D (×)	19.9ms	7.9ms	0.73 : 1	0.7 : 1
Model E (×)	43.2ms	34.3ms	0.53 : 1	0.3 : 1

[Figure 3]

FIGS. 5A and 5B show the response characteristic represented by brightness versus time when a pixel stays lit up for one frame time (On→Off) in models A, B shown in FIG. 3. Both of the rising and falling of the response of model A

8:41-44

**INTRINSIC EVIDENCE FOR DISPUTED TERM “SO AS TO MAKE A TIME INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE SUBSTANTIALLY EQUAL TO AN IDEAL QUANTITY OF LIGHT IN A STATIONARY STATE WITH RESPECT TO THE NEXT BRIGHTNESS LEVEL ” (cont'd)**



FIGS. 5A and 5B show the response characteristic represented by brightness versus time when a pixel stays lit up for one frame time (On→Off) in models A, B shown in FIG. 3. Both of the rising and falling of the response of model A

8:41-44

**INTRINSIC EVIDENCE FOR DISPUTED TERM “SO AS TO MAKE A TIME INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE SUBSTANTIALLY EQUAL TO AN IDEAL QUANTITY OF LIGHT IN A STATIONARY STATE WITH RESPECT TO THE NEXT BRIGHTNESS LEVEL ” (cont'd)**

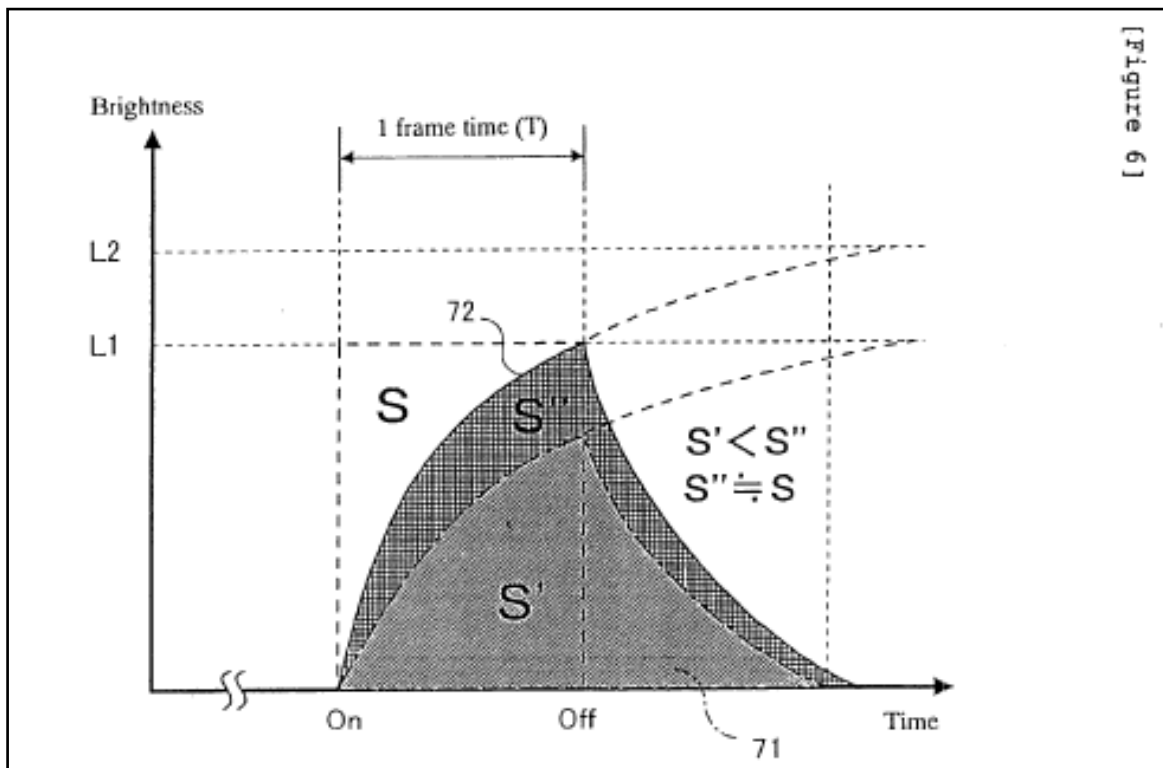


FIG. 6 shows an effect when brightness is set by taking a required offset into account. If the liquid crystal is driven trying to achieve desired brightness L1 as target, only the quantity of light (S') indicated by reference number 71 can be obtained due to the response time of the liquid crystal described above. The quantity of light (S') 71 is much smaller than the quantity of light (S) provided by the ideal response characteristic shown in FIG. 4. On the other hand, if the liquid crystal is driven with the aim of achieving brightness L2 which is larger than the desired brightness of L1, the quantity of light (S'') indicated by reference number 72 can be obtained. By overdriving the LC to brightness L2, the LC reaches L1 in a short response time and the quantity of light (S'') 72 can be obtained which is approximately the same as the quantity of light (S), which would be provided with the ideal response characteristic ( $S'' \approx S$ ). Here, optimum brightness L2 with respect to L1 can be obtained from the data shown in FIG. 2.

9:8-25

**INTRINSIC EVIDENCE FOR DISPUTED TERM “SO AS TO MAKE A TIME INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE SUBSTANTIALLY EQUAL TO AN IDEAL QUANTITY OF LIGHT IN A STATIONARY STATE WITH RESPECT TO THE NEXT BRIGHTNESS LEVEL ” (cont'd)**

[Figure 7]

26 (Graph base table)

Next brightness Previous brightness	0	10	20	30	40	50	60	70	80	90	100
0	0	28	48	63	74	83	88	93	96	98	100
10	0	10	30	45	56	65	70	75	80	90	100
20	0	10	20	35	46	55	60	70	80	90	100
30	0	10	20	30	41	50	60	70	80	90	100
40	0	10	20	30	40	50	60	70	80	90	100
50	0	10	20	30	40	50	60	70	80	90	100
60	0	10	20	30	40	50	60	70	80	90	100
70	0	10	20	30	40	50	59	70	80	90	100
80	0	10	20	30	40	45	54	65	80	90	100
90	0	10	20	25	30	35	44	55	70	90	100
100	0	2	4	7	12	17	26	38	52	72	100

FIG. 7 is a table showing a relation between brightness L1 and L2 and represents the content of the graph base table 26 stored in the ROM 23 shown in FIG. 1. The content of the graph base table 26 shown in FIG. 7 represents a relation between the previous brightness and the next brightness for the LC cell 32 having the characteristic shown in FIG. 2, by taking the effect shown in FIG. 6 into consideration. The previous brightness can be obtained from a video signal input through the ASIC21 shown in FIG. 1 and stored in the frame buffer 22. The next brightness can be obtained from the next video signal input to the ASIC 21. The graph base table 26 is constructed for each of the R, G, B color signals and the values in the table vary depending on the characteristic of the LC cell 32.

9:26-39

**INTRINSIC EVIDENCE FOR DISPUTED TERM “SO AS TO MAKE A TIME INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE SUBSTANTIALLY EQUAL TO AN IDEAL QUANTITY OF LIGHT IN A STATIONARY STATE WITH RESPECT TO THE NEXT BRIGHTNESS LEVEL ” (cont'd)**

[Figure 7]

26 (Graph base table)

Next brightness \ Previous brightness	0	10	20	30	40	50	60	70	80	90	100
0	0	28	48	63	74	83	88	93	96	98	100
10	0	10	30	45	56	65	70	75	80	90	100
20	0	10	20	35	46	55	60	70	80	90	100
30	0	10	20	30	41	50	60	70	80	90	100
40	0	10	20	30	40	50	60	70	80	90	100
50	0	10	20	30	40	50	60	70	80	90	100
60	0	10	20	30	40	50	60	70	80	90	100
70	0	10	20	30	40	50	59	70	80	90	100
80	0	10	20	30	40	45	54	65	80	90	100
90	0	10	20	25	30	35	44	55	70	90	100
100	0	2	4	7	12	17	26	38	52	72	100

The first row of the graph base table 26 shown in FIG. 7 indicates brightness output for the next brightness when the previous brightness is 0 and match the readings of the R signal in the moving state line 50 in the graph shown in FIG. 2. For example, if the next brightness is “10”, find a value

9:40-44

41. In this embodiment, if a difference between the previous brightness and the next brightness is greater than an offset, the next brightness is output without change. For example,

9:56-58

**INTRINSIC EVIDENCE FOR DISPUTED TERM “SO AS TO MAKE A TIME INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE SUBSTANTIALLY EQUAL TO AN IDEAL QUANTITY OF LIGHT IN A STATIONARY STATE WITH RESPECT TO THE NEXT BRIGHTNESS LEVEL ” (cont'd)**

As described above, the embodiment is configured to store offsets in table form based on the relation between a brightness level in a stationary state and that in a moving state in order to obtain an ideal quantity of light. Thus, even during the movement of a display image on the LCD screen, the image can be displayed virtually the same brightness to the eye as in its stationary state, thereby inhibiting flicker on the screen.

In addition, the embodiment is configured to store the previous brightness level (gray scale value) in the frame buffer 22 and a supplementary correction is made by the ASIC 21 using the data in the graph base table 26 based on the relation between the brightness level of the next video data and the previous brightness level. Thus, whether a wire-frame model is moving or stationary is not required to be determined. Instead, the movement of the model can be determined from a difference between the determined brightness and the previous brightness. As a result, flicker can be inhibited by a simple circuit configuration.

10:49-67

**EXHIBIT \_\_\_\_\_**  
**U.S. PATENT NO. 6,778,160**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 1**

1. A liquid crystal display, comprising:  
an input logic for inputting a video signal from a host;  
a storage for storing the previous brightness level of the video signal input through said input logic;  
a determinator for determining an output brightness level based on the previous brightness level stored in said storage and the next brightness level of the next video signal input to said input logic so as to make a time integration quantity of a brightness change substantially equal to an ideal quantity of light in a stationary state with respect to the next brightness level; and  
a driver for driving an image displaying liquid crystal cell based on said output brightness level determined by said determination logic.

**LGD's Claim Construction**

**video signal** - a signal carrying a brightness level from a predetermined range.

**the next brightness level of the next video signal input to said input logic** - the brightness level of the video signal received from the host input to the input logic for the next time increment.

**ASSERTED CLAIM 12**

12. A liquid crystal driving method, comprising the steps of:  
storing first brightness information for an input pixel in a frame buffer;  
applying based on second brightness information for the next input pixel and said first brightness information stored in said frame buffer an offset for making the time integration quantity of a brightness change substantially equal to an ideal light quantity which is the brightness in a stationary state to said second brightness information;  
outputting said second brightness information to which said offset is applied to a driving circuit for driving an liquid crystal cell; and  
storing said second brightness information for the input pixel in a frame buffer.

**first brightness information for an input pixel** - the brightness level of an input signal for a pixel.

**second brightness information for the next input pixel** - the brightness level for the next frame of the input signal for the pixel.

**INTRINSIC EVIDENCE FOR DISPUTED TERM “VIDEO SIGNAL”**

The “ideal quantity of light” herein is, to take an example, the quantity of light based on a response characteristic which provides a target brightness level at a time point at which the frame is turned on and provides a brightness level of zero at the time point at which the frame is turned off on a display device in which each pixel is driven for each frame. The brightness level can be represented as a target brightness value by a gray scale and considered as an indication of the characteristic of human visual sensation to brightness. In addition, a brightness change can be considered as a response characteristic depending on the types of liquid

4:47-52

The video signal input through the input consists of a plurality of color signals and the table in the determinator is provided for each of the color signals so that a brightness level correction for each color can be made with respect to flicker perception of the human eye to reduce a difference in brightness, thereby an easy-on-the-eye liquid crystal display can be provided to the user. While the color signals may be R (red), G (green), B (blue) signals used in displays, other display systems can also be used.

5:7-15

In another category, the present invention is a flicker inhibition method for inhibiting flicker caused by a difference in brightness when an input wire-frame model is displayed by a liquid crystal cell. The method is characterized by storing a relation between brightness in a stationary state in which a wire-frame model having a predetermined gray scale is displayed on a particular pixel across a plurality of frames and brightness in a moving state in which the wire-frame model having the predetermined gray scale changes frame to frame with respect to the particular pixel, applying an offset based on the stored relation to the gray scale of the wire-frame model if the input wire-frame model is in a moving state, and driving the liquid crystal cell based on the gray scale to which the offset is applied to display the wire-frame model.

5:51-65

**INTRINSIC EVIDENCE FOR DISPUTED TERM “VIDEO SIGNAL”**  
**(cont'd)**

The present invention is still further characterized in that the input pixel consists of a plurality color signals and includes the step of storing the first brightness information in the frame buffer stores the first brightness information for each of the color signals, and the step of applying the offset applies the offset to each of the color signals, thus the brightness of each color of a color image consisting of a plurality of color signals can be corrected individually, allowing more adequate flicker inhibition.

6:28:36

**INTRINSIC EVIDENCE FOR DISPUTED TERM “VIDEO SIGNAL”**  
**(cont'd)**

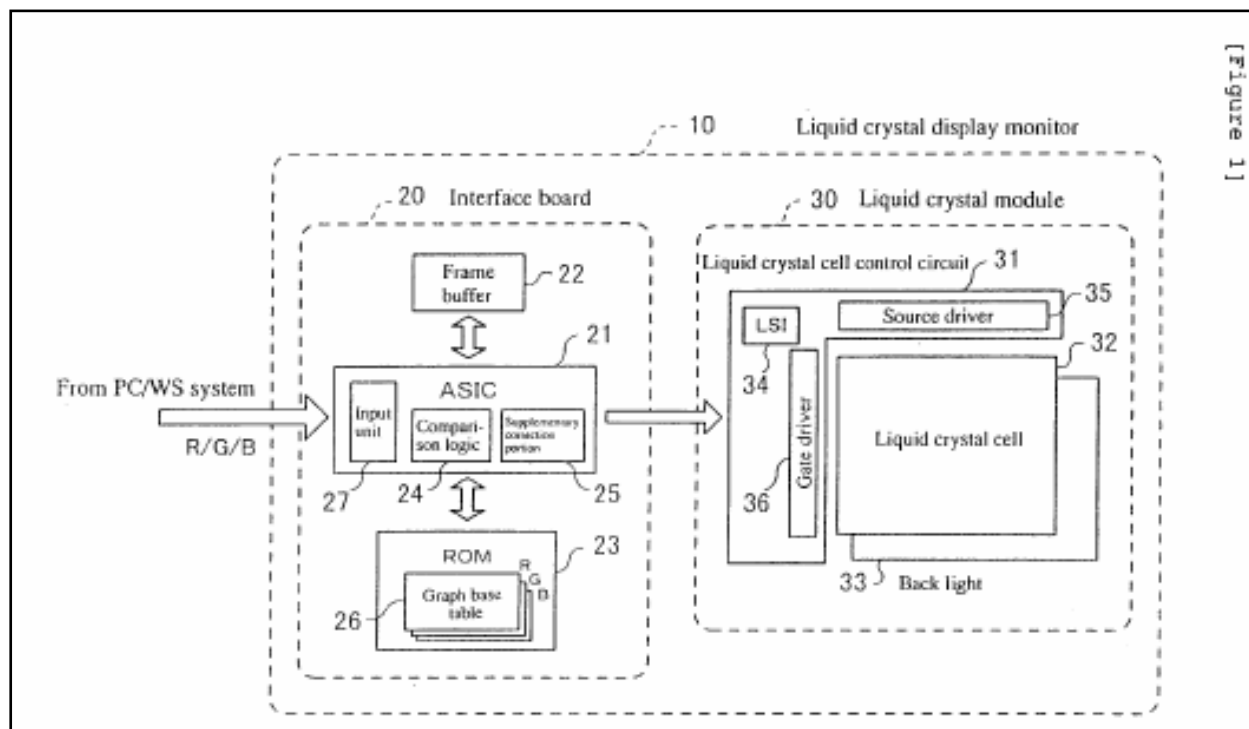


FIG. 1 is a drawing for showing the overall configuration of a liquid crystal display according to an embodiment of the present invention. Reference number 10 denotes a liquid

6:51-53

The I/F board 20 comprises a input unit 27 for inputting video data from a host such as a PC/WS system, a comparison logic 24 for comparing the previous brightness with the next brightness for an input video signal, and an Application-Specific Integrate Circuit (ASIC) 21 including a logic having units such as a supplementary correction portion 25 for performing a supplementary correction. The I/F board 20 also comprises a frame buffer 22 for temporarily storing the input video signal and read-only memory (ROM) 23 containing information needed for the operation of the ASIC 21. The frame buffer 22 stores input video signal value

6:66-67,  
7:1-9

## INTRINSIC EVIDENCE FOR DISPUTED TERM “VIDEO SIGNAL” (cont'd)

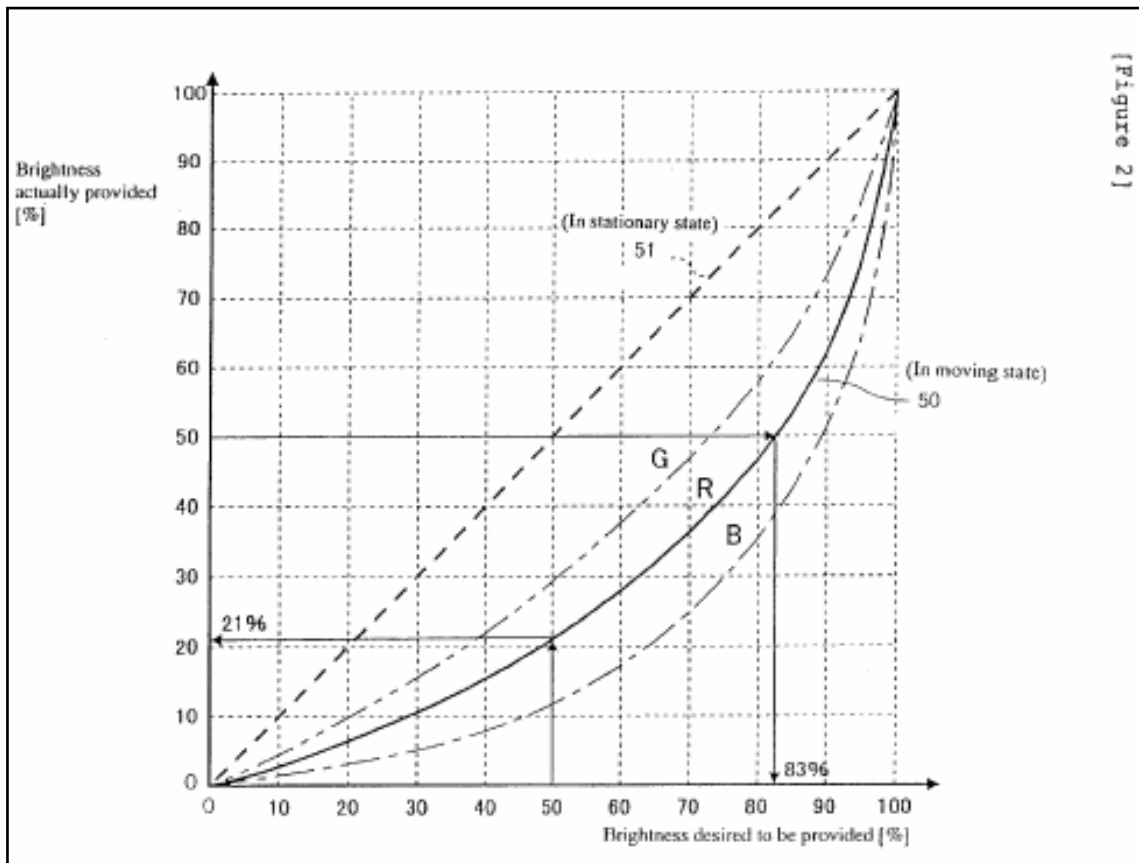


FIG. 2 is a graph showing an example of the brightness of a wire-frame model moving on the LCD panel used in this embodiment. The horizontal scale indicates brightness (%) desired to be provided and the vertical scale indicates brightness (%) actually provided in the Figure. The dashed line 51 indicates the relationship between the desired brightness and actual brightness of the model in a stationary state. The solid line 50 indicates the relationship between the desired brightness and actual brightness of the model in a moving state for an R (red) signal. The alternate long and short two dashes line indicates a G (green) signal in the moving state and the alternate long and short one dash line indicates a B (blue) signal in the moving state. The characteristics in the moving state vary from LCD panel to LCD panel.

7:31-45

**INTRINSIC EVIDENCE FOR DISPUTED TERM “VIDEO SIGNAL”**  
**(cont'd)**

[Figure 7]

26 (Graph base table)

Next brightness Previous brightness	0	10	20	30	40	50	60	70	80	90	100
0	0	28	48	63	74	83	88	93	96	98	100
10	0	10	30	45	56	65	70	75	80	90	100
20	0	10	20	35	46	55	60	70	80	90	100
30	0	10	20	30	41	50	60	70	80	90	100
40	0	10	20	30	40	50	60	70	80	90	100
50	0	10	20	30	40	50	60	70	80	90	100
60	0	10	20	30	40	50	60	70	80	90	100
70	0	10	20	30	40	50	59	70	80	90	100
80	0	10	20	30	40	45	54	65	80	90	100
90	0	10	20	25	30	35	44	55	70	90	100
100	0	2	4	7	12	17	26	38	52	72	100

The first row of the graph base table 26 shown in FIG. 7 indicates brightness output for the next brightness when the previous brightness is 0 and match the readings of the R signal in the moving state line 50 in the graph shown in FIG. 2. For example, if the next brightness is “10”, find a value

9:40-44

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41. In this embodiment, if a difference between the previous brightness and the next brightness is greater than an offset, the next brightness is output without change. For example,

9:56-58

## INTRINSIC EVIDENCE FOR DISPUTED TERM "VIDEO SIGNAL" (cont'd)

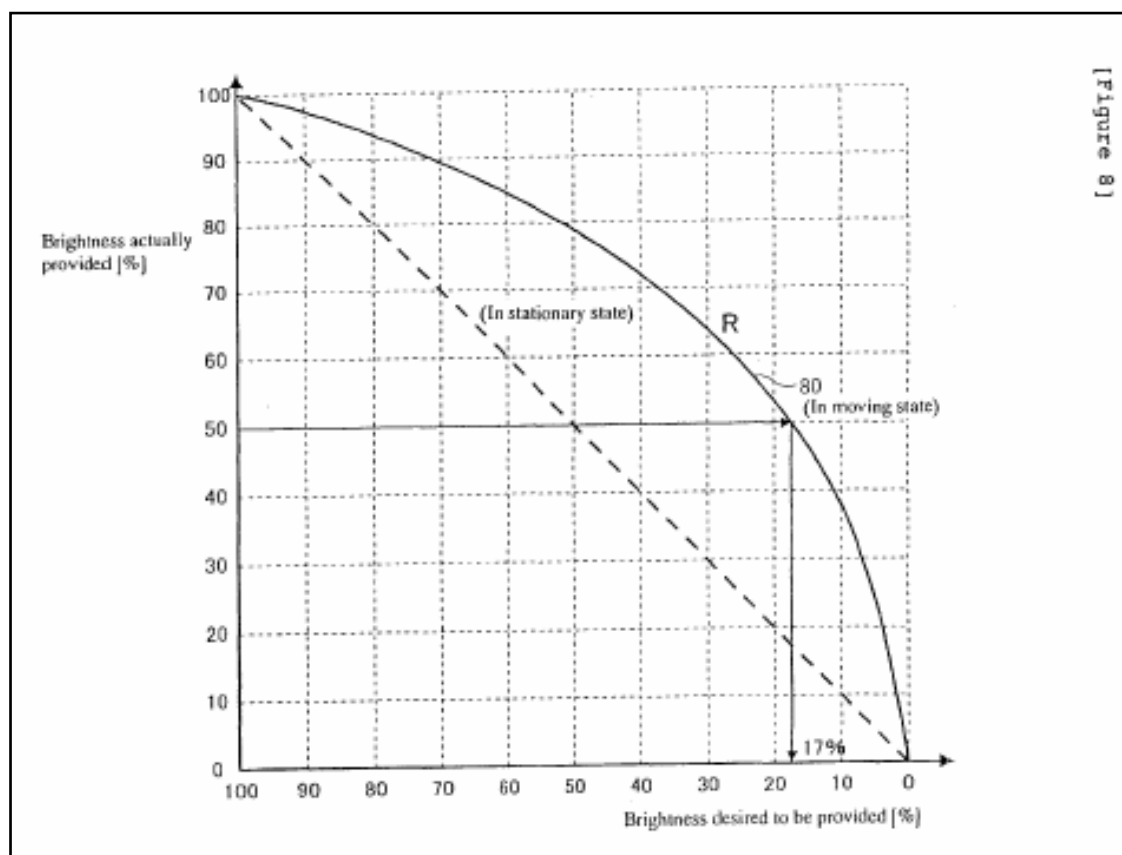


FIG. 8 is a graph showing brightness desired to be provided versus brightness provided actually when brightness falls. The liquid crystal in the example in FIG. 8 has brightness which falls with exhibiting a characteristic similar to the rising characteristic shown in FIG. 2. Accordingly, the line 80 indicating a moving state shown in FIG. 8 is the vertically-flipped curve of the line 50 in a moving state shown in FIG. 2. Tick mark labels on the horizontal scale are also inverted. As can be seen from the graph, when the brightness actually provided is 50%, the brightness desired to be provided is 17%. This matches the value when the previous brightness is 100 and the next brightness is 50 in the table in FIG. 7. That is, the moving state line 80 in FIG. 8 exactly indicates the fall of the previous brightness from 100% in FIG. 7.

10:26-40

**INTRINSIC EVIDENCE FOR DISPUTED TERM “VIDEO SIGNAL”**  
**(cont'd)**

In addition, the embodiment is configured to store the previous brightness level (gray scale value) in the frame buffer 22 and a supplementary correction is made by the ASIC 21 using the data in the graph base table 26 based on the relation between the brightness level of the next video data and the previous brightness level. Thus, whether a

10:57-62

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “THE NEXT BRIGHTNESS LEVEL OF THE NEXT VIDEO SIGNAL INPUT TO SAID INPUT LOGIC”**

The “ideal quantity of light” herein is, to take an example, the quantity of light based on a response characteristic which provides a target brightness level at a time point at which the frame is turned on and provides a brightness level of zero at the time point at which the frame is turned off on a display device in which each pixel is driven for each frame. The brightness level can be represented as a target brightness value by a gray scale and considered as an indication of the characteristic of human visual sensation to brightness. In addition, a brightness change can be considered as a response characteristic depending on the types of liquid

4:47-52

The apparatus further comprises a frame buffer for storing the brightness information of the input wire-frame model as the previous brightness, and characterized by that the storage portion stores the offset as table information based on a relation between the previous brightness stored in the frame buffer and the brightness of the next input wire-frame model, thus, flicker in a moving state can be advantageously inhibited without providing separate determining units for moving and stationary states.

5:31-39

Viewing the present invention as a liquid crystal driving method, the liquid crystal driving method of the present invention is characterized by the steps of storing first brightness information for an input pixel in a frame buffer, and applying, based on second brightness information for the next input pixel and the first brightness information stored in the frame buffer, an offset for making the time integration quantity of a brightness change substantially equal to an ideal light quantity which is brightness in a stationary state to the second brightness information. The steps further include the outputting of the second brightness information to which the offset is applied to a driving circuit for driving an liquid crystal cell, and storing the second brightness information for the input pixel in a frame buffer. This liquid crystal driving method allows the inhibition of flicker by using a simple apparatus without globally determining whether a model is moving or stationary.

6:11:27

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “THE NEXT BRIGHTNESS LEVEL OF THE NEXT VIDEO SIGNAL INPUT TO SAID INPUT LOGIC” (cont'd)**

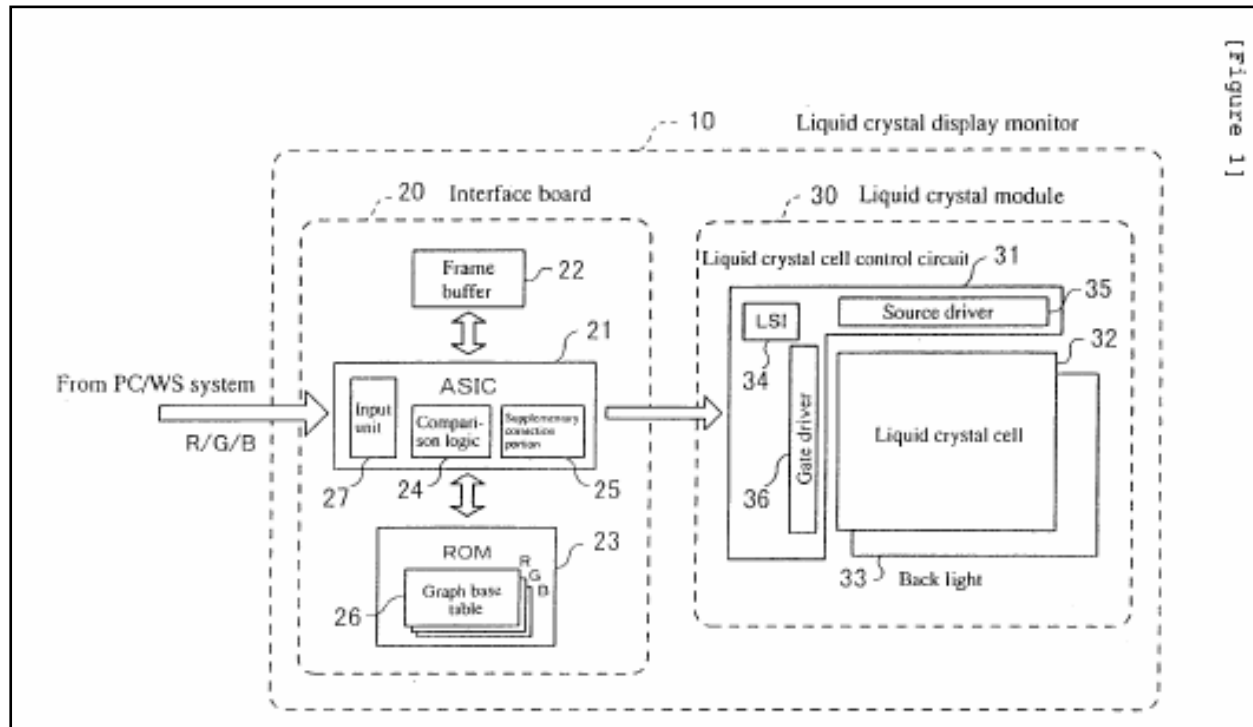


FIG. 1 is a drawing for showing the overall configuration of a liquid crystal display according to an embodiment of the present invention. Reference number 10 denotes a liquid

6:51-53

The I/F board 20 comprises a input unit 27 for inputting video data from a host such as a PC/WS system, a comparison logic 24 for comparing the previous brightness with the next brightness for an input video signal, and an Application-Specific Integrate Circuit (ASIC) 21 including a logic having units such as a supplementary correction portion 25 for performing a supplementary correction. The I/F board 20 also comprises a frame buffer 22 for temporarily storing the input video signal and read-only memory (ROM) 23 containing information needed for the operation of the ASIC 21. The frame buffer 22 stores input video signal value

6:66-7:9

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “THE NEXT BRIGHTNESS LEVEL OF THE NEXT VIDEO SIGNAL INPUT TO SAID INPUT LOGIC” (cont'd)**

[Figure 7]

26 (Graph base table)

Next brightness Previous brightness	0	10	20	30	40	50	60	70	80	90	100
0	0	28	48	63	74	83	88	93	96	98	100
10	0	10	30	45	56	65	70	75	80	90	100
20	0	10	20	35	46	55	60	70	80	90	100
30	0	10	20	30	41	50	60	70	80	90	100
40	0	10	20	30	40	50	60	70	80	90	100
50	0	10	20	30	40	50	60	70	80	90	100
60	0	10	20	30	40	50	60	70	80	90	100
70	0	10	20	30	40	50	59	70	80	90	100
80	0	10	20	30	40	45	54	65	80	90	100
90	0	10	20	25	30	35	44	55	70	90	100
100	0	2	4	7	12	17	26	38	52	72	100

FIG. 7 is a table showing a relation between brightness L1 and L2 and represents the content of the graph base table 26 stored in the ROM 23 shown in FIG. 1. The content of the graph base table 26 shown in FIG. 7 represents a relation between the previous brightness and the next brightness for the LC cell 32 having the characteristic shown in FIG. 2, by taking the effect shown in FIG. 6 into consideration. The previous brightness can be obtained from a video signal input through the ASIC21 shown in FIG. 1 and stored in the frame buffer 22. The next brightness can be obtained from the next video signal input to the ASIC 21. The graph base table 26 is constructed for each of the R, G, B color signals and the values in the table vary depending on the characteristic of the LC cell 32.

9:26-39

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “THE NEXT BRIGHTNESS LEVEL OF THE NEXT VIDEO SIGNAL INPUT TO SAID INPUT LOGIC” (cont'd)**

[Figure 7]

26 (Graph base table)

Next brightness Previous brightness	0	10	20	30	40	50	60	70	80	90	100
0	0	28	48	63	74	83	88	93	96	98	100
10	0	10	30	45	56	65	70	75	80	90	100
20	0	10	20	35	46	55	60	70	80	90	100
30	0	10	20	30	41	50	60	70	80	90	100
40	0	10	20	30	40	50	60	70	80	90	100
50	0	10	20	30	40	50	60	70	80	90	100
60	0	10	20	30	40	50	60	70	80	90	100
70	0	10	20	30	40	50	59	70	80	90	100
80	0	10	20	30	40	45	54	65	80	90	100
90	0	10	20	25	30	35	44	55	70	90	100
100	0	2	4	7	12	17	26	38	52	72	100

The first row of the graph base table 26 shown in FIG. 7 indicates brightness output for the next brightness when the previous brightness is 0 and match the readings of the R signal in the moving state line 50 in the graph shown in FIG. 2. For example, if the next brightness is “10”, find a value

9:40-44

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41. In this embodiment, if a difference between the previous brightness and the next brightness is greater than an offset, the next brightness is output without change. For example,

9:56-58

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “THE NEXT BRIGHTNESS LEVEL OF THE NEXT VIDEO SIGNAL INPUT TO SAID INPUT LOGIC” (cont'd)**

On the other hand, when brightness falls from a certain halftone to another halftone, the offset is subtracted from the previous brightness. The example in FIG. 7 shows a case where the characteristic of the LC cell 32 when brightness rises (the cell is turned on) is the same as that when the brightness falls (the cell is turned off). In this example, if the previous brightness is 100 and the next brightness is 10, the output value will be  $100 - 98 = 2$ . The value “98” is equal to the value when the previous brightness is 0 and the next brightness is 90 in FIG. 7. Similarly, if the previous brightness is 100 and the next brightness is 20, then  $100 - 96 = 4$ . If the previous brightness is 90 and the next brightness is 30, then  $100 - 75 = 25$ . The value “75” is equal to the value when the previous brightness is 10 and the next brightness is 70 in FIG. 7. Similarly, if the previous brightness is 90 and the next brightness is 40, then  $100 - 70 = 30$ . The value “70” is equal to the value when the previous brightness is 10 and the next brightness is 60 in FIG. 7.

9:64-10:3

As described above, the embodiment is configured to store offsets in table form based on the relation between a brightness level in a stationary state and that in a moving state in order to obtain an ideal quantity of light. Thus, even during the movement of a display image on the LCD screen, the image can be displayed virtually the same brightness to the eye as in its stationary state, thereby inhibiting flicker on the screen.

In addition, the embodiment is configured to store the previous brightness level (gray scale value) in the frame buffer 22 and a supplementary correction is made by the ASIC 21 using the data in the graph base table 26 based on the relation between the brightness level of the next video data and the previous brightness level. Thus, whether a wire-frame model is moving or stationary is not required to be determined. Instead, the movement of the model can be determined from a difference between the determined brightness and the previous brightness. As a result, flicker can be inhibited by a simple circuit configuration.

10:49-67

## **INTRINSIC EVIDENCE FOR DISPUTED TERM “FIRST BRIGHTNESS INFORMATION FOR AN INPUT PIXEL”**

The “ideal quantity of light” herein is, to take an example, the quantity of light based on a response characteristic which provides a target brightness level at a time point at which the frame is turned on and provides a brightness level of zero at the time point at which the frame is turned off on a display device in which each pixel is driven for each frame. The brightness level can be represented as a target brightness value by a gray scale and considered as an indication of the characteristic of human visual sensation to brightness. In addition, a brightness change can be considered as a response characteristic depending on the types of liquid

4:42-52

The video signal input through the input consists of a plurality of color signals and the table in the determinator is provided for each of the color signals so that a brightness level correction for each color can be made with respect to flicker perception of the human eye to reduce a difference in brightness, thereby an easy-on-the-eye liquid crystal display can be provided to the user. While the color signals may be R (red), G (green), B (blue) signals used in displays, other display systems can also be used.

5:7-15

The apparatus further comprises a frame buffer for storing the brightness information of the input wire-frame model as the previous brightness, and characterized by that the storage portion stores the offset as table information based on a relation between the previous brightness stored in the frame buffer and the brightness of the next input wire-frame model, thus, flicker in a moving state can be advantageously inhibited without providing separate determining units for moving and stationary states.

5:31-39

**INTRINSIC EVIDENCE FOR DISPUTED TERM “FIRST BRIGHTNESS INFORMATION FOR AN INPUT PIXEL” (cont'd)**

In another category, the present invention is a flicker inhibition method for inhibiting flicker caused by a difference in brightness when an input wire-frame model is displayed by a liquid crystal cell. The method is characterized by storing a relation between brightness in a stationary state in which a wire-frame model having a predetermined gray scale is displayed on a particular pixel across a plurality of frames and brightness in a moving state in which the wire-frame model having the predetermined gray scale changes frame to frame with respect to the particular pixel, applying an offset based on the stored relation to the gray scale of the wire-frame model if the input wire-frame model is in a moving state, and driving the liquid crystal cell based on the gray scale to which the offset is applied to display the wire-frame model.

5:51-65

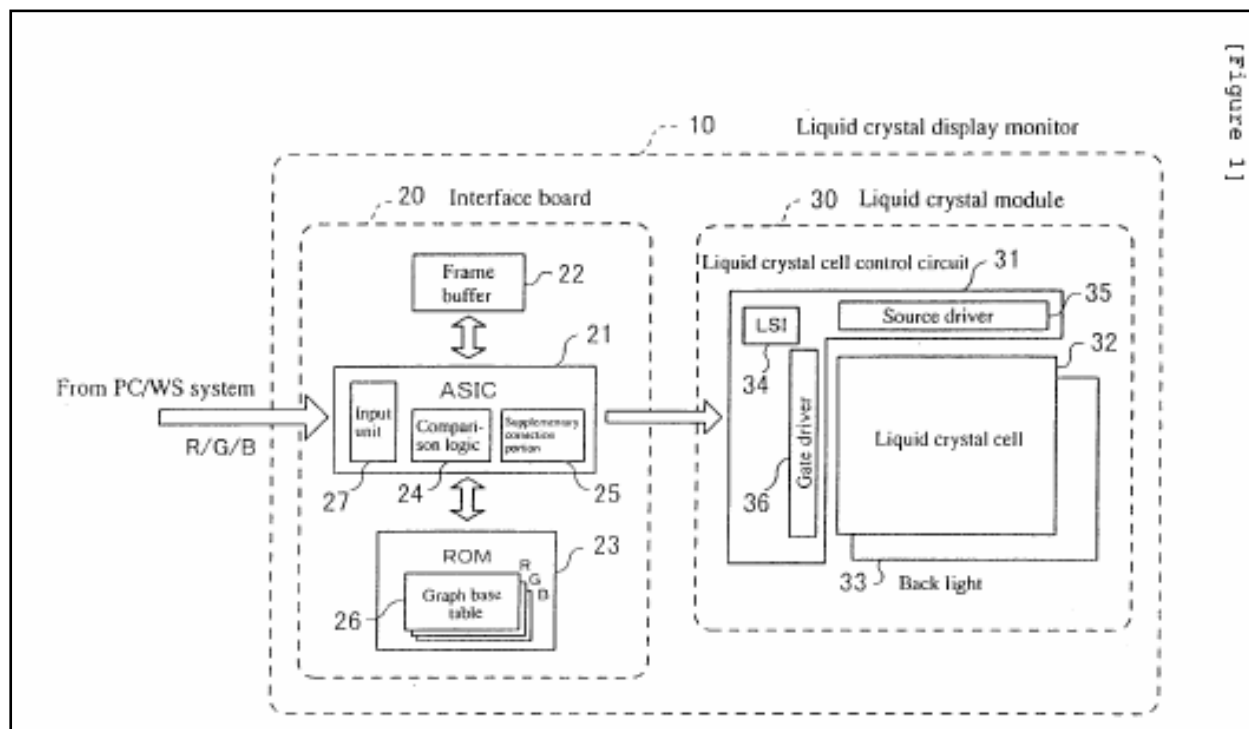
Viewing the present invention as a liquid crystal driving method, the liquid crystal driving method of the present invention is characterized by the steps of storing first brightness information for an input pixel in a frame buffer, and applying, based on second brightness information for the next input pixel and the first brightness information stored in the frame buffer, an offset for making the time integration quantity of a brightness change substantially equal to an ideal light quantity which is brightness in a stationary state to the second brightness information. The steps further include the outputting of the second brightness information to which the offset is applied to a driving circuit for driving an liquid crystal cell, and storing the second brightness information for the input pixel in a frame buffer. This liquid crystal driving method allows the inhibition of flicker by using a simple apparatus without globally determining whether a model is moving or stationary.

6:11-27

The present invention is still further characterized in that the input pixel consists of a plurality color signals and includes the step of storing the first brightness information in the frame buffer stores the first brightness information for each of the color signals, and the step of applying the offset applies the offset to each of the color signals, thus the brightness of each color of a color image consisting of a plurality of color signals can be corrected individually, allowing more adequate flicker inhibition.

6:28-36

**INTRINSIC EVIDENCE FOR DISPUTED TERM “FIRST BRIGHTNESS INFORMATION FOR AN INPUT PIXEL” (cont'd)**



[Figure 1]

FIG. 1 is a drawing for showing the overall configuration of a liquid crystal display according to an embodiment of the present invention. Reference number 10 denotes a liquid

6:51-53

The I/F board 20 comprises a input unit 27 for inputting video data from a host such as a PC/WS system, a comparison logic 24 for comparing the previous brightness with the next brightness for an input video signal, and an Application-Specific Integrate Circuit (ASIC) 21 including a logic having units such as a supplementary correction portion 25 for performing a supplementary correction. The I/F board 20 also comprises a frame buffer 22 for temporarily storing the input video signal and read-only memory (ROM) 23 containing information needed for the operation of the ASIC 21. The frame buffer 22 stores input video signal value

6:66-7:9

**INTRINSIC EVIDENCE FOR DISPUTED TERM “FIRST BRIGHTNESS INFORMATION FOR AN INPUT PIXEL” (cont'd)**

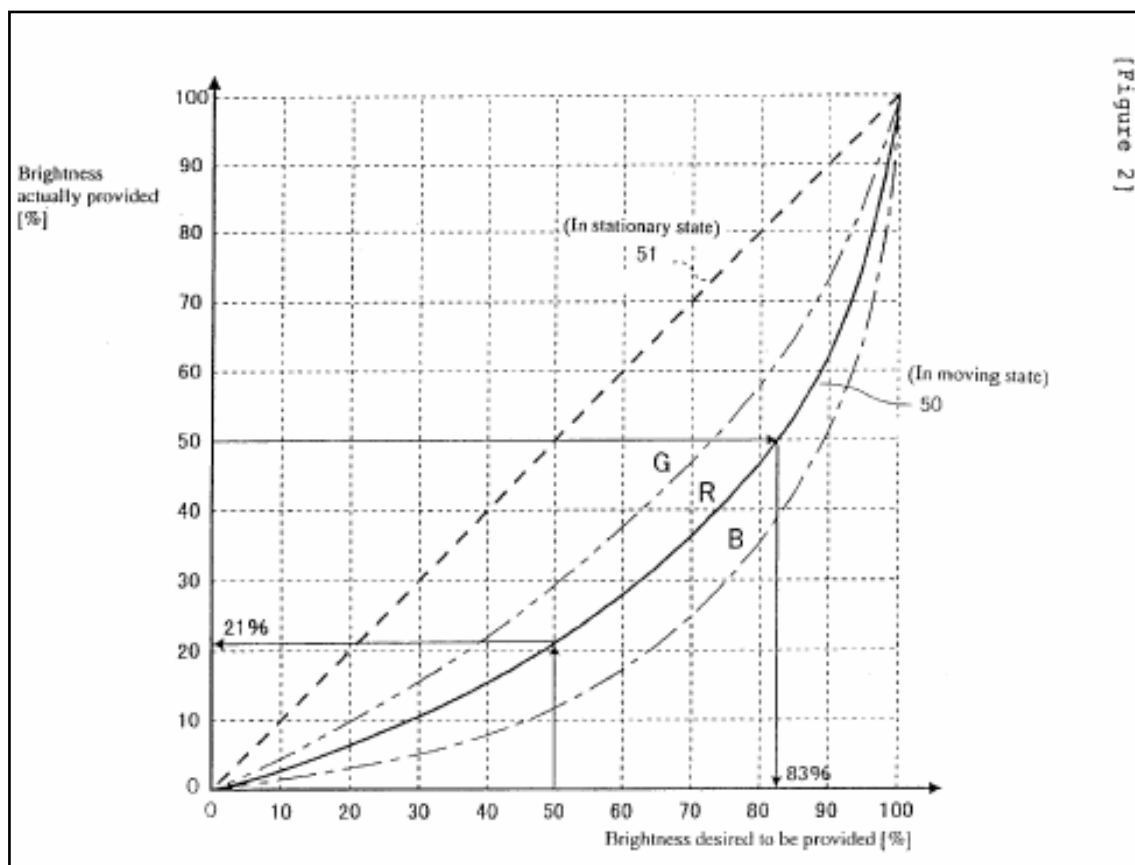


FIG. 2 is a graph showing an example of the brightness of a wire-frame model moving on the LCD panel used in this embodiment. The horizontal scale indicates brightness (%) desired to be provided and the vertical scale indicates brightness (%) actually provided in the Figure. The dashed line 51 indicates the relationship between the desired brightness and actual brightness of the model in a stationary state. The solid line 50 indicates the relationship between the desired brightness and actual brightness of the model in a moving state for an R (red) signal. The alternate long and short two dashes line indicates a G (green) signal in the moving state and the alternate long and short one dash line indicates a B (blue) signal in the moving state. The characteristics in the moving state vary from LCD panel to LCD panel.

7:31-45

**INTRINSIC EVIDENCE FOR DISPUTED TERM “FIRST  
BRIGHTNESS INFORMATION FOR AN INPUT PIXEL” (cont'd)**

[Figure 7]

26 (Graph base table)

Next brightness Previous brightness	0	10	20	30	40	50	60	70	80	90	100
0	0	28	48	63	74	83	88	93	96	98	100
10	0	10	30	45	56	65	70	75	80	90	100
20	0	10	20	35	46	55	60	70	80	90	100
30	0	10	20	30	41	50	60	70	80	90	100
40	0	10	20	30	40	50	60	70	80	90	100
50	0	10	20	30	40	50	60	70	80	90	100
60	0	10	20	30	40	50	60	70	80	90	100
70	0	10	20	30	40	50	59	70	80	90	100
80	0	10	20	30	40	45	54	65	80	90	100
90	0	10	20	25	30	35	44	55	70	90	100
100	0	2	4	7	12	17	26	38	52	72	100

FIG. 7 is a table showing a relation between brightness L1 and L2 and represents the content of the graph base table 26 stored in the ROM 23 shown in FIG. 1. The content of the graph base table 26 shown in FIG. 7 represents a relation between the previous brightness and the next brightness for the LC cell 32 having the characteristic shown in FIG. 2, by taking the effect shown in FIG. 6 into consideration. The previous brightness can be obtained from a video signal input through the ASIC21 shown in FIG. 1 and stored in the frame buffer 22. The next brightness can be obtained from the next video signal input to the ASIC 21. The graph base table 26 is constructed for each of the R, G, B color signals and the values in the table vary depending on the characteristic of the LC cell 32.

9:26-39

**INTRINSIC EVIDENCE FOR DISPUTED TERM “FIRST BRIGHTNESS INFORMATION FOR AN INPUT PIXEL” (cont'd)**

[Figure 7]

26 (Graph base table)

Next brightness Previous brightness	0	10	20	30	40	50	60	70	80	90	100
0	0	28	48	63	74	83	88	93	96	98	100
10	0	10	30	45	56	65	70	75	80	90	100
20	0	10	20	35	46	55	60	70	80	90	100
30	0	10	20	30	41	50	60	70	80	90	100
40	0	10	20	30	40	50	60	70	80	90	100
50	0	10	20	30	40	50	60	70	80	90	100
60	0	10	20	30	40	50	60	70	80	90	100
70	0	10	20	30	40	50	59	70	80	90	100
80	0	10	20	30	40	45	54	65	80	90	100
90	0	10	20	25	30	35	44	55	70	90	100
100	0	2	4	7	12	17	26	38	52	72	100

The first row of the graph base table 26 shown in FIG. 7 indicates brightness output for the next brightness when the previous brightness is 0 and match the readings of the R signal in the moving state line 50 in the graph shown in FIG. 2. For example, if the next brightness is “10”, find a value

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41. In this embodiment, if a difference between the previous brightness and the next brightness is greater than an offset, the next brightness is output without change. For example,

9:40-58

**INTRINSIC EVIDENCE FOR DISPUTED TERM “FIRST  
BRIGHTNESS INFORMATION FOR AN INPUT PIXEL” (cont'd)**

On the other hand, when brightness falls from a certain halftone to another halftone, the offset is subtracted from the previous brightness. The example in FIG. 7 shows a case where the characteristic of the LC cell 32 when brightness rises (the cell is turned on) is the same as that when the brightness falls (the cell is turned off). In this example, if the previous brightness is 100 and the next brightness is 10, the output value will be  $100-98=2$ . The value “98” is equal to the value when the previous brightness is 0 and the next brightness is 90 in FIG. 7. Similarly, if the previous brightness is 100 and the next brightness is 20, then  $100-96=4$ . If the previous brightness is 90 and the next brightness is 30, then  $100-75=25$ . The value “75” is equal to the value when the previous brightness is 10 and the next brightness is 70 in FIG. 7. Similarly, if the previous brightness is 90 and the next brightness is 40, then  $100-70=30$ . The value “70” is equal to the value when the previous brightness is 10 and the next brightness is 60 in FIG. 7.

9:64-10:13

**INTRINSIC EVIDENCE FOR DISPUTED TERM “FIRST BRIGHTNESS INFORMATION FOR AN INPUT PIXEL” (cont'd)**

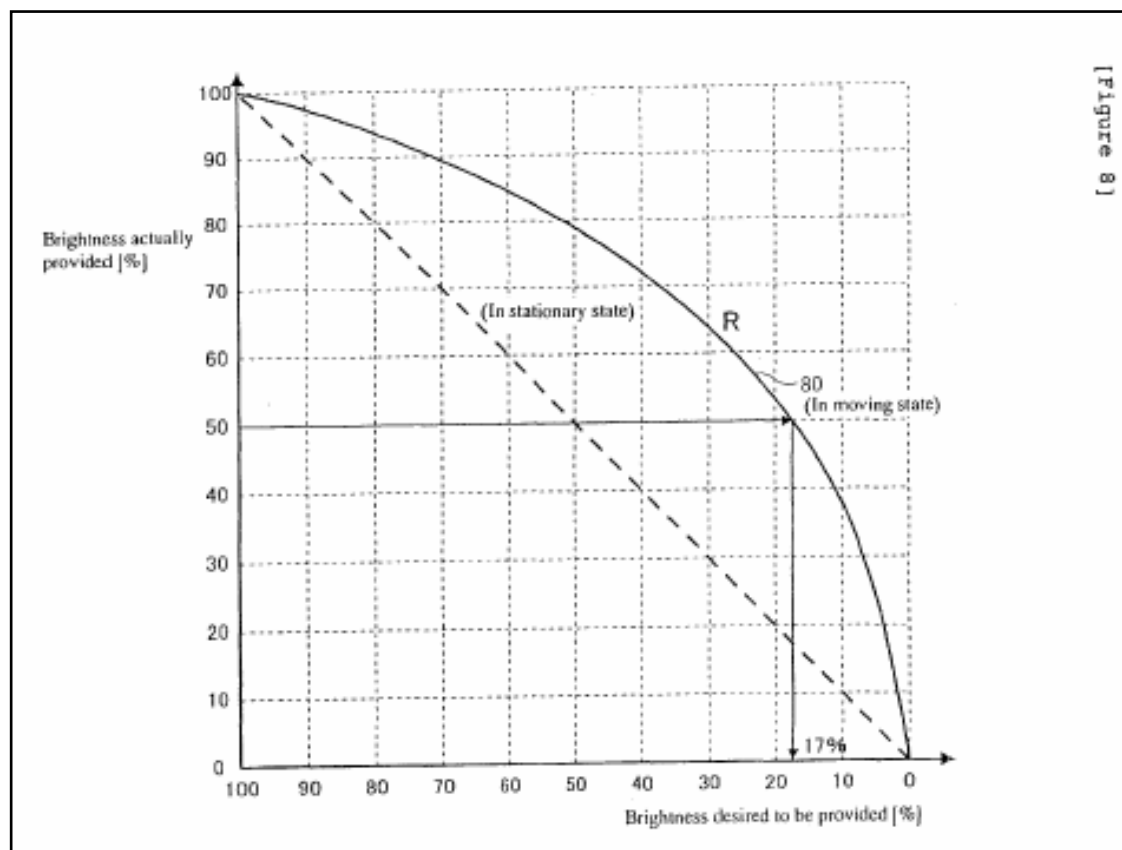


FIG. 8 is a graph showing brightness desired to be provided versus brightness provided actually when brightness falls. The liquid crystal in the example in FIG. 8 has brightness which falls with exhibiting a characteristic similar to the rising characteristic shown in FIG. 2. Accordingly, the line 80 indicating a moving state shown in FIG. 8 is the vertically-flipped curve of the line 50 in a moving state shown in FIG. 2. Tick mark labels on the horizontal scale are also inverted. As can be seen from the graph, when the brightness actually provided is 50%, the brightness desired to be provided is 17%. This matches the value when the previous brightness is 100 and the next brightness is 50 in the table in FIG. 7. That is, the moving state line 80 in FIG. 8 exactly indicates the fall of the previous brightness from 100% in FIG. 7.

10:26-40

**INTRINSIC EVIDENCE FOR DISPUTED TERM “FIRST  
BRIGHTNESS INFORMATION FOR AN INPUT PIXEL” (cont'd)**

As described above, the embodiment is configured to store offsets in table form based on the relation between a brightness level in a stationary state and that in a moving state in order to obtain an ideal quantity of light. Thus, even during the movement of a display image on the LCD screen, the image can be displayed virtually the same brightness to the eye as in its stationary state, thereby inhibiting flicker on the screen.

In addition, the embodiment is configured to store the previous brightness level (gray scale value) in the frame buffer 22 and a supplementary correction is made by the ASIC 21 using the data in the graph base table 26 based on the relation between the brightness level of the next video data and the previous brightness level. Thus, whether a wire-frame model is moving or stationary is not required to be determined. Instead, the movement of the model can be determined from a difference between the determined brightness and the previous brightness. As a result, flicker can be inhibited by a simple circuit configuration.

10:49-67

## **INTRINSIC EVIDENCE FOR DISPUTED TERM “SECOND BRIGHTNESS INFORMATION FOR AN INPUT PIXEL”**

The “ideal quantity of light” herein is, to take an example, the quantity of light based on a response characteristic which provides a target brightness level at a time point at which the frame is turned on and provides a brightness level of zero at the time point at which the frame is turned off on a display device in which each pixel is driven for each frame. The brightness level can be represented as a target brightness value by a gray scale and considered as an indication of the characteristic of human visual sensation to brightness. In addition, a brightness change can be considered as a response characteristic depending on the types of liquid

4:47-52

The apparatus further comprises a frame buffer for storing the brightness information of the input wire-frame model as the previous brightness, and characterized by that the storage portion stores the offset as table information based on a relation between the previous brightness stored in the frame buffer and the brightness of the next input wire-frame model, thus, flicker in a moving state can be advantageously inhibited without providing separate determining units for moving and stationary states.

5:31-39

Viewing the present invention as a liquid crystal driving method, the liquid crystal driving method of the present invention is characterized by the steps of storing first brightness information for an input pixel in a frame buffer, and applying, based on second brightness information for the next input pixel and the first brightness information stored in the frame buffer, an offset for making the time integration quantity of a brightness change substantially equal to an ideal light quantity which is brightness in a stationary state to the second brightness information. The steps further include the outputting of the second brightness information to which the offset is applied to a driving circuit for driving an liquid crystal cell, and storing the second brightness information for the input pixel in a frame buffer. This liquid crystal driving method allows the inhibition of flicker by using a simple apparatus without globally determining whether a model is moving or stationary.

6:11-27

**INTRINSIC EVIDENCE FOR DISPUTED TERM “SECOND BRIGHTNESS INFORMATION FOR AN INPUT PIXEL” (cont'd)**

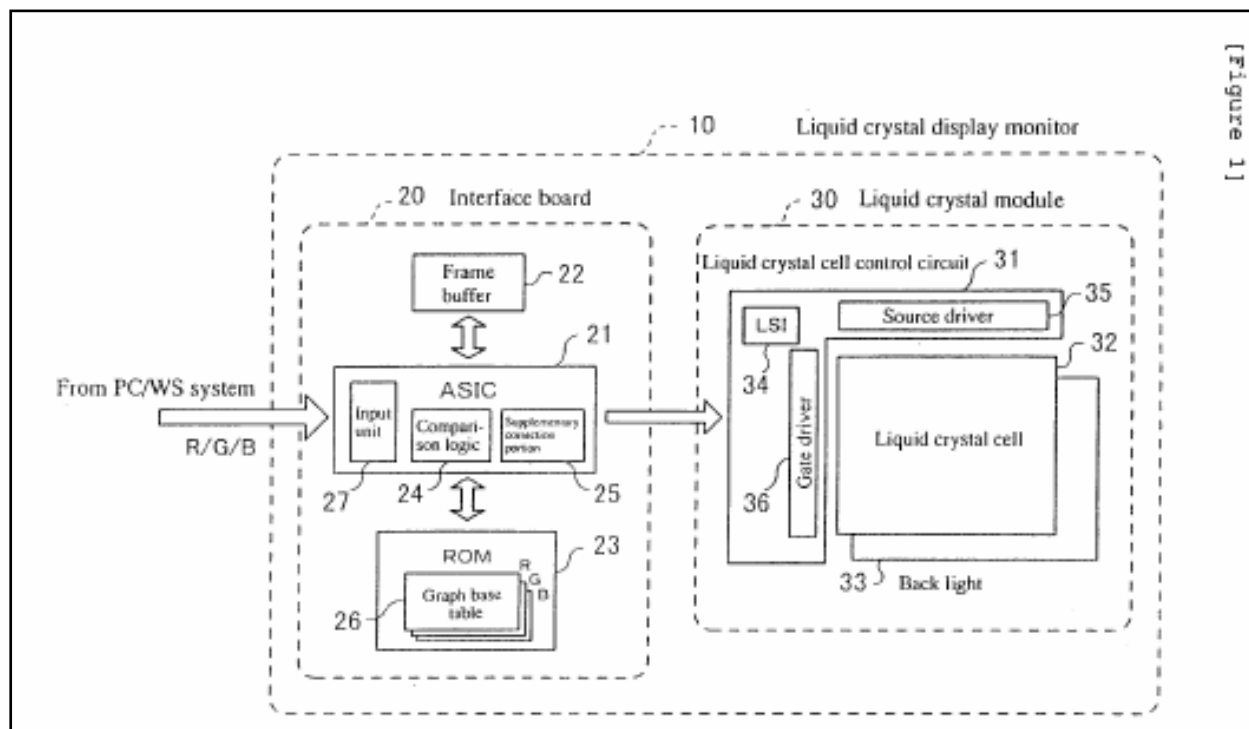


FIG. 1 is a drawing for showing the overall configuration of a liquid crystal display according to an embodiment of the present invention. Reference number 10 denotes a liquid

6:51-53

The I/F board 20 comprises a input unit 27 for inputting video data from a host such as a PC/WS system, a comparison logic 24 for comparing the previous brightness with the next brightness for an input video signal, and an Application-Specific Integrate Circuit (ASIC) 21 including a logic having units such as a supplementary correction portion 25 for performing a supplementary correction. The I/F board 20 also comprises a frame buffer 22 for temporarily storing the input video signal and read-only memory (ROM) 23 containing information needed for the operation of the ASIC 21. The frame buffer 22 stores input video signal value

6:66-67,  
7:1-9

**INTRINSIC EVIDENCE FOR DISPUTED TERM “SECOND BRIGHTNESS INFORMATION FOR AN INPUT PIXEL” (cont'd)**

[Figure 7]

26 (Graph base table)

Next brightness Previous brightness	0	10	20	30	40	50	60	70	80	90	100
0	0	28	48	63	74	83	88	93	96	98	100
10	0	10	30	45	56	65	70	75	80	90	100
20	0	10	20	35	46	55	60	70	80	90	100
30	0	10	20	30	41	50	60	70	80	90	100
40	0	10	20	30	40	50	60	70	80	90	100
50	0	10	20	30	40	50	60	70	80	90	100
60	0	10	20	30	40	50	60	70	80	90	100
70	0	10	20	30	40	50	59	70	80	90	100
80	0	10	20	30	40	45	54	65	80	90	100
90	0	10	20	25	30	35	44	55	70	90	100
100	0	2	4	7	12	17	26	38	52	72	100

FIG. 7 is a table showing a relation between brightness L1 and L2 and represents the content of the graph base table 26 stored in the ROM 23 shown in FIG. 1. The content of the graph base table 26 shown in FIG. 7 represents a relation between the previous brightness and the next brightness for the LC cell 32 having the characteristic shown in FIG. 2, by taking the effect shown in FIG. 6 into consideration. The previous brightness can be obtained from a video signal input through the ASIC21 shown in FIG. 1 and stored in the frame buffer 22. The next brightness can be obtained from the next video signal input to the ASIC 21. The graph base table 26 is constructed for each of the R, G, B color signals and the values in the table vary depending on the characteristic of the LC cell 32.

9:26-39

**INTRINSIC EVIDENCE FOR DISPUTED TERM “SECOND BRIGHTNESS INFORMATION FOR AN INPUT PIXEL” (cont'd)**

[Figure 7]

26 (Graph base table)

Next brightness Previous brightness	0	10	20	30	40	50	60	70	80	90	100
0	0	28	48	63	74	83	88	93	96	98	100
10	0	10	30	45	56	65	70	75	80	90	100
20	0	10	20	35	46	55	60	70	80	90	100
30	0	10	20	30	41	50	60	70	80	90	100
40	0	10	20	30	40	50	60	70	80	90	100
50	0	10	20	30	40	50	60	70	80	90	100
60	0	10	20	30	40	50	60	70	80	90	100
70	0	10	20	30	40	50	59	70	80	90	100
80	0	10	20	30	40	45	54	65	80	90	100
90	0	10	20	25	30	35	44	55	70	90	100
100	0	2	4	7	12	17	26	38	52	72	100

The first row of the graph base table 26 shown in FIG. 7 indicates brightness output for the next brightness when the previous brightness is 0 and match the readings of the R signal in the moving state line 50 in the graph shown in FIG. 2. For example, if the next brightness is “10”, find a value

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41. In this embodiment, if a difference between the previous brightness and the next brightness is greater than an offset, the next brightness is output without change. For example,

9:40-58

**INTRINSIC EVIDENCE FOR DISPUTED TERM “SECOND BRIGHTNESS INFORMATION FOR AN INPUT PIXEL” (cont'd)**

On the other hand, when brightness falls from a certain halftone to another halftone, the offset is subtracted from the previous brightness. The example in FIG. 7 shows a case where the characteristic of the LC cell 32 when brightness rises (the cell is turned on) is the same as that when the brightness falls (the cell is turned off). In this example, if the previous brightness is 100 and the next brightness is 10, the output value will be  $100 - 98 = 2$ . The value “98” is equal to the value when the previous brightness is 0 and the next brightness is 90 in FIG. 7. Similarly, if the previous brightness is 100 and the next brightness is 20, then  $100 - 96 = 4$ . If the previous brightness is 90 and the next brightness is 30, then  $100 - 75 = 25$ . The value “75” is equal to the value when the previous brightness is 10 and the next brightness is 70 in FIG. 7. Similarly, if the previous brightness is 90 and the next brightness is 40, then  $100 - 70 = 30$ . The value “70” is equal to the value when the previous brightness is 10 and the next brightness is 60 in FIG. 7.

9:64-67,  
10:1-13

As described above, the embodiment is configured to store offsets in table form based on the relation between a brightness level in a stationary state and that in a moving state in order to obtain an ideal quantity of light. Thus, even during the movement of a display image on the LCD screen, the image can be displayed virtually the same brightness to the eye as in its stationary state, thereby inhibiting flicker on the screen.

In addition, the embodiment is configured to store the previous brightness level (gray scale value) in the frame buffer 22 and a supplementary correction is made by the ASIC 21 using the data in the graph base table 26 based on the relation between the brightness level of the next video data and the previous brightness level. Thus, whether a wire-frame model is moving or stationary is not required to be determined. Instead, the movement of the model can be determined from a difference between the determined brightness and the previous brightness. As a result, flicker can be inhibited by a simple circuit configuration.

10:49-67

**EXHIBIT \_\_\_\_\_**  
**U.S. PATENT NO. 6,778,160**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 1**

1. A liquid crystal display, comprising:  
an input logic for inputting a video signal from a host;  
a storage for storing the previous brightness level of the video signal input through said input logic;  
a determinator for determining an output brightness level based on the previous brightness level stored in said storage and the next brightness level of the next video signal input to said input logic so as to make a time integration quantity of a brightness change substantially equal to an ideal quantity of light in a stationary state with respect to the next brightness level; and  
a driver for driving an image displaying liquid crystal cell based on said output brightness level determined by said determination logic.

**LGD's Claim Construction**

**ideal quantity of light in a stationary state** - quantity of light based on the ideal response characteristic of the liquid crystal cell when the liquid crystal cell is provided with the next brightness level during the next time increment and the previous brightness level before and after the next time increment.

**an offset for making the time integration quantity of a brightness change substantially equal to an ideal light quantity which is the brightness in a stationary state to said second brightness**

**information** - a value predetermined based on difference in quantity of light between the actual and ideal response characteristics of the pixel so that the quantity of light based on the actual response characteristic of the pixel to be substantially equal to the quantity of light based on the ideal response characteristic of the pixel when the pixel is provided with the second brightness level during the next frame and the first brightness level before and after the next frame.

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “IDEAL  
QUANTITY OF LIGHT IN A STATIONARY STATE”**

The term “response time” used in the industry refers to the sum of (1) time required to reverse color by applying a voltage to a liquid crystal cell and (2) time required to restore the original color by the removal of the applied voltage. The term “frame” used in the industry represents the

1:39-43

The “ideal quantity of light” herein is, to take an example, the quantity of light based on a response characteristic which provides a target brightness level at a time point at which the frame is turned on and provides a brightness level of zero at the time point at which the frame is turned off on a display device in which each pixel is driven for each frame. The brightness level can be represented as a target brightness value by a gray scale and considered as an indication of the characteristic of human visual sensation to brightness. In addition, a brightness change can be considered as a response characteristic depending on the types of liquid

4:47-52

The moving state brightness used for storing the relation is the brightness when the particular pixel changes back to the off state one frame after it is driven from the off state to the on state during the passage of the wire-frame model over the particular pixel.

Furthermore, the brightness in the moving state which is used when the relation is stored is the quantity of light equal to the brightness change integrated with respect to time.

5:66-6:6

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “IDEAL  
QUANTITY OF LIGHT IN A STATIONARY STATE” (cont'd)**

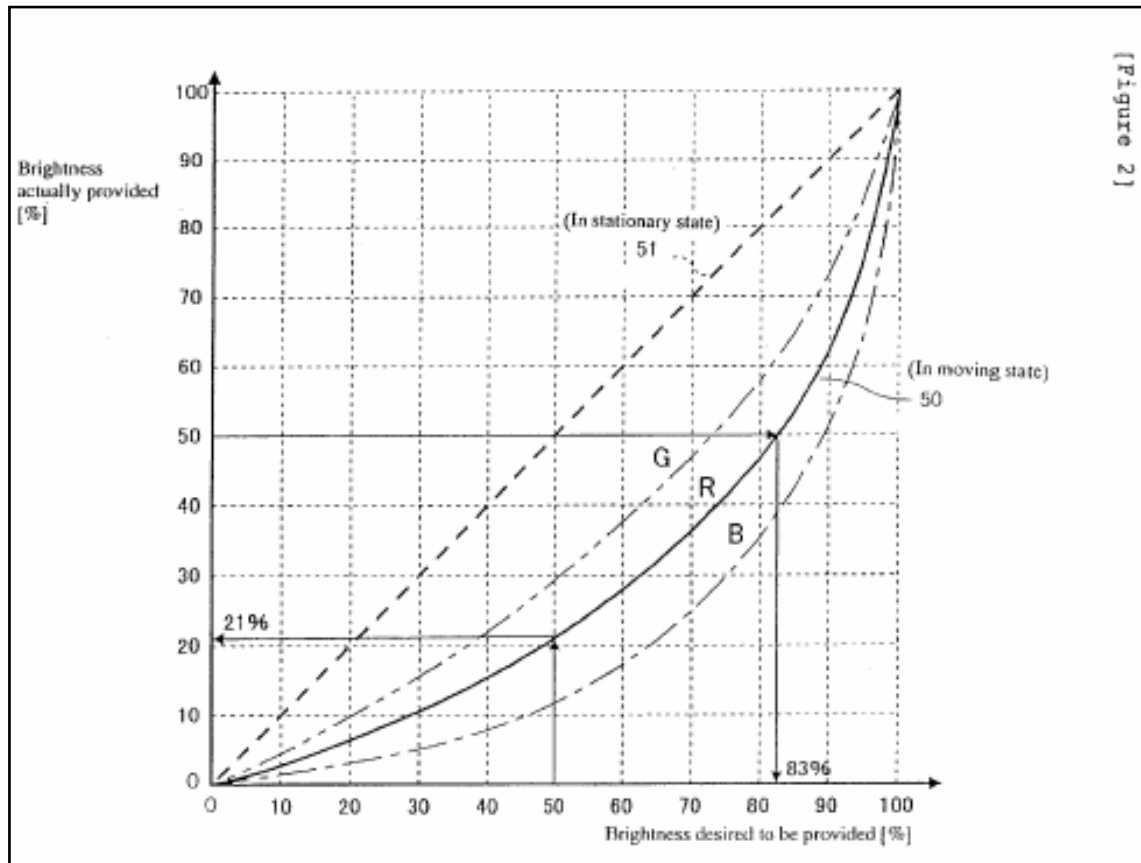


FIG. 2 is a graph showing an example of the brightness of a wire-frame model moving on the LCD panel used in this embodiment. The horizontal scale indicates brightness (%) desired to be provided and the vertical scale indicates brightness (%) actually provided in the Figure. The dashed line 51 indicates the relationship between the desired brightness and actual brightness of the model in a stationary state. The solid line 50 indicates the relationship between the desired brightness and actual brightness of the model in a moving state for an R (red) signal. The alternate long and short two dashes line indicates a G (green) signal in the moving state and the alternate long and short one dash line indicates a B (blue) signal in the moving state. The characteristics in the moving state vary from LCD panel to LCD panel.

7:31-45

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “IDEAL  
QUANTITY OF LIGHT IN A STATIONARY STATE” (cont'd)**

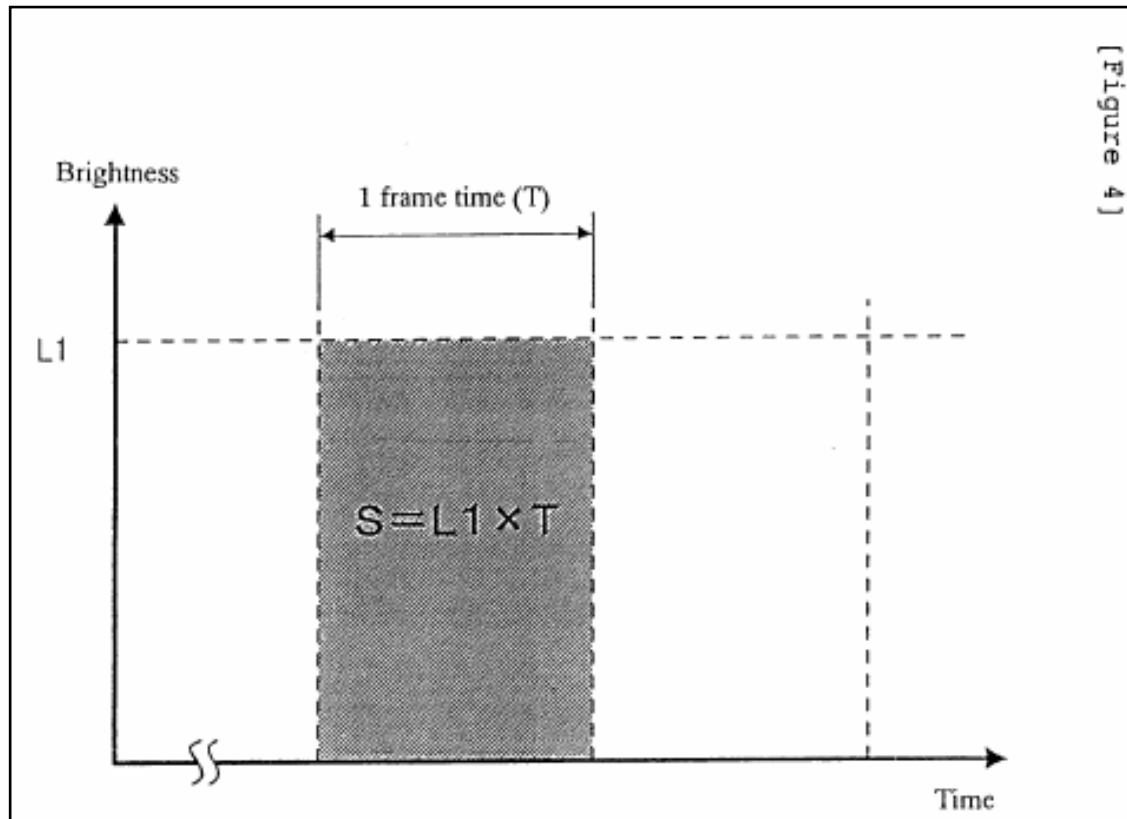
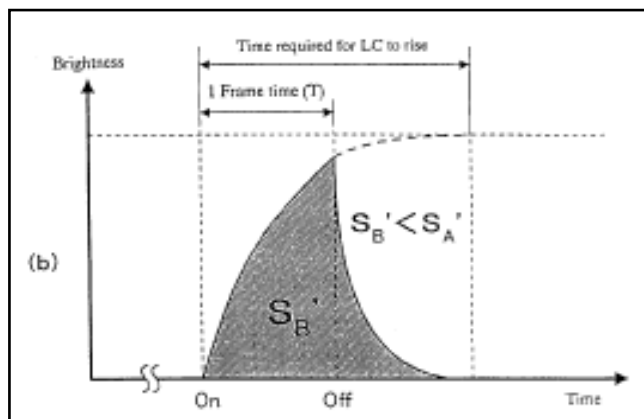
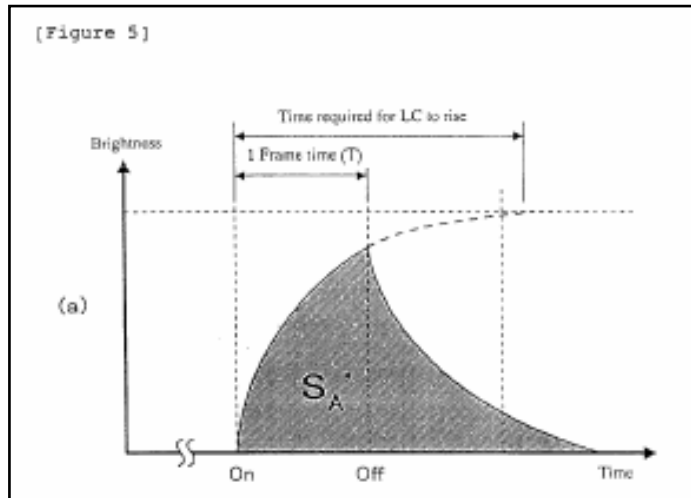


FIG. 4 shows the response characteristic of an ideal liquid crystal and indicates the state in which a particular pixel is kept lit up at a brightness of L1, that is in a stationary state. Here, the quantity of light (S) emitted in one frame time (T) is equal to  $L1 \times T$  (i.e. brightness  $\times$  time) as shown in the shaded area in FIG. 4.

8:35-40

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “IDEAL  
QUANTITY OF LIGHT IN A STATIONARY STATE” (cont'd)**



FIGS. 5A and 5B show the response characteristic represented by brightness versus time when a pixel stays lit up for one frame time (On→Off) in models A, B shown in FIG. 3. Both of the rising and falling of the response of model A

8:41-44

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “IDEAL QUANTITY OF LIGHT IN A STATIONARY STATE” (cont'd)**

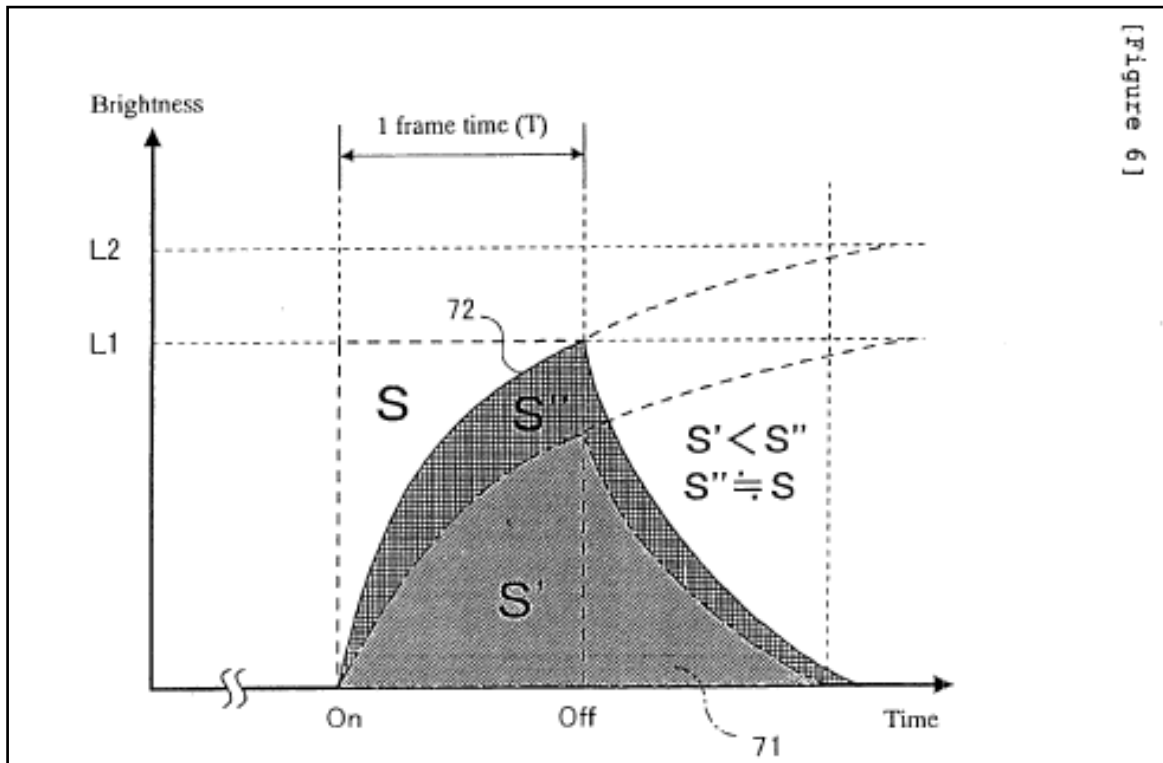


FIG. 6 shows an effect when brightness is set by taking a required offset into account. If the liquid crystal is driven trying to achieve desired brightness  $L_1$  as target, only the quantity of light ( $S'$ ) indicated by reference number 71 can be obtained due to the response time of the liquid crystal described above. The quantity of light ( $S'$ ) 71 is much smaller than the quantity of light ( $S$ ) provided by the ideal response characteristic shown in FIG. 4. On the other hand, if the liquid crystal is driven with the aim of achieving brightness  $L_2$  which is larger than the desired brightness of  $L_1$ , the quantity of light ( $S''$ ) indicated by reference number 72 can be obtained. By overdriving the LC to brightness  $L_2$ , the LC reaches  $L_1$  in a short response time and the quantity of light ( $S''$ ) 72 can be obtained which is approximately the same as the quantity of light ( $S$ ), which would be provided with the ideal response characteristic ( $S'' \sim S$ ). Here, optimum brightness  $L_2$  with respect to  $L_1$  can be obtained from the data shown in FIG. 2.

9:8-25

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “IDEAL  
QUANTITY OF LIGHT IN A STATIONARY STATE” (cont'd)**

[Figure 7]

26 (Graph base table)

Next brightness Previous brightness	0	10	20	30	40	50	60	70	80	90	100
0	0	28	48	63	74	83	88	93	96	98	100
10	0	10	30	45	56	65	70	75	80	90	100
20	0	10	20	35	46	55	60	70	80	90	100
30	0	10	20	30	41	50	60	70	80	90	100
40	0	10	20	30	40	50	60	70	80	90	100
50	0	10	20	30	40	50	60	70	80	90	100
60	0	10	20	30	40	50	60	70	80	90	100
70	0	10	20	30	40	50	59	70	80	90	100
80	0	10	20	30	40	45	54	65	80	90	100
90	0	10	20	25	30	35	44	55	70	90	100
100	0	2	4	7	12	17	26	38	52	72	100

FIG. 7 is a table showing a relation between brightness L1 and L2 and represents the content of the graph base table 26 stored in the ROM 23 shown in FIG. 1. The content of the graph base table 26 shown in FIG. 7 represents a relation between the previous brightness and the next brightness for the LC cell 32 having the characteristic shown in FIG. 2, by taking the effect shown in FIG. 6 into consideration. The previous brightness can be obtained from a video signal input through the ASIC21 shown in FIG. 1 and stored in the frame buffer 22. The next brightness can be obtained from the next video signal input to the ASIC 21. The graph base table 26 is constructed for each of the R, G, B color signals and the values in the table vary depending on the characteristic of the LC cell 32.

9:26-39

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “IDEAL  
QUANTITY OF LIGHT IN A STATIONARY STATE” (cont'd)**

[Figure 7]

26 (Graph base table)

Next brightness Previous brightness	0	10	20	30	40	50	60	70	80	90	100
0	0	28	48	63	74	83	88	93	96	98	100
10	0	10	30	45	56	65	70	75	80	90	100
20	0	10	20	35	46	55	60	70	80	90	100
30	0	10	20	30	41	50	60	70	80	90	100
40	0	10	20	30	40	50	60	70	80	90	100
50	0	10	20	30	40	50	60	70	80	90	100
60	0	10	20	30	40	50	60	70	80	90	100
70	0	10	20	30	40	50	59	70	80	90	100
80	0	10	20	30	40	45	54	65	80	90	100
90	0	10	20	25	30	35	44	55	70	90	100
100	0	2	4	7	12	17	26	38	52	72	100

The first row of the graph base table 26 shown in FIG. 7 indicates brightness output for the next brightness when the previous brightness is 0 and match the readings of the R signal in the moving state line 50 in the graph shown in FIG. 2. For example, if the next brightness is “10”, find a value

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41. In this embodiment, if a difference between the previous brightness and the next brightness is greater than an offset, the next brightness is output without change. For example,

9:40-58

**INTRINSIC EVIDENCE FOR DISPUTED TERM “AN OFFSET FOR MAKING THE TIME INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE SUBSTANTIALLY EQUAL TO AN IDEAL QUANTITY WHICH IS THE BRIGHTNESS IN A STATIONARY STATE TO SAID SECOND BRIGHTNESS INFORMATION”**

The term “response time” used in the industry refers to the sum of (1) time required to reverse color by applying a voltage to a liquid crystal cell and (2) time required to restore the original color by the removal of the applied voltage. The term “frame” used in the industry represents the

1:39-43

In Published Unexamined Japanese Patent Application No. 2-153687, a LCD is provided which is configured to discriminate between a static image area having less motion and a fast-moving area and apply a signal process only to the moving area to emphasize time-based changes in an image, thereby improving response time in the image area where better response time is required to reduce visual persistence and noise.

In Published Unexamined Japanese Patent Application No. 4-365094, a LCD is provided which is configured to be driven by reading pre-stored optimum image data according to the direction and degree of a change when the image data changes, thereby allowing the LCD to rapidly follow the fast-changing image.

In Published Unexamined Japanese Patent Application No. 6-62355, a technology is disclosed which superposes a difference component between fields or frames on a video

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In Published Unexamined Japanese Patent Application No. 7-56532, a technology is disclosed which provides table memory containing a table of image increase/decrease values and drive a liquid crystal panel (liquid crystal cell) by performing an addition/subtraction in order to improve response changes due to changes in the gray scale in the liquid crystal panel. However, the amount to be added or subtracted is expressed only by the word “optimum” and no specific amount is disclosed.

1:50-2:12

**INTRINSIC EVIDENCE FOR DISPUTED TERM “AN OFFSET FOR MAKING THE TIME INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE SUBSTANTIALLY EQUAL TO AN IDEAL QUANTITY WHICH IS THE BRIGHTNESS IN A STATIONARY STATE TO SAID SECOND BRIGHTNESS INFORMATION” (cont'd)**

The “ideal quantity of light” herein is, to take an example, the quantity of light based on a response characteristic which provides a target brightness level at a time point at which the frame is turned on and provides a brightness level of zero at the time point at which the frame is turned off on a display device in which each pixel is driven for each frame. The brightness level can be represented as a target brightness value by a gray scale and considered as an indication of the characteristic of human visual sensation to brightness. In addition, a brightness change can be considered as a response characteristic depending on the types of liquid crystal cells (liquid crystal panels). Quantity of light is considered as a time integration quantity of a brightness change and can be expressed as brightness\_time, if the brightness is constant. The representation “substantially

4:42-56

The determinant is characterized by comprising a table for storing a brightness level determined by the characteristic of a liquid crystal cell according to a relation between the previous brightness level and the next brightness level, and determining an output brightness level by modifying the next brightness level based on the brightness level read from the table. With this configuration, flicker due to changes in

4:61-67

**INTRINSIC EVIDENCE FOR DISPUTED TERM “AN OFFSET FOR MAKING THE TIME INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE SUBSTANTIALLY EQUAL TO AN IDEAL QUANTITY WHICH IS THE BRIGHTNESS IN A STATIONARY STATE TO SAID SECOND BRIGHTNESS INFORMATION” (cont'd)**

The offset set by the setting elements can be determined based on a time integration quantity, which is a change in brightness in the moving-state vide signal integrated with respect to time, and the quantity of light in stationary state, thus a difference in brightness can be preferably reduced in consideration of the human visual perception characteristic to inhibit flicker appropriately.

The moving-state video signal passed through the input consists of a plurality of color signals, the offset set by the setting elements is determined for each of the color signals, and the generator generates the output video signal for each color signal based on the offset determined for each color signal. Thus a difference in brightness between moving and stationary states can be corrected for each color signal to inhibit flicker on a color image display.

5:16-30

The apparatus further comprises a frame buffer for storing the brightness information of the input wire-frame model as the previous brightness, and characterized by that the storage portion stores the offset as table information based on a relation between the previous brightness stored in the frame buffer and the brightness of the next input wire-frame model, thus, flicker in a moving state can be advantageously inhibited without providing separate determining units for moving and stationary states.

5:31-39

In another category, the present invention is a flicker inhibition method for inhibiting flicker caused by a difference in brightness when an input wire-frame model is displayed by a liquid crystal cell. The method is characterized by storing a relation between brightness in a stationary state in which a wire-frame model having a predetermined gray scale is displayed on a particular pixel across a plurality of frames and brightness in a moving state in which the wire-frame model having the predetermined gray scale changes frame to frame with respect to the particular pixel, applying an offset based on the stored relation to the gray scale of the wire-frame model if the input wire-frame model is in a moving state, and driving the liquid crystal cell based on the gray scale to which the offset is applied to display the wire-frame model.

5:51-65

**INTRINSIC EVIDENCE FOR DISPUTED TERM “AN OFFSET FOR MAKING THE TIME INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE SUBSTANTIALLY EQUAL TO AN IDEAL QUANTITY WHICH IS THE BRIGHTNESS IN A STATIONARY STATE TO SAID SECOND BRIGHTNESS INFORMATION” (cont'd)**

The moving state brightness used for storing the relation is the brightness when the particular pixel changes back to the off state one frame after it is driven from the off state to the on state during the passage of the wire-frame model over the particular pixel.

Furthermore, the brightness in the moving state which is used when the relation is stored is the quantity of light equal to the brightness change integrated with respect to time.

5:66-6:6

Viewing the present invention as a liquid crystal driving method, the liquid crystal driving method of the present invention is characterized by the steps of storing first brightness information for an input pixel in a frame buffer, and applying, based on second brightness information for the next input pixel and the first brightness information stored in the frame buffer, an offset for making the time integration quantity of a brightness change substantially equal to an ideal light quantity which is brightness in a stationary state to the second brightness information. The steps further include the outputting of the second brightness information to which the offset is applied to a driving circuit for driving an liquid crystal cell, and storing the second brightness information for the input pixel in a frame buffer. This liquid crystal driving method allows the inhibition of flicker by using a simple apparatus without globally determining whether a model is moving or stationary.

6:11-27

The offset applying step is characterized by the step of reading a pre-stored offset based on the relation between the first and second brightness information and applying the read offset to the second brightness information.

6:37-40

**INTRINSIC EVIDENCE FOR DISPUTED TERM “AN OFFSET FOR MAKING THE TIME INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE SUBSTANTIALLY EQUAL TO AN IDEAL QUANTITY WHICH IS THE BRIGHTNESS IN A STATIONARY STATE TO SAID SECOND BRIGHTNESS INFORMATION” (cont'd)**

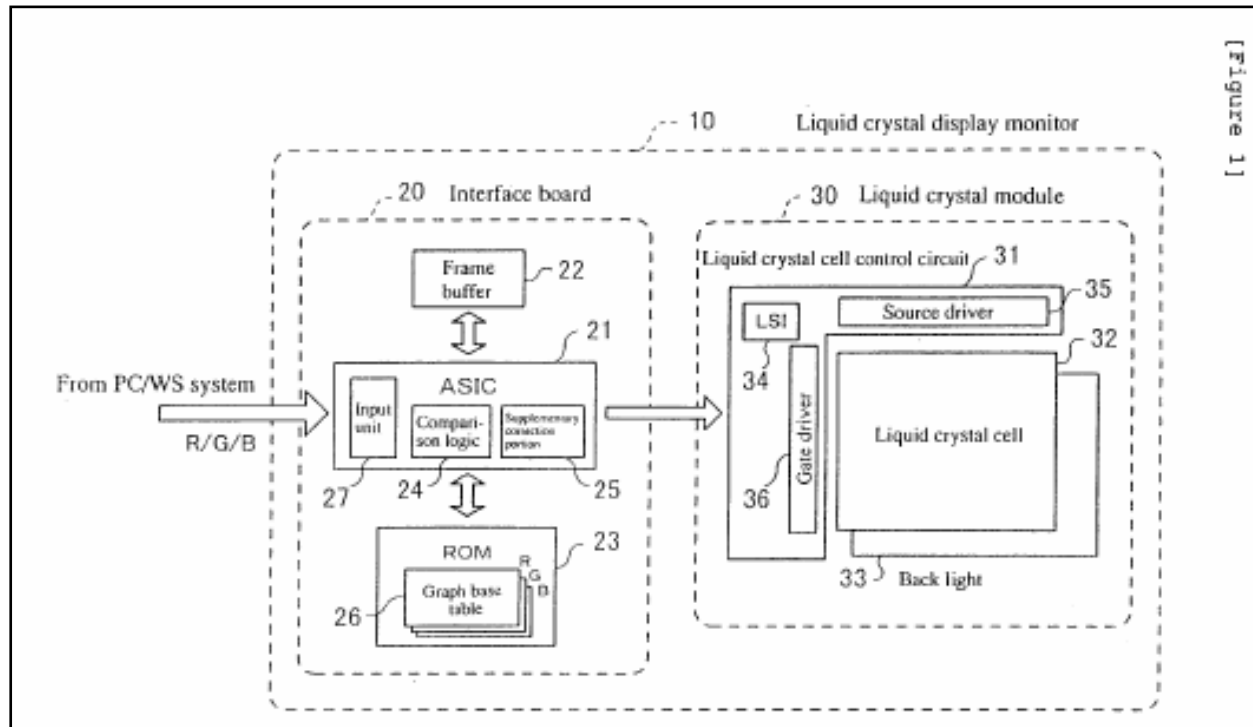


FIG. 1 is a drawing for showing the overall configuration of a liquid crystal display according to an embodiment of the present invention. Reference number 10 denotes a liquid

6:50-53

The I/F board 20 comprises an input unit 27 for inputting video data from a host such as a PC/WS system, a comparison logic 24 for comparing the previous brightness with the next brightness for an input video signal, and an Application-Specific Integrate Circuit (ASIC) 21 including a logic having units such as a supplementary correction portion 25 for performing a supplementary correction. The I/F board 20 also comprises a frame buffer 22 for temporarily storing the input video signal and read-only memory (ROM) 23 containing information needed for the operation of the ASIC 21. The frame buffer 22 stores input video signal value

6:66-7:9

**INTRINSIC EVIDENCE FOR DISPUTED TERM “AN OFFSET FOR MAKING THE TIME INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE SUBSTANTIALLY EQUAL TO AN IDEAL QUANTITY WHICH IS THE BRIGHTNESS IN A STATIONARY STATE TO SAID SECOND BRIGHTNESS INFORMATION” (cont'd)**

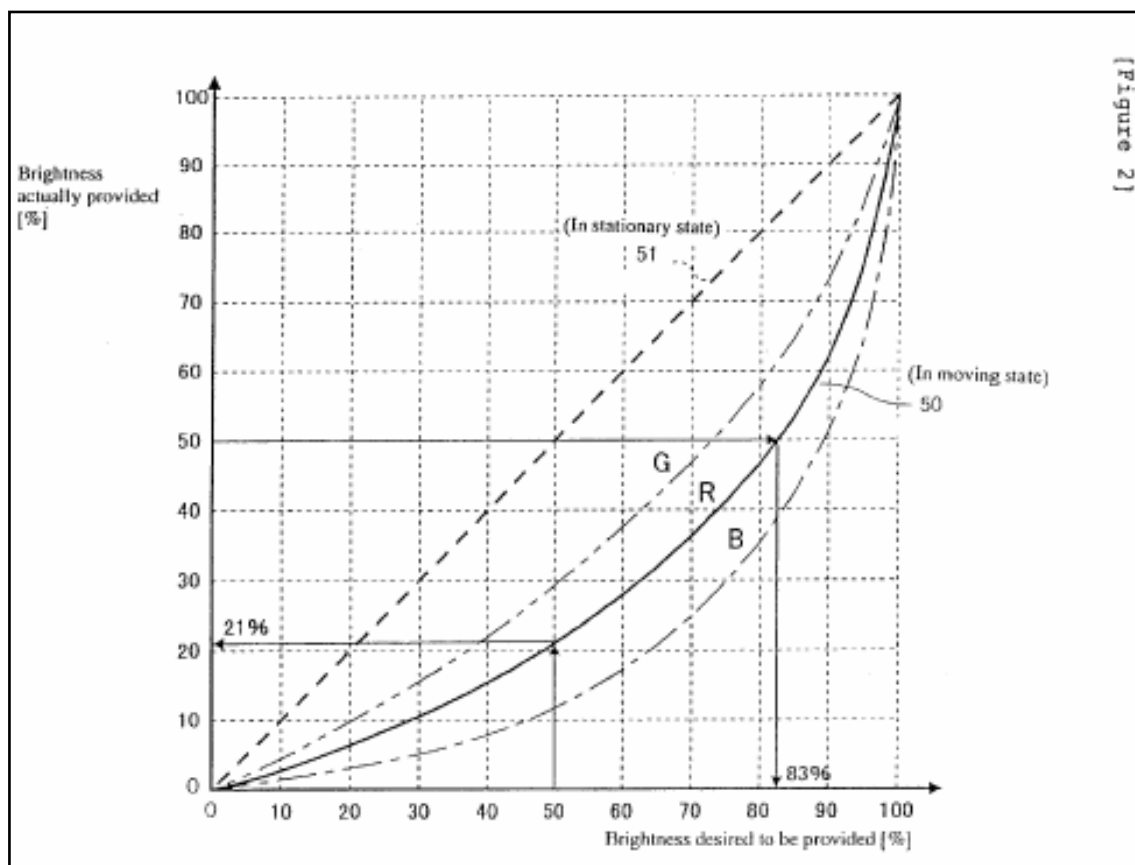


FIG. 2 is a graph showing an example of the brightness of a wire-frame model moving on the LCD panel used in this embodiment. The horizontal scale indicates brightness (%) desired to be provided and the vertical scale indicates brightness (%) actually provided in the Figure. The dashed line 51 indicates the relationship between the desired brightness and actual brightness of the model in a stationary state. The solid line 50 indicates the relationship between the desired brightness and actual brightness of the model in a moving state for an R (red) signal. The alternate long and short two dashes line indicates a G (green) signal in the moving state and the alternate long and short one dash line indicates a B (blue) signal in the moving state. The characteristics in the moving state vary from LCD panel to LCD panel.

7:31-45

**INTRINSIC EVIDENCE FOR DISPUTED TERM “AN OFFSET FOR MAKING THE TIME INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE SUBSTANTIALLY EQUAL TO AN IDEAL QUANTITY WHICH IS THE BRIGHTNESS IN A STATIONARY STATE TO SAID SECOND BRIGHTNESS INFORMATION” (cont'd)**

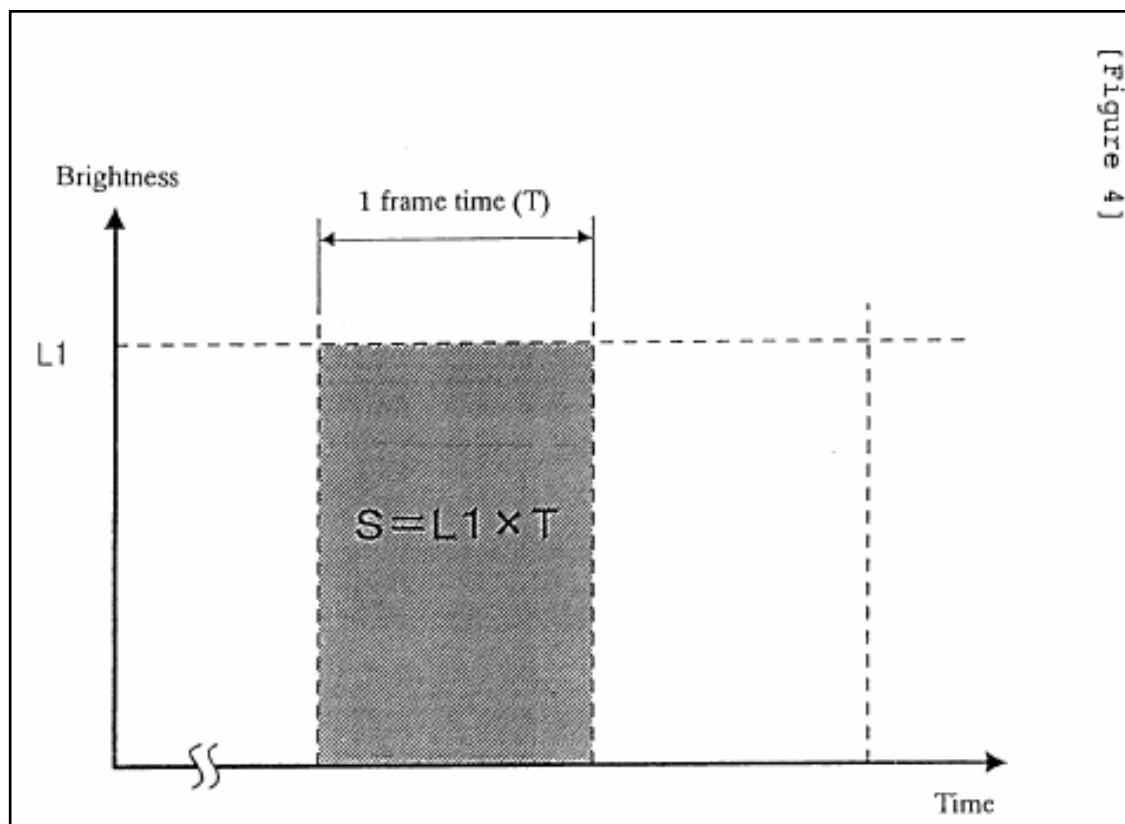


FIG. 4 shows the response characteristic of an ideal liquid crystal and indicates the state in which a particular pixel is kept lit up at a brightness of L1, that is in a stationary state. Here, the quantity of light (S) emitted in one frame time (T) is equal to  $L1 \times T$  (i.e. brightness  $\times$  time) as shown in the shaded area in FIG. 4.

8:35-40

**INTRINSIC EVIDENCE FOR DISPUTED TERM “AN OFFSET FOR MAKING THE TIME INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE SUBSTANTIALLY EQUAL TO AN IDEAL QUANTITY WHICH IS THE BRIGHTNESS IN A STATIONARY STATE TO SAID SECOND BRIGHTNESS INFORMATION” (cont'd)**

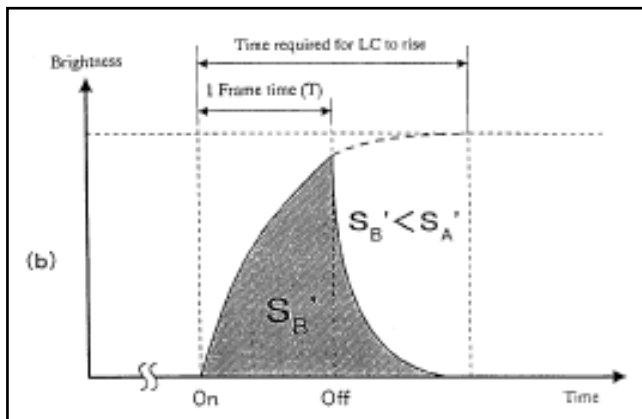
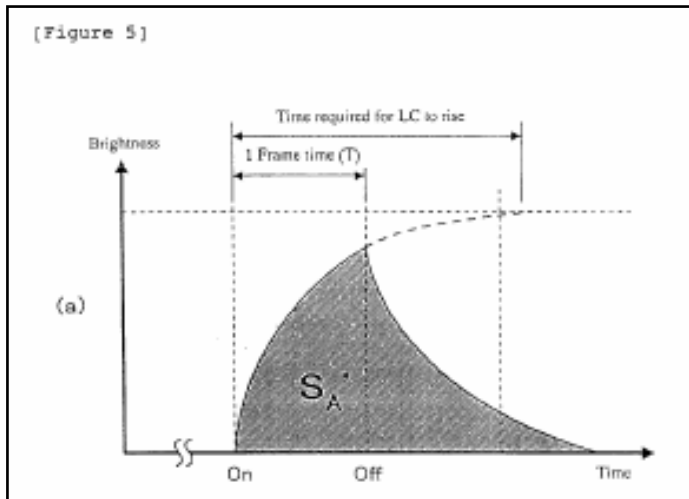
61 Model (Magnitude of flicker)	62 Response rising time	63 Response falling time	64 Light quantity ratio (to ideal LC)	65 Brightness ratio of drawing in moving state to that in stationary state
Model A (○)	20.3ms	21.6ms	1.02 : 1	1.0 : 1
Model B (×)	18.5ms	10.0ms	0.81 : 1	0.8 : 1
Model C (△)	10.0ms	4.5ms	0.85 : 1	0.9 : 1
Model D (×)	19.9ms	7.9ms	0.73 : 1	0.7 : 1
Model E (×)	43.2ms	34.3ms	0.53 : 1	0.3 : 1

[Figure 3]

FIGS. 5A and 5B show the response characteristic represented by brightness versus time when a pixel stays lit up for one frame time (On→Off) in models A, B shown in FIG. 3. Both of the rising and falling of the response of model A

8:41-44

**INTRINSIC EVIDENCE FOR DISPUTED TERM “AN OFFSET FOR MAKING THE TIME INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE SUBSTANTIALLY EQUAL TO AN IDEAL QUANTITY WHICH IS THE BRIGHTNESS IN A STATIONARY STATE TO SAID SECOND BRIGHTNESS INFORMATION” (cont'd)**



FIGS. 5A and 5B show the response characteristic represented by brightness versus time when a pixel stays lit up for one frame time (On→Off) in models A, B shown in FIG. 3. Both of the rising and falling of the response of model A

8:41-44

**INTRINSIC EVIDENCE FOR DISPUTED TERM “AN OFFSET FOR MAKING THE TIME INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE SUBSTANTIALLY EQUAL TO AN IDEAL QUANTITY WHICH IS THE BRIGHTNESS IN A STATIONARY STATE TO SAID SECOND BRIGHTNESS INFORMATION” (cont'd)**

[Figure 7]

26 (Graph base table)

Next brightness Previous brightness	0	10	20	30	40	50	60	70	80	90	100
0	0	28	48	63	74	83	88	93	96	98	100
10	0	10	30	45	56	65	70	75	80	90	100
20	0	10	20	35	46	55	60	70	80	90	100
30	0	10	20	30	41	50	60	70	80	90	100
40	0	10	20	30	40	50	60	70	80	90	100
50	0	10	20	30	40	50	60	70	80	90	100
60	0	10	20	30	40	50	60	70	80	90	100
70	0	10	20	30	40	50	59	70	80	90	100
80	0	10	20	30	40	45	54	65	80	90	100
90	0	10	20	25	30	35	44	55	70	90	100
100	0	2	4	7	12	17	26	38	52	72	100

FIG. 7 is a table showing a relation between brightness L1 and L2 and represents the content of the graph base table 26 stored in the ROM 23 shown in FIG. 1. The content of the graph base table 26 shown in FIG. 7 represents a relation between the previous brightness and the next brightness for the LC cell 32 having the characteristic shown in FIG. 2, by taking the effect shown in FIG. 6 into consideration. The previous brightness can be obtained from a video signal input through the ASIC21 shown in FIG. 1 and stored in the frame buffer 22. The next brightness can be obtained from the next video signal input to the ASIC 21. The graph base table 26 is constructed for each of the R, G, B color signals and the values in the table vary depending on the characteristic of the LC cell 32.

9:26-39

**INTRINSIC EVIDENCE FOR DISPUTED TERM “AN OFFSET FOR MAKING THE TIME INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE SUBSTANTIALLY EQUAL TO AN IDEAL QUANTITY WHICH IS THE BRIGHTNESS IN A STATIONARY STATE TO SAID SECOND BRIGHTNESS INFORMATION” (cont'd)**

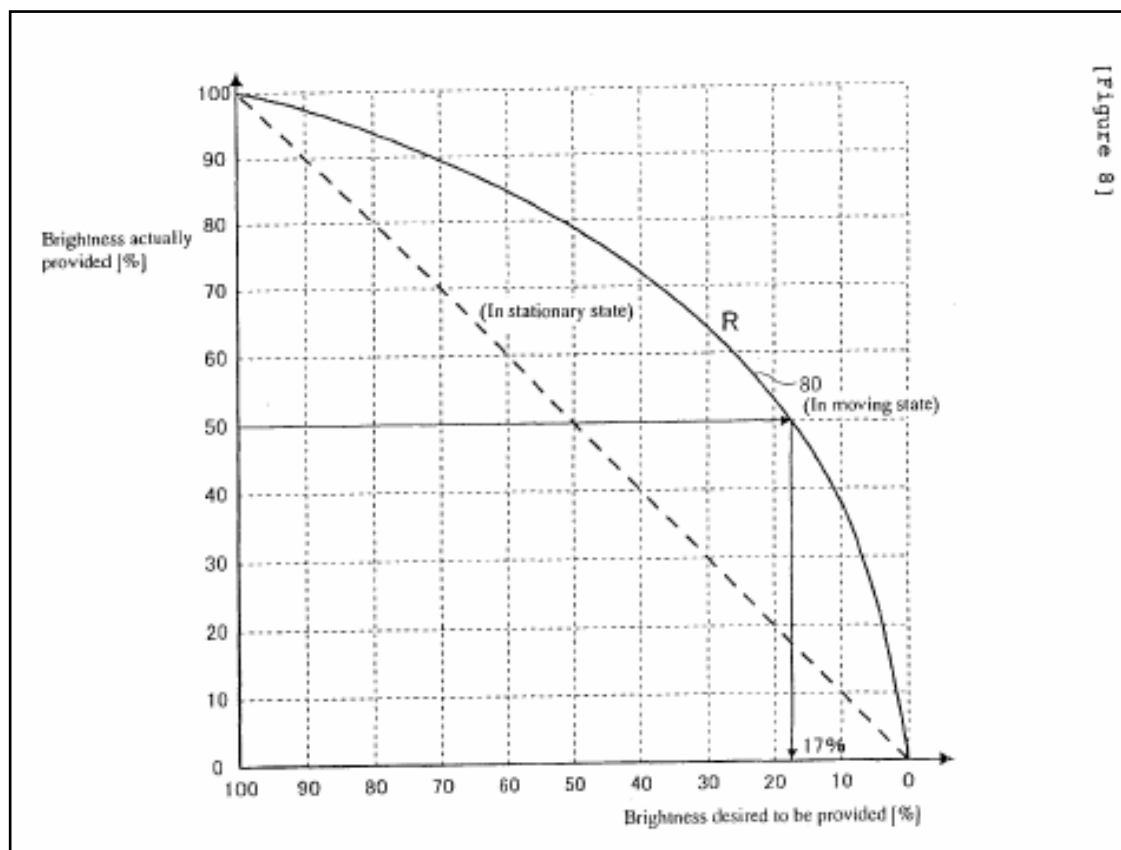


FIG. 8 is a graph showing brightness desired to be provided versus brightness provided actually when brightness falls. The liquid crystal in the example in FIG. 8 has brightness which falls with exhibiting a characteristic similar to the rising characteristic shown in FIG. 2. Accordingly, the line 80 indicating a moving state shown in FIG. 8 is the vertically-flipped curve of the line 50 in a moving state shown in FIG. 2. Tick mark labels on the horizontal scale are also inverted. As can be seen from the graph, when the brightness actually provided is 50%, the brightness desired to be provided is 17%. This matches the value when the previous brightness is 100 and the next brightness is 50 in the table in FIG. 7. That is, the moving state line 80 in FIG. 8 exactly indicates the fall of the previous brightness from 100% in FIG. 7.

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**INTRINSIC EVIDENCE FOR DISPUTED TERM “AN OFFSET FOR MAKING THE TIME INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE SUBSTANTIALLY EQUAL TO AN IDEAL QUANTITY WHICH IS THE BRIGHTNESS IN A STATIONARY STATE TO SAID SECOND BRIGHTNESS INFORMATION” (cont'd)**

As described above, the embodiment is configured to store offsets in table form based on the relation between a brightness level in a stationary state and that in a moving state in order to obtain an ideal quantity of light. Thus, even during the movement of a display image on the LCD screen, the image can be displayed virtually the same brightness to the eye as in its stationary state, thereby inhibiting flicker on the screen.

In addition, the embodiment is configured to store the previous brightness level (gray scale value) in the frame buffer 22 and a supplementary correction is made by the ASIC 21 using the data in the graph base table 26 based on the relation between the brightness level of the next video data and the previous brightness level. Thus, whether a wire-frame model is moving or stationary is not required to be determined. Instead, the movement of the model can be determined from a difference between the determined brightness and the previous brightness. As a result, flicker can be inhibited by a simple circuit configuration.

10:49-67

**EXHIBIT \_\_\_\_\_**  
**U.S. PATENT NO. 6,778,160**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 1**

1. A liquid crystal display, comprising:  
 an input logic for inputting a video signal from a host;  
 a storage for storing the previous brightness level of the video signal input through said input logic;  
 a determinator for determining an output brightness level based on the previous brightness level stored in said storage and the next brightness level of the next video signal input to said input logic so as to make a **time integration quantity of a brightness change substantially equal** to an ideal quantity of light in a stationary state with respect to the next brightness level; and  
 a driver for driving an **image displaying liquid crystal cell** based on said output brightness level determined by said determination logic.

**ASSERTED CLAIM 12**

12. A liquid crystal driving method, comprising the steps of:  
 storing **first brightness information for an input pixel** in a frame buffer;  
 applying based on second brightness information for the next input pixel and said first brightness information stored in said frame buffer an offset for making the time integration quantity of a brightness change substantially equal to an ideal light quantity which is the brightness in a stationary state to said second brightness information;  
 outputting said second brightness information to which said offset is applied to a driving circuit for driving an liquid crystal cell; and  
 storing said second brightness information for the input pixel in a frame buffer.

**LGD's Claim Construction**

**image displaying liquid crystal cell** - an image display element with a liquid crystal that has the ideal response characteristic at the maximum brightness change given the predetermined range of brightness levels.

**pixel** - an image display element with a liquid crystal that has the ideal response characteristic at the maximum brightness change.

**frame buffer** - a memory circuit or device that temporarily holds brightness levels for all pixels that form one complete picture on the liquid crystal display.

**substantially equal<sup>2</sup>** – Indefinite or a level which is not completely the same but can be accepted as a substantially equivalent level, and includes a level which is closer to an ideal quantity of light than no preventive measures are taken

<sup>1</sup> Disputed Term “time integration quantity of a brightness change substantially equal” also appears in asserted Claim 12 in the same context.

<sup>2</sup> Disputed Term “substantially equal” also appears in asserted Claim 12 in the same context.

## **INTRINSIC EVIDENCE FOR DISPUTED TERMS “IMAGE DISPLAYING LIQUID CRYSTAL CELL” AND “PIXEL”**

In CAD applications, a wire-frame model is typically displayed using many thin lines in white or other colors against a black background. Assuming that the wire-model is white (all of the colors R (red)/G (green)/B (blue) are “ON”) as an example, no problem arises when the model stay stationary on the screen because only a few frames are required to achieve an proper brightness. However, if the operator move the model on the screen, the proper brightness cannot completely be achieved. That is, if a pixel is made light up only in one frame, the brightness of the pixel may not reach the predetermined brightness because the response of the LCD itself is slow as mentioned above. This situation will be described below with reference to the drawings.

2:26-39

FIG. 9 shows the movement of lines when a wire-frame model is moved on the screen. FIG. 10 shows on/off states of the pixels on line (i) in each frame at the time point in FIG. 9. FIG. 11 shows a change in the brightness of pixel (j).

Herein, as shown in FIG. 9, in the case where attention is paid to a particular pixel, assuming that a line of the wire frame 200 moves through frames (n-1) 201 to (n) 202 to (n+1) 203 in sequence. That is, the pixel lights up in a time period equivalent to the frames in which the line passes over the pixel and goes off immediately after that.

2:40-49

Focusing attention on line (i) 205 represented by a dashed line, in particular, on the particular pixel, each frame is driven from OFF to ON by the movement of pixel (j) 206, then one frame after goes back from ON to OFF, as shown in FIG. 10. However, because the response time of commonly-used liquid crystals is longer than 16.7 ms, pixel (j) 206 changes back to black before completely returning from black to white. That is, as shown in FIG. 11, pixel (j) 206 is OFF in frame (n-1) 201, goes ON in frame (n) 202, then goes OFF in frame (n+1) 203. However, the target brightness of pixel (j) 206 is not reached even though it is turned on in order to achieve 100% brightness in frame (n) 202. As a result, the brightness of the line drawing during movement will be low. The inventors have found that when a wire-frame model is continuously moved in a CAD application, the wire-frame model in fact repeatedly alternates between moving and stationary states every several frames and blinks due to a difference in display brightness between the moving and stationary states, and this difference causes “flicker.”

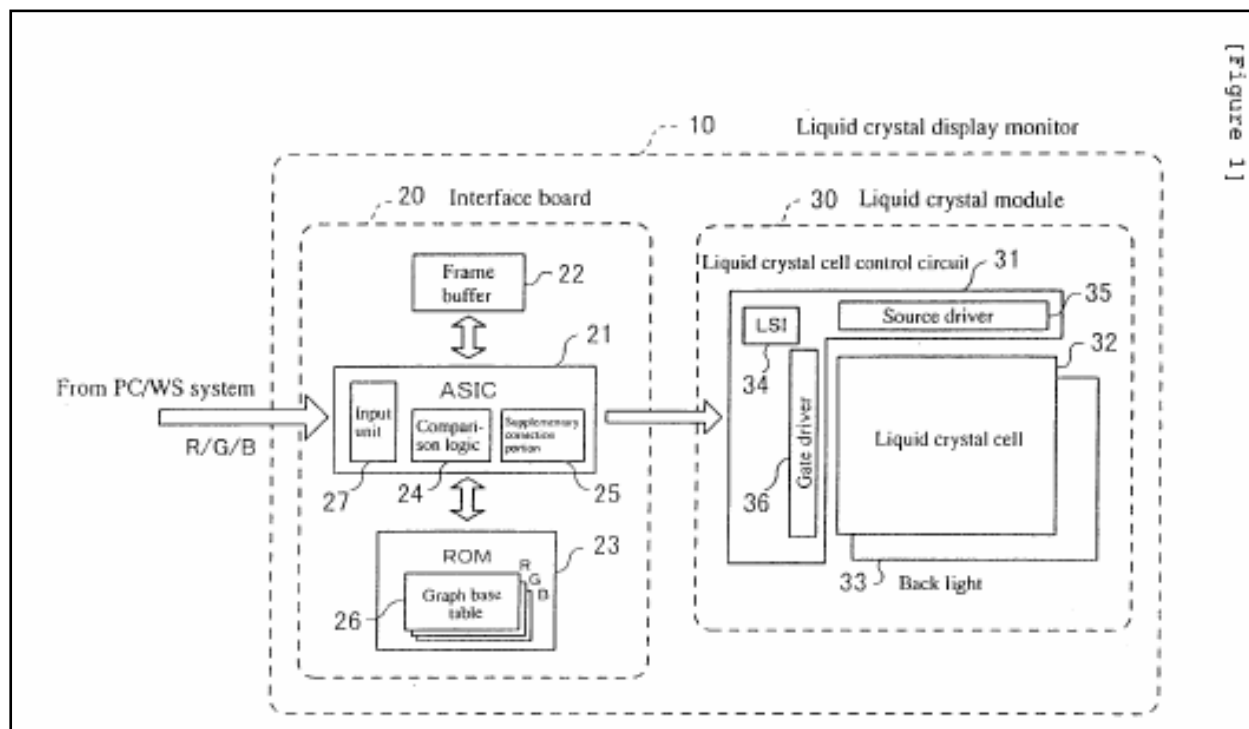
2:50-3:2

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “IMAGE  
DISPLAYING LIQUID CRYSTAL CELL” AND “PIXEL” (cont'd)**

Because the wire-frame model in the present invention is a model consisting of a large number of thin lines in white or other colors in a CAD application, for example, in which flicker is especially troublesome, the flicker inhibition by correcting gray scale of such a wire-frame model in a moving state is highly effective.

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**INTRINSIC EVIDENCE FOR DISPUTED TERMS “IMAGE DISPLAYING LIQUID CRYSTAL CELL” AND “PIXEL” (cont'd)**



[Figure 1]

FIG. 1 is a drawing for showing the overall configuration of a liquid crystal display according to an embodiment of the present invention. Reference number 10 denotes a liquid

6:51-53

The I/F board 20 comprises a input unit 27 for inputting video data from a host such as a PC/WS system, a comparison logic 24 for comparing the previous brightness with the next brightness for an input video signal, and an Application-Specific Integrate Circuit (ASIC) 21 including a logic having units such as a supplementary correction portion 25 for performing a supplementary correction. The I/F board 20 also comprises a frame buffer 22 for temporarily storing the input video signal and read-only memory (ROM) 23 containing information needed for the operation of the ASIC 21. The frame buffer 22 stores input video signal value

6:66-7:9

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “IMAGE  
DISPLAYING LIQUID CRYSTAL CELL” AND “PIXEL” (cont'd)**

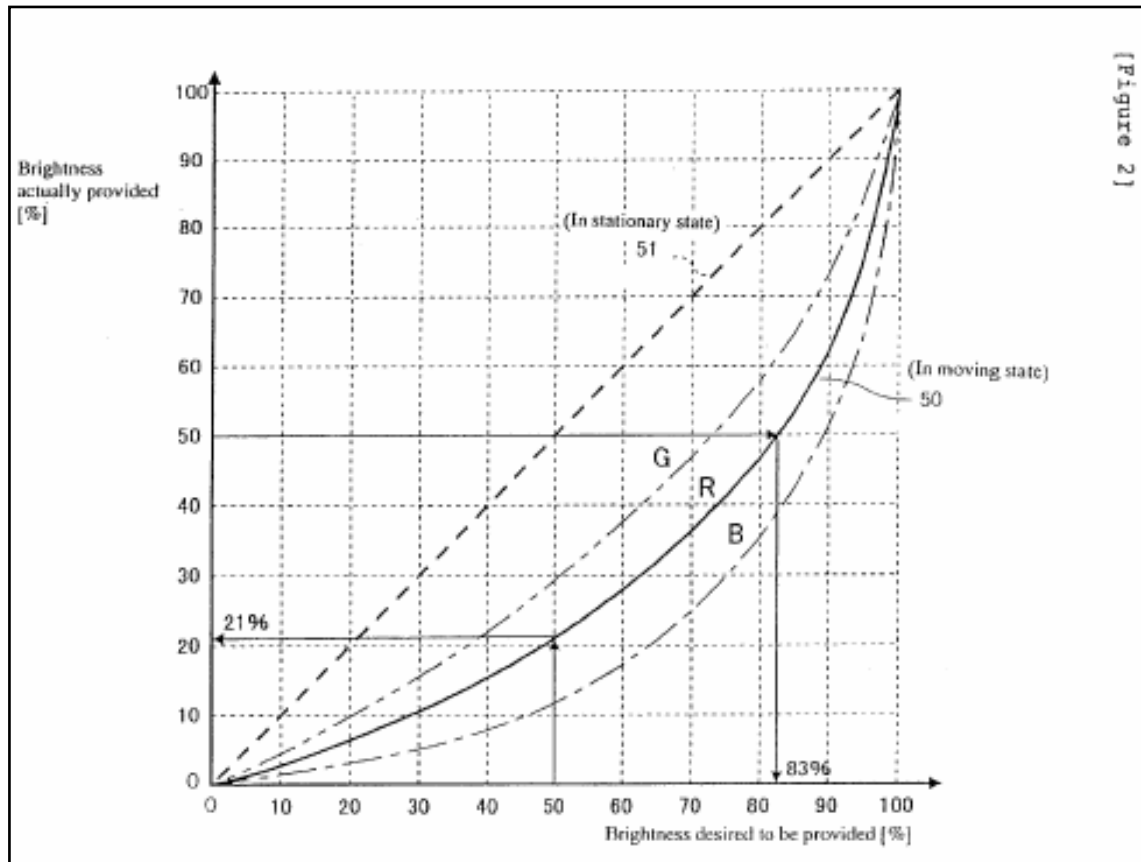


FIG. 2 is a graph showing an example of the brightness of a wire-frame model moving on the LCD panel used in this embodiment. The horizontal scale indicates brightness (%) desired to be provided and the vertical scale indicates brightness (%) actually provided in the Figure. The dashed line 51 indicates the relationship between the desired brightness and actual brightness of the model in a stationary state. The solid line 50 indicates the relationship between the desired brightness and actual brightness of the model in a moving state for an R (red) signal. The alternate long and short two dashes line indicates a G (green) signal in the moving state and the alternate long and short one dash line indicates a B (blue) signal in the moving state. The characteristics in the moving state vary from LCD panel to LCD panel.

7:31-45

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “IMAGE DISPLAYING LIQUID CRYSTAL CELL” AND “PIXEL” (cont'd)**

[Figure 3]

61 Model (Magnitude of flicker)	62 Response rising time	63 Response falling time	64 Light quantity ratio (to ideal LC)	65 Brightness ratio of drawing in moving state to that in stationary state
Model A (○)	20.3ms	21.6ms	1.02 : 1	1.0 : 1
Model B (×)	18.5ms	10.0ms	0.81 : 1	0.8 : 1
Model C (△)	10.0ms	4.5ms	0.85 : 1	0.9 : 1
Model D (×)	19.9ms	7.9ms	0.73 : 1	0.7 : 1
Model E (×)	43.2ms	34.3ms	0.53 : 1	0.3 : 1

FIG. 3 is a table showing the measurements of the response time of liquid crystal at the maximum brightness in five LCD models (models A to E). In a model 61 shown in the first column, the symbol in parentheses indicates the magnitude of flicker at the maximum brightness. Symbol “○” indicates that almost no flicker is visually perceived, symbol “△” indicates that flicker level is quite acceptable,

7:66-8:5

In terms of whether the response at the maximum brightness is adequately fast, both of the response rising time 62 and the falling time 63 of model A is poor compared to model B. However, when a wire-frame model in an actual CAD application is displayed and moved on these LCD models, flicker in model A is less than in model B. The

7:20-25

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “IMAGE  
DISPLAYING LIQUID CRYSTAL CELL” AND “PIXEL” (cont'd)**

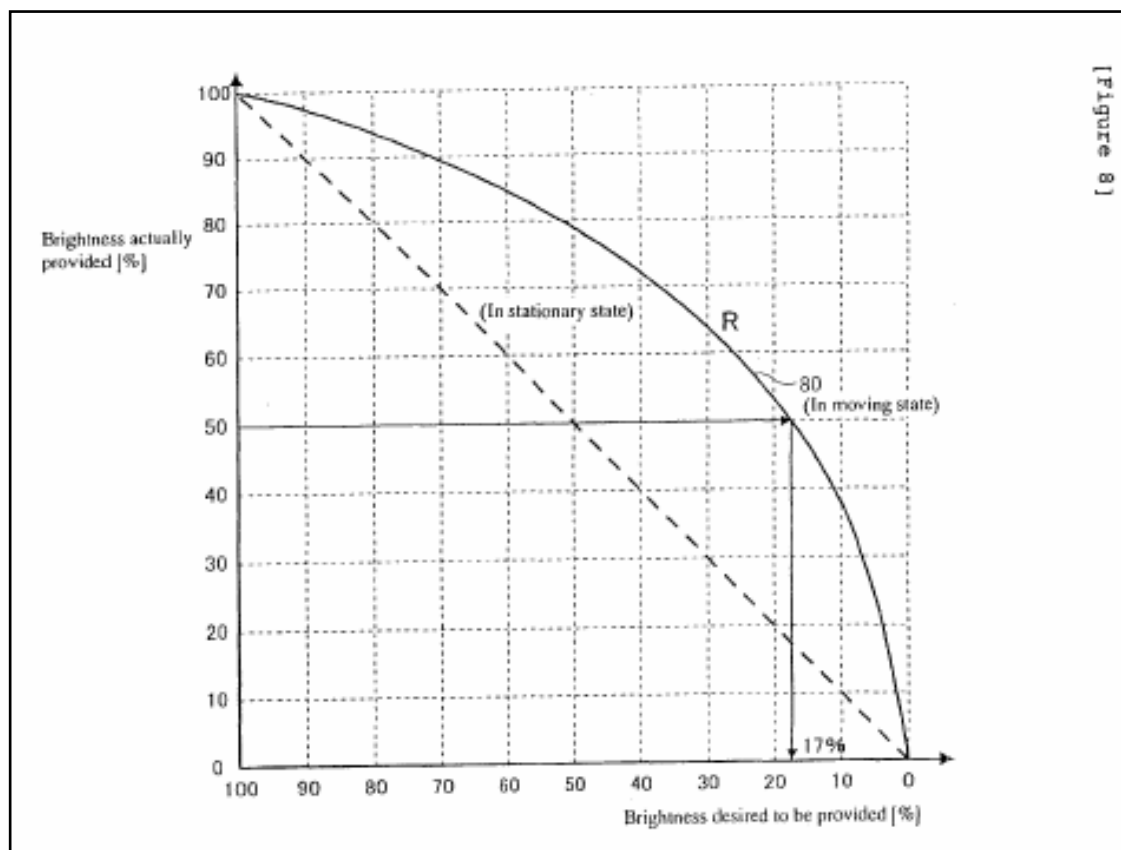


FIG. 8 is a graph showing brightness desired to be provided versus brightness provided actually when brightness falls. The liquid crystal in the example in FIG. 8 has brightness which falls with exhibiting a characteristic similar to the rising characteristic shown in FIG. 2. Accordingly, the line 80 indicating a moving state shown in FIG. 8 is the vertically-flipped curve of the line 50 in a moving state shown in FIG. 2. Tick mark labels on the horizontal scale are also inverted. As can be seen from the graph, when the brightness actually provided is 50%, the brightness desired to be provided is 17%. This matches the value when the previous brightness is 100 and the next brightness is 50 in the table in FIG. 7. That is, the moving state line 80 in FIG. 8 exactly indicates the fall of the previous brightness from 100% in FIG. 7.

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**INTRINSIC EVIDENCE FOR DISPUTED TERM “FRAME BUFFER”**

The apparatus further comprises a frame buffer for storing the brightness information of the input wire-frame model as the previous brightness, and characterized by that the storage portion stores the offset as table information based on a relation between the previous brightness stored in the frame buffer and the brightness of the next input wire-frame model, thus, flicker in a moving state can be advantageously inhibited without providing separate determining units for moving and stationary states.

5:31-39

Viewing the present invention as a liquid crystal driving method, the liquid crystal driving method of the present invention is characterized by the steps of storing first brightness information for an input pixel in a frame buffer, and applying, based on second brightness information for the next input pixel and the first brightness information stored in the frame buffer, an offset for making the time integration quantity of a brightness change substantially equal to an ideal light quantity which is brightness in a stationary state to the second brightness information. The steps further include the outputting of the second brightness information to which the offset is applied to a driving circuit for driving an liquid crystal cell, and storing the second brightness information for the input pixel in a frame buffer. This liquid crystal driving method allows the inhibition of flicker by using a simple apparatus without globally determining whether a model is moving or stationary.

6:11-27

**INTRINSIC EVIDENCE FOR DISPUTED TERM “FRAME BUFFER”**  
**(cont'd)**

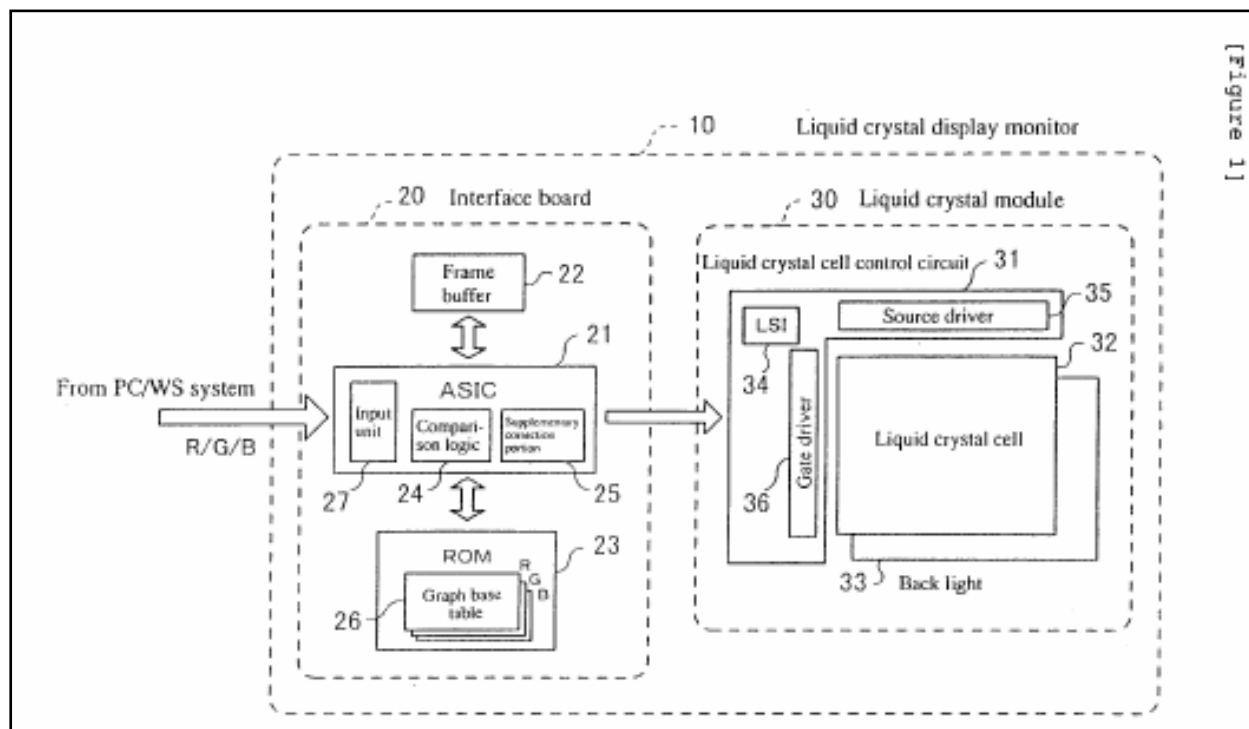


FIG. 1 is a drawing for showing the overall configuration of a liquid crystal display according to an embodiment of the present invention. Reference number 10 denotes a liquid

6:51-53

The I/F board 20 comprises a input unit 27 for inputting video data from a host such as a PC/WS system, a comparison logic 24 for comparing the previous brightness with the next brightness for an input video signal, and an Application-Specific Integrate Circuit (ASIC) 21 including a logic having units such as a supplementary correction portion 25 for performing a supplementary correction. The I/F board 20 also comprises a frame buffer 22 for temporarily storing the input video signal and read-only memory (ROM) 23 containing information needed for the operation of the ASIC 21. The frame buffer 22 stores input video signal value

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# INTRINSIC EVIDENCE FOR DISPUTED TERM "FRAME BUFFER" (cont'd)

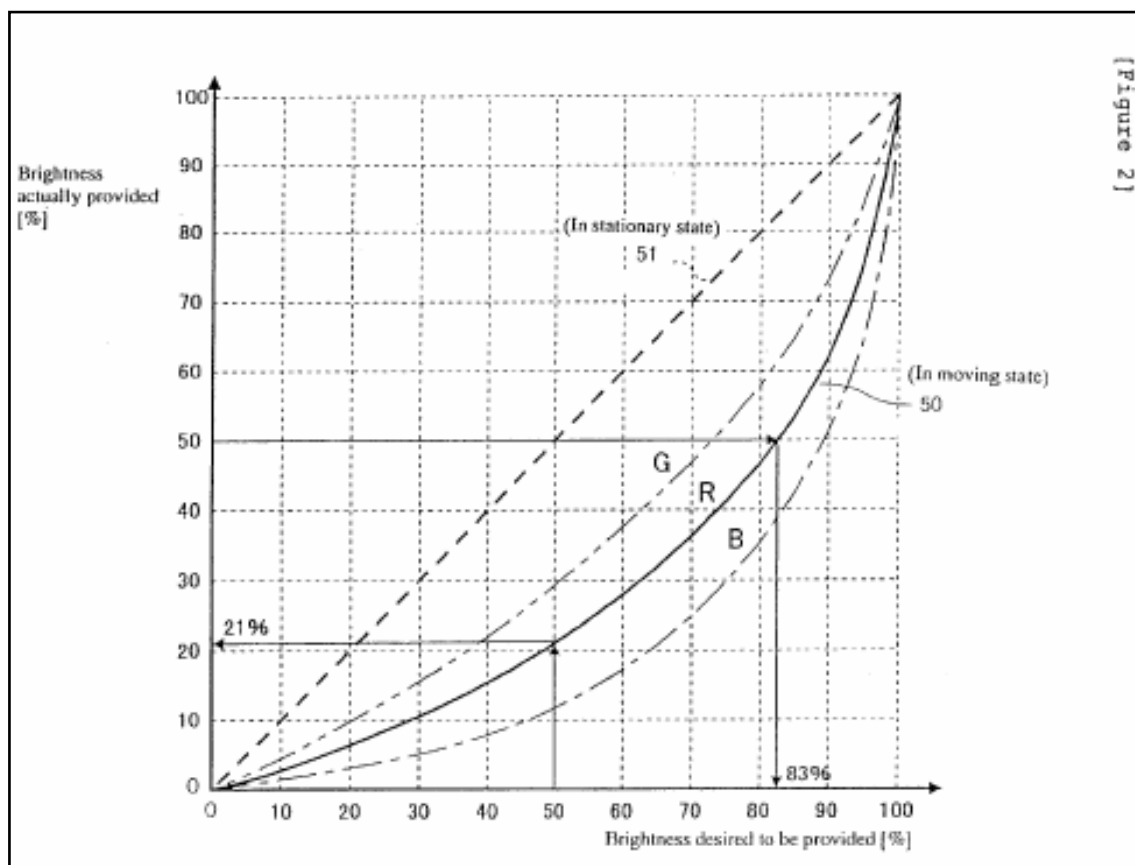


FIG. 2 is a graph showing an example of the brightness of a wire-frame model moving on the LCD panel used in this embodiment. The horizontal scale indicates brightness (%) desired to be provided and the vertical scale indicates brightness (%) actually provided in the Figure. The dashed line 51 indicates the relationship between the desired brightness and actual brightness of the model in a stationary state. The solid line 50 indicates the relationship between the desired brightness and actual brightness of the model in a moving state for an R (red) signal. The alternate long and short two dashes line indicates a G (green) signal in the moving state and the alternate long and short one dash line indicates a B (blue) signal in the moving state. The characteristics in the moving state vary from LCD panel to LCD panel.

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**INTRINSIC EVIDENCE FOR DISPUTED TERM “FRAME BUFFER”**  
**(cont'd)**

[Figure 7]

26 (Graph base table)

Next brightness Previous brightness	0	10	20	30	40	50	60	70	80	90	100
0	0	28	48	63	74	83	88	93	96	98	100
10	0	10	30	45	56	65	70	75	80	90	100
20	0	10	20	35	46	55	60	70	80	90	100
30	0	10	20	30	41	50	60	70	80	90	100
40	0	10	20	30	40	50	60	70	80	90	100
50	0	10	20	30	40	50	60	70	80	90	100
60	0	10	20	30	40	50	60	70	80	90	100
70	0	10	20	30	40	50	59	70	80	90	100
80	0	10	20	30	40	45	54	65	80	90	100
90	0	10	20	25	30	35	44	55	70	90	100
100	0	2	4	7	12	17	26	38	52	72	100

FIG. 7 is a table showing a relation between brightness L1 and L2 and represents the content of the graph base table 26 stored in the ROM 23 shown in FIG. 1. The content of the graph base table 26 shown in FIG. 7 represents a relation between the previous brightness and the next brightness for the LC cell 32 having the characteristic shown in FIG. 2, by taking the effect shown in FIG. 6 into consideration. The previous brightness can be obtained from a video signal input through the ASIC21 shown in FIG. 1 and stored in the frame buffer 22. The next brightness can be obtained from the next video signal input to the ASIC 21. The graph base table 26 is constructed for each of the R, G, B color signals and the values in the table vary depending on the characteristic of the LC cell 32.

9:26-39

**INTRINSIC EVIDENCE FOR DISPUTED TERM “FRAME BUFFER”**  
**(cont'd)**

[Figure 7]

26 (Graph base table)

Next brightness Previous brightness	0	10	20	30	40	50	60	70	80	90	100
0	0	28	48	63	74	83	88	93	96	98	100
10	0	10	30	45	56	65	70	75	80	90	100
20	0	10	20	35	46	55	60	70	80	90	100
30	0	10	20	30	41	50	60	70	80	90	100
40	0	10	20	30	40	50	60	70	80	90	100
50	0	10	20	30	40	50	60	70	80	90	100
60	0	10	20	30	40	50	60	70	80	90	100
70	0	10	20	30	40	50	59	70	80	90	100
80	0	10	20	30	40	45	54	65	80	90	100
90	0	10	20	25	30	35	44	55	70	90	100
100	0	2	4	7	12	17	26	38	52	72	100

The first row of the graph base table 26 shown in FIG. 7 indicates brightness output for the next brightness when the previous brightness is 0 and match the readings of the R signal in the moving state line 50 in the graph shown in FIG. 2. For example, if the next brightness is “10”, find a value

9:40-44

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41. In this embodiment, if a difference between the previous brightness and the next brightness is greater than an offset, the next brightness is output without change. For example,

9:56-58

## **INTRINSIC EVIDENCE FOR DISPUTED TERM “FRAME BUFFER”** **(cont'd)**

On the other hand, when brightness falls from a certain halftone to another halftone, the offset is subtracted from the previous brightness. The example in FIG. 7 shows a case where the characteristic of the LC cell 32 when brightness rises (the cell is turned on) is the same as that when the brightness falls (the cell is turned off). In this example, if the previous brightness is 100 and the next brightness is 10, the output value will be  $100 - 98 = 2$ . The value “98” is equal to the value when the previous brightness is 0 and the next brightness is 90 in FIG. 7. Similarly, if the previous brightness is 100 and the next brightness is 20, then  $100 - 96 = 4$ . If the previous brightness is 90 and the next brightness is 30, then  $100 - 75 = 25$ . The value “75” is equal to the value when the previous brightness is 10 and the next brightness is 70 in FIG. 7. Similarly, if the previous brightness is 90 and the next brightness is 40, then  $100 - 70 = 30$ . The value “70” is equal to the value when the previous brightness is 10 and the next brightness is 60 in FIG. 7.

9:64-10:14

As described above, the embodiment is configured to store offsets in table form based on the relation between a brightness level in a stationary state and that in a moving state in order to obtain an ideal quantity of light. Thus, even during the movement of a display image on the LCD screen, the image can be displayed virtually the same brightness to the eye as in its stationary state, thereby inhibiting flicker on the screen.

In addition, the embodiment is configured to store the previous brightness level (gray scale value) in the frame buffer 22 and a supplementary correction is made by the ASIC 21 using the data in the graph base table 26 based on the relation between the brightness level of the next video data and the previous brightness level. Thus, whether a wire-frame model is moving or stationary is not required to be determined. Instead, the movement of the model can be determined from a difference between the determined brightness and the previous brightness. As a result, flicker can be inhibited by a simple circuit configuration.

10:49-67

**INTRINSIC EVIDENCE FOR DISPUTED TERM “SUBSTANTIALLY  
EQUAL”**

brightness is constant. The representation “substantially equal level” refers to a level which is not completely the same but can be accepted as a substantially equivalent level, and includes a level which is closer to an ideal quantity of light than no preventive measures are taken.

4:56-60

**EXHIBIT \_\_\_\_\_**  
**U.S. PATENT NO. 6,778,160**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 12**

12. A liquid crystal driving method, comprising the steps of:  
storing first brightness information for an input pixel in a frame buffer;  
applying based on second brightness information for the next input pixel and said first brightness information stored in said frame buffer an offset for making the time integration quantity of a brightness change substantially equal to an ideal light quantity which is the brightness in a stationary state to said second brightness information;  
outputting said second brightness information to which said offset is applied to a driving circuit for driving an liquid crystal cell; and  
storing said second brightness information for the input pixel in a frame buffer.

**LGD's Claim Construction**

**time integration quantity of a brightness change –**

Indefinite or quantity of light based on the actual response characteristic of the liquid cell when the liquid crystal cell is provided with the next brightness level during the next time increment in the previous brightness level before and after the next time increment.

**ideal light quantity which is the brightness in a stationary state - (see above term).**

**INTRINSIC EVIDENCE FOR DISPUTED TERM “TIME  
INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE” AND  
“IDEAL LIGHT QUANTITY WHICH IS THE BRIGHTNESS WHICH  
IS THE BRIGHTNESS IN A STATIONARY STATE”**

The term “response time” used in the industry refers to the sum of (1) time required to reverse color by applying a voltage to a liquid crystal cell and (2) time required to restore the original color by the removal of the applied voltage. The term “frame” used in the industry represents the

1:39-43

The “ideal quantity of light” herein is, to take an example, the quantity of light based on a response characteristic which provides a target brightness level at a time point at which the frame is turned on and provides a brightness level of zero at the time point at which the frame is turned off on a display device in which each pixel is driven for each frame. The brightness level can be represented as a target brightness value by a gray scale and considered as an indication of the characteristic of human visual sensation to brightness. In addition, a brightness change can be considered as a response characteristic depending on the types of liquid crystal cells (liquid crystal panels). Quantity of light is considered as a time integration quantity of a brightness change and can be expressed as brightness\_time, if the brightness is constant. The representation “substantially

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The determinant is characterized by comprising a table for storing a brightness level determined by the characteristic of a liquid crystal cell according to a relation between the previous brightness level and the next brightness level, and determining an output brightness level by modifying the next brightness level based on the brightness level read from the table. With this configuration, flicker due to changes in

4:42-67

**INTRINSIC EVIDENCE FOR DISPUTED TERM “TIME  
INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE” AND  
“IDEAL LIGHT QUANTITY WHICH IS THE BRIGHTNESS WHICH  
IS THE BRIGHTNESS IN A STATIONARY STATE” (cont'd)**

The offset set by the setting elements can be determined based on a time integration quantity, which is a change in brightness in the moving-state vide signal integrated with respect to time, and the quantity of light in stationary state, thus a difference in brightness can be preferably reduced in consideration of the human visual perception characteristic to inhibit flicker appropriately.

The moving-state video signal passed through the input consists of a plurality of color signals, the offset set by the setting elements is determined for each of the color signals, and the generator generates the output video signal for each color signal based on the offset determined for each color signal. Thus a difference in brightness between moving and stationary states can be corrected for each color signal to inhibit flicker on a color image display.

5:16-30

The moving state brightness used for storing the relation is the brightness when the particular pixel changes back to the off state one frame after it is driven from the off state to the on state during the passage of the wire-frame model over the particular pixel.

Furthermore, the brightness in the moving state which is used when the relation is stored is the quantity of light equal to the brightness change integrated with respect to time.

5:66-6:6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “TIME  
INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE” AND  
“IDEAL LIGHT QUANTITY WHICH IS THE BRIGHTNESS WHICH  
IS THE BRIGHTNESS IN A STATIONARY STATE” (cont'd)**

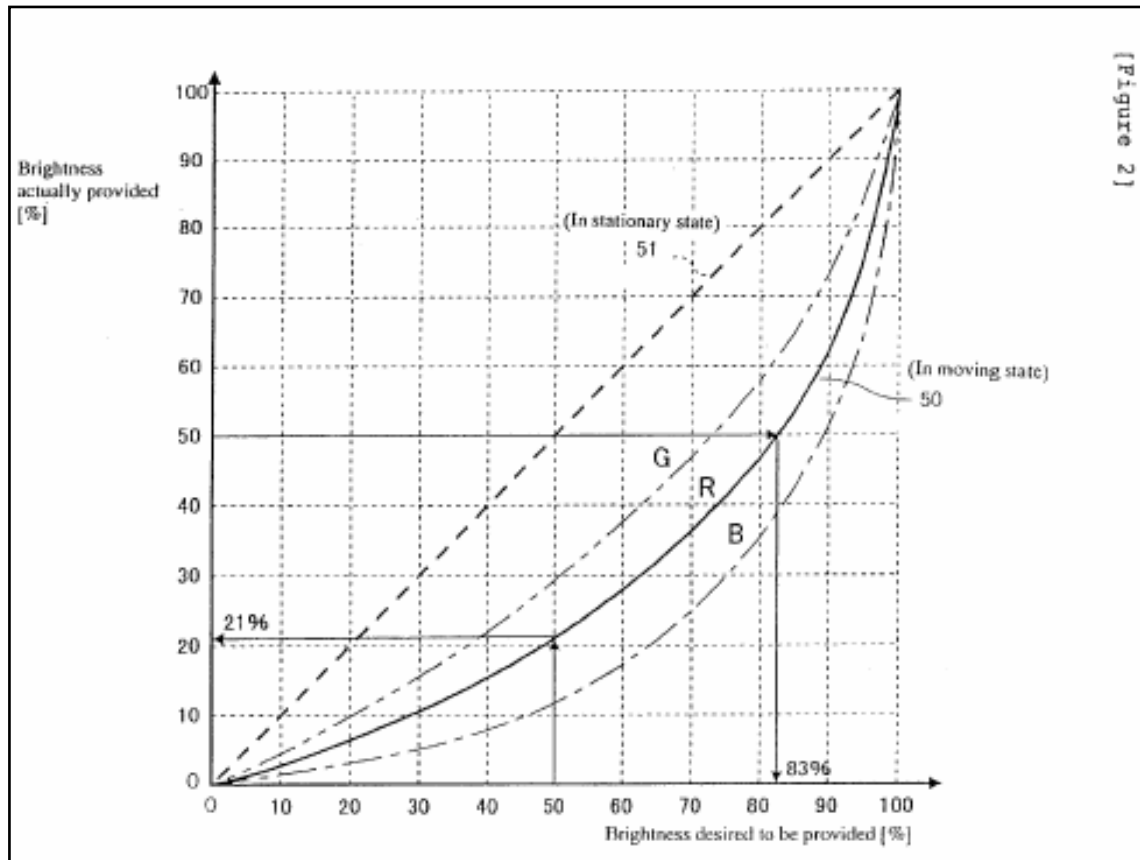


FIG. 2 is a graph showing an example of the brightness of a wire-frame model moving on the LCD panel used in this embodiment. The horizontal scale indicates brightness (%) desired to be provided and the vertical scale indicates brightness (%) actually provided in the Figure. The dashed line 51 indicates the relationship between the desired brightness and actual brightness of the model in a stationary state. The solid line 50 indicates the relationship between the desired brightness and actual brightness of the model in a moving state for an R (red) signal. The alternate long and short two dashes line indicates a G (green) signal in the moving state and the alternate long and short one dash line indicates a B (blue) signal in the moving state. The characteristics in the moving state vary from LCD panel to LCD panel.

7:31-45

**INTRINSIC EVIDENCE FOR DISPUTED TERM “TIME  
INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE” AND  
“IDEAL LIGHT QUANTITY WHICH IS THE BRIGHTNESS WHICH  
IS THE BRIGHTNESS IN A STATIONARY STATE” (cont'd)**

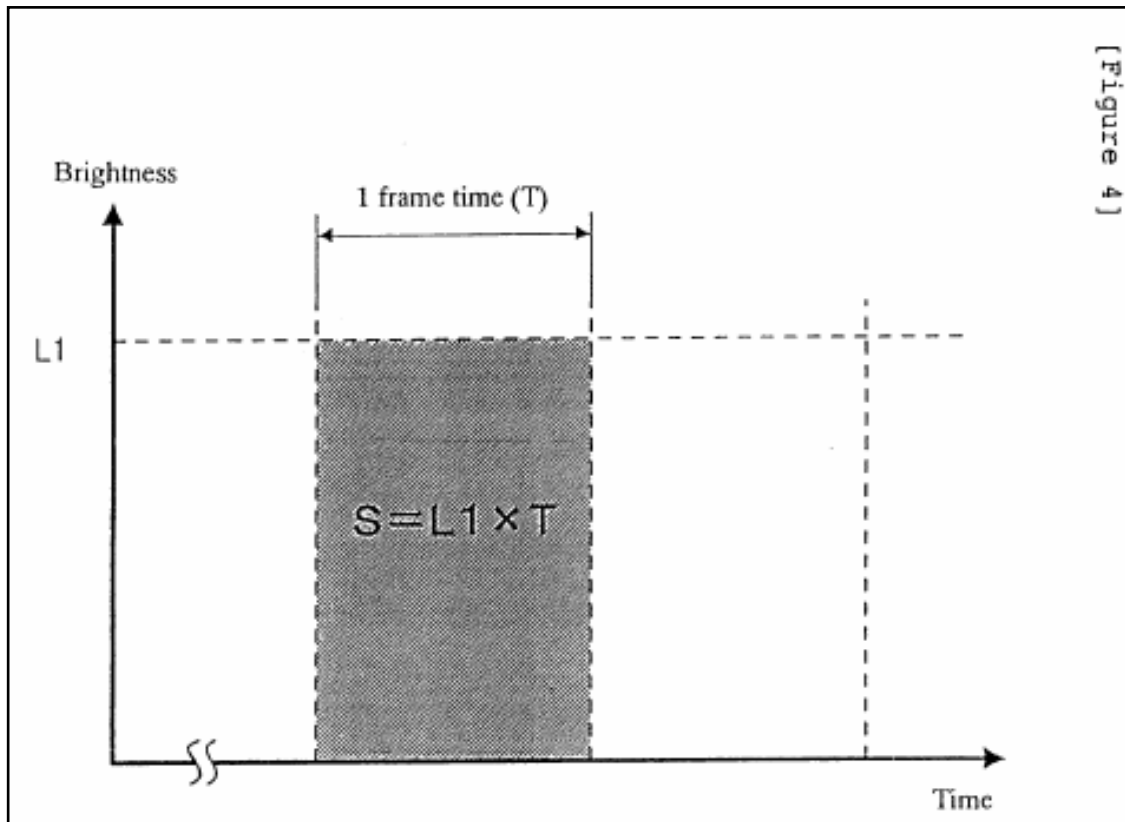


FIG. 4 shows the response characteristic of an ideal liquid crystal and indicates the state in which a particular pixel is kept lit up at a brightness of  $L1$ , that is in a stationary state. Here, the quantity of light ( $S$ ) emitted in one frame time ( $T$ ) is equal to  $L1 \times T$  (i.e. brightness  $\times$  time) as shown in the shaded area in FIG. 4.

8:35-40

**INTRINSIC EVIDENCE FOR DISPUTED TERM “TIME  
INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE” AND  
“IDEAL LIGHT QUANTITY WHICH IS THE BRIGHTNESS WHICH  
IS THE BRIGHTNESS IN A STATIONARY STATE” (cont'd)**

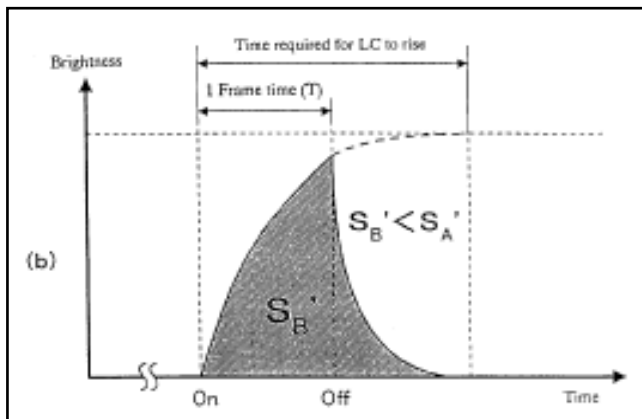
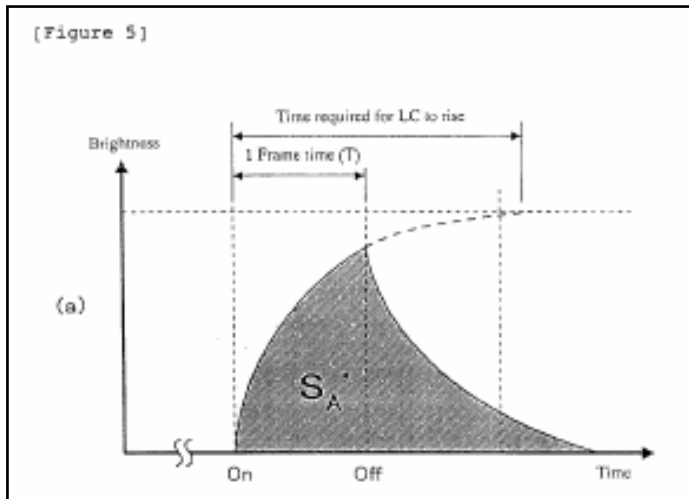
61 Model (Magnitude of flicker)	62 Response rising time	63 Response falling time	64 Light quantity ratio (to ideal LC)	65 Brightness ratio of drawing in moving state to that in stationary state
Model A (○)	20.3ms	21.6ms	1.02 : 1	1.0 : 1
Model B (×)	18.5ms	10.0ms	0.81 : 1	0.8 : 1
Model C (△)	10.0ms	4.5ms	0.85 : 1	0.9 : 1
Model D (×)	19.9ms	7.9ms	0.73 : 1	0.7 : 1
Model E (×)	43.2ms	34.3ms	0.53 : 1	0.3 : 1

[Figure 3]

FIGS. 5A and 5B show the response characteristic represented by brightness versus time when a pixel stays lit up for one frame time (On→Off) in models A, B shown in FIG. 3. Both of the rising and falling of the response of model A

8:41-44

**INTRINSIC EVIDENCE FOR DISPUTED TERM “TIME  
INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE” AND  
“IDEAL LIGHT QUANTITY WHICH IS THE BRIGHTNESS WHICH  
IS THE BRIGHTNESS IN A STATIONARY STATE” (cont'd)**



FIGS. 5A and 5B show the response characteristic represented by brightness versus time when a pixel stays lit up for one frame time (On→Off) in models A, B shown in FIG. 3. Both of the rising and falling of the response of model A

8:41-44

**INTRINSIC EVIDENCE FOR DISPUTED TERM “TIME  
INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE” AND  
“IDEAL LIGHT QUANTITY WHICH IS THE BRIGHTNESS WHICH  
IS THE BRIGHTNESS IN A STATIONARY STATE” (cont'd)**

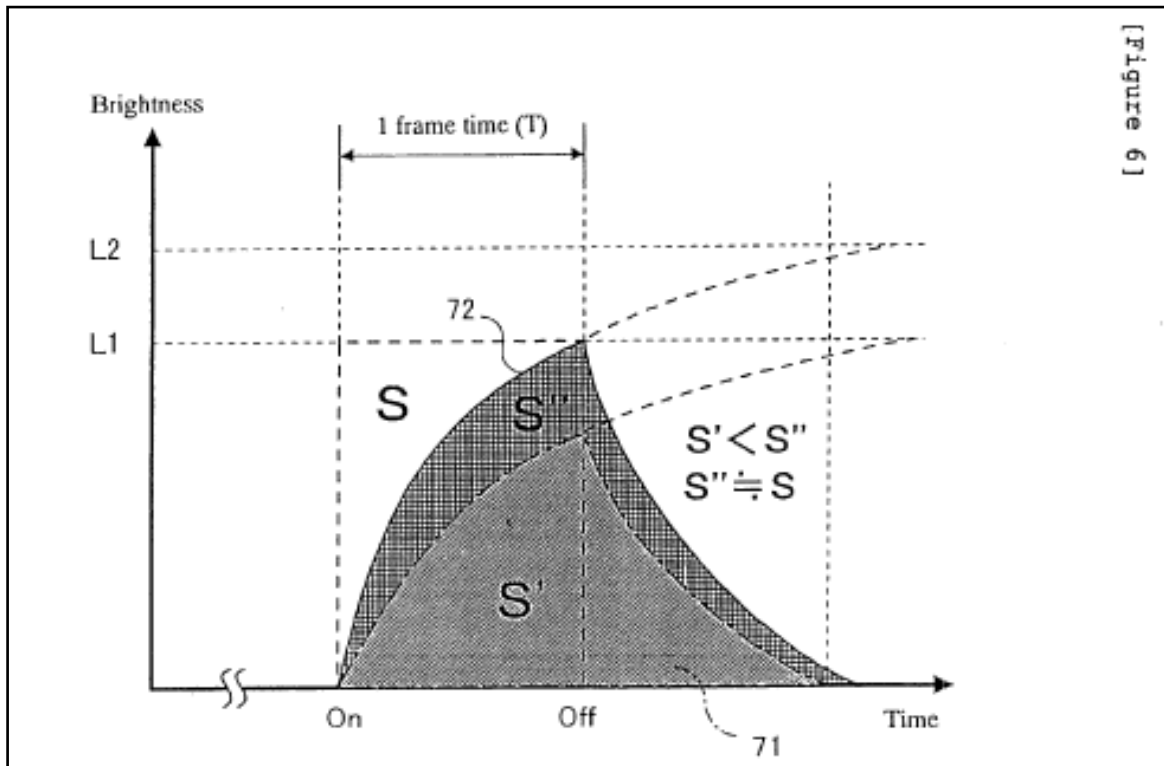


FIG. 6 shows an effect when brightness is set by taking a required offset into account. If the liquid crystal is driven trying to achieve desired brightness L1 as target, only the quantity of light (S') indicated by reference number 71 can be obtained due to the response time of the liquid crystal described above. The quantity of light (S') 71 is much smaller than the quantity of light (S) provided by the ideal response characteristic shown in FIG. 4. On the other hand, if the liquid crystal is driven with the aim of achieving brightness L2 which is larger than the desired brightness of L1, the quantity of light (S'') indicated by reference number 72 can be obtained. By overdriving the LC to brightness L2, the LC reaches L1 in a short response time and the quantity of light (S'') 72 can be obtained which is approximately the same as the quantity of light (S), which would be provided with the ideal response characteristic (S''≈S). Here, optimum brightness L2 with respect to L1 can be obtained from the data shown in FIG. 2.

9:8-25

**INTRINSIC EVIDENCE FOR DISPUTED TERM “TIME  
INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE” AND  
“IDEAL LIGHT QUANTITY WHICH IS THE BRIGHTNESS WHICH  
IS THE BRIGHTNESS IN A STATIONARY STATE” (cont'd)**

[Figure 7]

26 (Graph base table)

Next brightness Previous brightness	0	10	20	30	40	50	60	70	80	90	100
0	0	28	48	63	74	83	88	93	96	98	100
10	0	10	30	45	56	65	70	75	80	90	100
20	0	10	20	35	46	55	60	70	80	90	100
30	0	10	20	30	41	50	60	70	80	90	100
40	0	10	20	30	40	50	60	70	80	90	100
50	0	10	20	30	40	50	60	70	80	90	100
60	0	10	20	30	40	50	60	70	80	90	100
70	0	10	20	30	40	50	59	70	80	90	100
80	0	10	20	30	40	45	54	65	80	90	100
90	0	10	20	25	30	35	44	55	70	90	100
100	0	2	4	7	12	17	26	38	52	72	100

FIG. 7 is a table showing a relation between brightness L1 and L2 and represents the content of the graph base table 26 stored in the ROM 23 shown in FIG. 1. The content of the graph base table 26 shown in FIG. 7 represents a relation between the previous brightness and the next brightness for the LC cell 32 having the characteristic shown in FIG. 2, by taking the effect shown in FIG. 6 into consideration. The previous brightness can be obtained from a video signal input through the ASIC21 shown in FIG. 1 and stored in the frame buffer 22. The next brightness can be obtained from the next video signal input to the ASIC 21. The graph base table 26 is constructed for each of the R, G, B color signals and the values in the table vary depending on the characteristic of the LC cell 32.

9:26-39

**INTRINSIC EVIDENCE FOR DISPUTED TERM “TIME  
INTEGRATION QUANTITY OF A BRIGHTNESS CHANGE” AND  
“IDEAL LIGHT QUANTITY WHICH IS THE BRIGHTNESS WHICH  
IS THE BRIGHTNESS IN A STATIONARY STATE” (cont'd)**

As described above, the embodiment is configured to store offsets in table form based on the relation between a brightness level in a stationary state and that in a moving state in order to obtain an ideal quantity of light. Thus, even during the movement of a display image on the LCD screen, the image can be displayed virtually the same brightness to the eye as in its stationary state, thereby inhibiting flicker on the screen.

In addition, the embodiment is configured to store the previous brightness level (gray scale value) in the frame buffer 22 and a supplementary correction is made by the ASIC 21 using the data in the graph base table 26 based on the relation between the brightness level of the next video data and the previous brightness level. Thus, whether a wire-frame model is moving or stationary is not required to be determined. Instead, the movement of the model can be determined from a difference between the determined brightness and the previous brightness. As a result, flicker can be inhibited by a simple circuit configuration.

10:49-67

# **EXHIBIT L-25**

**EX. L-25**  
**CMO US PATENT NO. 7,090,506**

**INDEX OF DISPUTED TERMS**

<b><u>CLAIM TERMS</u></b>	<b><u>PAGE</u></b>
a first flexible printed circuit board, electrically connecting the display module and the system.....	9
display module .....	9
a second flexible printed circuit board, electrically connecting the display module and the first flexible printed circuit board.....	1
the first and second flexible printed circuit boards are joined by hot bar soldering .....	1
the first and second flexible printed circuit boards are joined by anisotropic conductive film (ACF) bonding.....	1

**EXHIBIT L-25**  
**U.S. PATENT NO. 7,090,506**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 1**

1. A signal transmission device, connecting a display module and a system, comprising: a first flexible printed circuit board, electrically connecting the display module and the system and a second flexible printed circuit board, electrically connecting the display module and the first flexible printed circuit board, wherein the first and second flexible printed circuit boards are joined by hot bar soldering.

**ASSERTED CLAIM 9**

9. A signal transmission device, connecting an display module and a system, comprising: a first flexible printed circuit board, electrically connecting the display module and the system; and a second flexible printed circuit board, electrically connecting the display module and the first flexible printed circuit board, wherein the first and second flexible printed circuit boards are joined by anisotropic conductive film (ACF) bonding.

**LGD's Claim Construction**

**a second flexible printed circuit board, electrically connecting the display module and the first flexible printed circuit board<sup>1</sup>** – a second flexible film with conductive patterns printed on its surface that electrically connects the display module and the first flexible film

**the first and second flexible printed circuit boards are joined by hot bar soldering** – both flexible printed circuit boards are connected to each other by a soldering process where the circuit boards are heated with a bar to melt the solder at multiple points simultaneously along each circuit board while pressure is applied to the connection

**the first and second flexible printed circuit boards are joined by anisotropic conductive film (ACF) bonding** – both flexible printed circuit boards are connected to each other by a process where a material that is conductive in one direction is pressed between the two circuit boards

<sup>1</sup> Disputed Term “a second flexible printed circuit board, electrically connecting the display module and the first flexible printed circuit board” also appears in asserted claim 17 in the same context.

**INTRINSIC EVIDENCE FOR DISPUTED TERM “A SECOND FLEXIBLE PRINTED CIRCUIT BOARD, ELECTRICALLY CONNECTING THE DISPLAY MODULE AND THE FIRST FLEXIBLE PRINTED CIRCUIT BOARD”:**

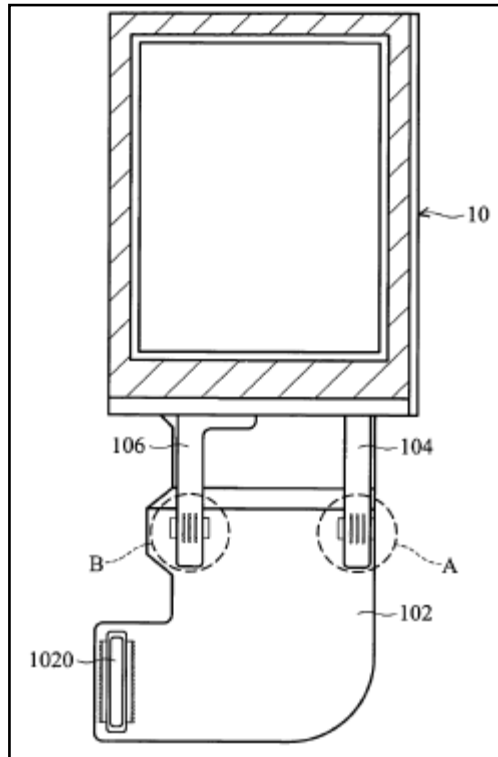


Fig. 2

Accordingly, an object of the present invention is to provide a signal transmission device. The signal transmission device comprises a first and a second flexible printed circuit boards, connecting an LCD module and a system. The first flexible printed circuit board electrically connects the LCD module and the system. The second flexible printed circuit board electrically connects the LCD module and the first flexible printed circuit board, wherein the first and second flexible printed circuit boards are joined by hot bar soldering or anisotropic conductive film (ACF) bonding.

1:34

**INTRINSIC EVIDENCE FOR DISPUTED TERM “A SECOND FLEXIBLE PRINTED CIRCUIT BOARD, ELECTRICALLY CONNECTING THE DISPLAY MODULE AND THE FIRST FLEXIBLE PRINTED CIRCUIT BOARD” (cont’d):**

cally, the second and third flexible printed circuit boards 104 and 106 individually communicate a touch panel signal and a light source signal between the touchscreen display module 10 and the system through the first flexible printed circuit board 102.

2:1-5

and light source signals from the touchscreen display module 10 can be collected in the first flexible printed circuit board 102 and communicated to the system via the connector 1020. That is, the display panel, touch panel and light source signals are integrated in the first flexible printed circuit board 102 and communicated to the system through a single connector 1020.

2:9-15

In FIG. 3a, the first flexible printed circuit board 102 defines a connection area 1021 with soldering pads S disposed thereon. Moreover, several alignment marks M are correspondingly disposed around the periphery of the connection area 1021 and the second flexible printed circuit board 104. Accurate positioning and connection is accomplished by aligning the alignment marks M on the first and second flexible printed circuit boards 102 and 104 during assembly. Similarly, the alignment marks M can also be applied to the third flexible printed circuit board 106 for accurate connection of the first flexible printed circuit board 102 as shown by the area B in FIG. 2.

2:26-37

In FIG. 4a, the first and second flexible printed circuit boards 102 and 104 are aligned via alignment holes H2. Accurate positioning and connection is accomplished by aligning the alignment holes H2 of the first and second flexible printed circuit board 102 and 104. Similarly, the alignment hole H2 can also be applied to the third flexible printed circuit board 106 for accurate connection of the first flexible printed circuit board 102 as shown by the area B in FIG. 2.

2:49-57

**INTRINSIC EVIDENCE FOR DISPUTED TERM “A SECOND FLEXIBLE PRINTED CIRCUIT BOARD, ELECTRICALLY CONNECTING THE DISPLAY MODULE AND THE FIRST FLEXIBLE PRINTED CIRCUIT BOARD” (cont’d):**

In summary, the present invention provides a signal transmission device capable of collecting touch panel and light source signals together in the first flexible printed circuit board 102. Thus, touch panel, light source and display panel signals between the touchscreen display module 10 and the system can be communicated through a single connector 1020 of the flexible printed circuit board 102. As mentioned, each flexible printed circuit board can be joined by hot bar soldering or anisotropic conductive film (ACF) bonding. Moreover, the alignment marks M or openings H2

2:58-67

electrically connected by a foldable flat cable FC. See col. 21, lines 51-54 and FIG. 31 of Shibata. In Shibata, the drive circuit substrates PCB1 and PCB2 are flexibly connected by the foldable flat cable FC, namely, they are not directly “joined by hot bar soldering” or “joined by anisotropic conductive film (ACF) bonding”, as recited in independent claims 1 and 9 of the present application.

In addition, Applicant notes that the flat cable FC in Shibata’s patent is neither a flexible printed circuit board nor a soldering material/anisotropic conductive film (ACF), as recited in claims 1 and 9. Moreover, the drive circuit substrates PCB1 and PCB2 in Shibata’s patent are not “flexible printed circuit boards”, and neither of them have “alignment mark” as recited in claim 17 of the present application. For at least this reason, independent claims 1, 9, and 17 patently define over Shibata.

Amendment and Response  
to Office Action at 10

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE FIRST AND SECOND FLEXIBLE PRINTED CIRCUIT BOARDS ARE JOINED BY HOT BAR SOLDERING”:**

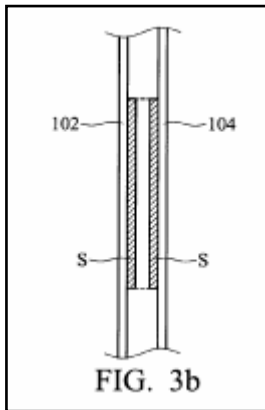


Fig. 3b

As shown in FIG. 3b, the first and second flexible printed circuit boards 102 and 104 are joined by hot bar soldering via corresponding soldering pads S. Thus, the touch panel signal of the second flexible printed circuit board 104 is collected in the first flexible printed circuit board 102.

2:16-20

circuit board 102. Thus, touch panel, light source and display panel signals between the touchscreen display module 10 and the system can be communicated through a single connector 1020 of the flexible printed circuit board 102. As mentioned, each flexible printed circuit board can be joined by hot bar soldering or anisotropic conductive film (ACF) bonding. Moreover, the alignment marks M or openings H2

2:61-67

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE FIRST AND SECOND FLEXIBLE PRINTED CIRCUIT BOARDS ARE JOINED BY HOT BAR SOLDERING” (cont’d):**

electrically connected by a foldable flat cable FC. See col. 21, lines 51-54 and FIG. 31 of Shibata. In Shibata, the drive circuit substrates PCB1 and PCB2 are flexibly connected by the foldable flat cable FC, namely, they are not directly “joined by hot bar soldering” or “joined by anisotropic conductive film (ACF) bonding”, as recited in independent claims 1 and 9 of the present application.

In addition, Applicant notes that the flat cable FC in Shibata’s patent is neither a flexible printed circuit board nor a soldering material/anisotropic conductive film (ACF), as recited in claims 1 and 9. Moreover, the drive circuit substrates PCB1 and PCB2 in Shibata’s patent are not “flexible printed circuit boards”, and neither of them have “alignment mark” as recited in claim 17 of the present application. For at least this reason, independent claims 1, 9, and 17 patently define over Shibata.

Amendment and Response  
to Office Action at 10

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE FIRST AND SECOND FLEXIBLE PRINTED CIRCUIT BOARDS ARE JOINED BY ANISOTROPIC CONDUCTIVE FILM (ACF) BONDING”**

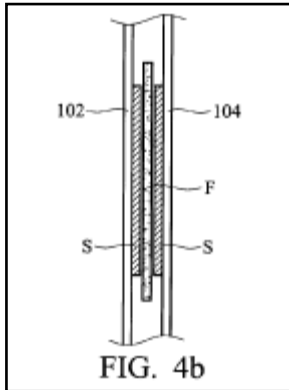


Fig. 4b

**Second Embodiment**

Referring to FIGS. 4a and 4b, the first and second flexible printed circuit boards 102 and 104 are joined by anisotropic conductive film (ACF) bonding via corresponding soldering pads S. As shown in FIG. 4b, an anisotropic conductive film F is electrically bonded between the soldering pads S of the first and second flexible printed circuit boards 102 and 104.

2:39-45

circuit board 102. Thus, touch panel, light source and display panel signals between the touchscreen display module 10 and the system can be communicated through a single connector 1020 of the flexible printed circuit board 102. As mentioned, each flexible printed circuit board can be joined by hot bar soldering or anisotropic conductive film (ACF) bonding. Moreover, the alignment marks M or openings H2

2:61-67

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE FIRST AND SECOND FLEXIBLE PRINTED CIRCUIT BOARDS ARE JOINED BY ANISOTROPIC CONDUCTIVE FILM (ACF) BONDING” (cont’d):**

electrically connected by a foldable flat cable FC. See col. 21, lines 51-54 and FIG. 31 of Shibata. In Shibata, the drive circuit substrates PCB1 and PCB2 are flexibly connected by the foldable flat cable FC, namely, they are not directly “joined by hot bar soldering” or “joined by anisotropic conductive film (ACF) bonding”, as recited in independent claims 1 and 9 of the present application.

In addition, Applicant notes that the flat cable FC in Shibata’s patent is neither a flexible printed circuit board nor a soldering material/anisotropic conductive film (ACF), as recited in claims 1 and 9. Moreover, the drive circuit substrates PCB1 and PCB2 in Shibata’s patent are not “flexible printed circuit boards”, and neither of them have “alignment mark” as recited in claim 17 of the present application. For at least this reason, independent claims 1, 9, and 17 patently define over Shibata.

Amendment and Response  
to Office Action at 10

**EXHIBIT 24**  
**U.S. PATENT NO. 7,090,506**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 1**

1. A signal transmission device, connecting a display module and a system, comprising: a first flexible printed circuit board, electrically connecting the display module and the system and a second flexible printed circuit board, electrically connecting the display module and the first flexible printed circuit board, wherein the first and second flexible printed circuit boards are joined by hot bar soldering.

**LGD's Claim Construction**

**a first flexible printed circuit board, electrically connecting the display module and the system<sup>1</sup>** – a first flexible film with conductive patterns printed on its surface that electrically connects the display module and the system

**display module<sup>2</sup>** – an assembly that includes an LCD panel, a touch panel and a light source

<sup>1</sup> Disputed Term “a first flexible printed circuit board, electrically connecting the display module and the system” also appears in asserted claims 9, and 17 in the same context.

<sup>2</sup> Disputed Term “display module” also appears in asserted claims 8, 9, 16, 17, and 23 in the same context.

**INTRINSIC EVIDENCE FOR DISPUTED TERM “A FIRST FLEXIBLE PRINTED CIRCUIT BOARD, ELECTRICALLY CONNECTING THE DISPLAY MODULE AND THE SYSTEM”:**

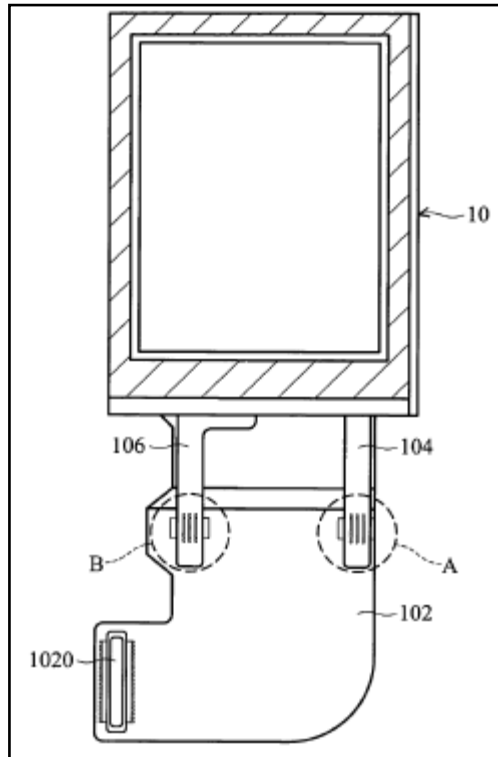


Fig. 2

Accordingly, an object of the present invention is to provide a signal transmission device. The signal transmission device comprises a first and a second flexible printed circuit boards, connecting an LCD module and a system. The first flexible printed circuit board electrically connects the LCD module and the system. The second flexible printed circuit board electrically connects the LCD module and the first flexible printed circuit board, wherein the first and second flexible printed circuit boards are joined by hot bar soldering or anisotropic conductive film (ACF) bonding.

1:34

**INTRINSIC EVIDENCE FOR DISPUTED TERM “A FIRST FLEXIBLE PRINTED CIRCUIT BOARD, ELECTRICALLY CONNECTING THE DISPLAY MODULE AND THE SYSTEM” (cont’d):**

cally, the second and third flexible printed circuit boards 104 and 106 individually communicate a touch panel signal and a light source signal between the touchscreen display module 10 and the system through the first flexible printed circuit board 102.

2:1-5

and light source signals from the touchscreen display module 10 can be collected in the first flexible printed circuit board 102 and communicated to the system via the connector 1020. That is, the display panel, touch panel and light source signals are integrated in the first flexible printed circuit board 102 and communicated to the system through a single connector 1020.

2:9-15

In FIG. 3a, the first flexible printed circuit board 102 defines a connection area 1021 with soldering pads S disposed thereon. Moreover, several alignment marks M are correspondingly disposed around the periphery of the connection area 1021 and the second flexible printed circuit board 104. Accurate positioning and connection is accomplished by aligning the alignment marks M on the first and second flexible printed circuit boards 102 and 104 during assembly. Similarly, the alignment marks M can also be applied to the third flexible printed circuit board 106 for accurate connection of the first flexible printed circuit board 102 as shown by the area B in FIG. 2.

2:26-37

In FIG. 4a, the first and second flexible printed circuit boards 102 and 104 are aligned via alignment holes H2. Accurate positioning and connection is accomplished by aligning the alignment holes H2 of the first and second flexible printed circuit board 102 and 104. Similarly, the alignment hole H2 can also be applied to the third flexible printed circuit board 106 for accurate connection of the first flexible printed circuit board 102 as shown by the area B in FIG. 2.

2:49-57

**INTRINSIC EVIDENCE FOR DISPUTED TERM “A FIRST FLEXIBLE PRINTED CIRCUIT BOARD, ELECTRICALLY CONNECTING THE DISPLAY MODULE AND THE SYSTEM” (cont’d):**

In summary, the present invention provides a signal transmission device capable of collecting touch panel and light source signals together in the first flexible printed circuit board 102. Thus, touch panel, light source and display panel signals between the touchscreen display module 10 and the system can be communicated through a single connector 1020 of the flexible printed circuit board 102. As mentioned, each flexible printed circuit board can be joined by hot bar soldering or anisotropic conductive film (ACF) bonding. Moreover, the alignment marks M or openings H2

2:58-67

electrically connected by a foldable flat cable FC. See col. 21, lines 51-54 and FIG. 31 of Shibata. In Shibata, the drive circuit substrates PCB1 and PCB2 are flexibly connected by the foldable flat cable FC, namely, they are not directly “joined by hot bar soldering” or “joined by anisotropic conductive film (ACF) bonding”, as recited in independent claims 1 and 9 of the present application.

In addition, Applicant notes that the flat cable FC in Shibata’s patent is neither a flexible printed circuit board nor a soldering material/anisotropic conductive film (ACF), as recited in claims 1 and 9. Moreover, the drive circuit substrates PCB1 and PCB2 in Shibata’s patent are not “flexible printed circuit boards”, and neither of them have “alignment mark” as recited in claim 17 of the present application. For at least this reason, independent claims 1, 9, and 17 patently define over Shibata.

Amendment and Response  
to Office Action at 10

## **INTRINSIC EVIDENCE FOR DISPUTED TERM “DISPLAY MODULE”:**

### 2. Description of the Related Art

Generally, a conventional touchscreen LCD module comprises an LCD panel, a touch panel and a light source. Referring to FIG. 1, the conventional touchscreen LCD module 10 communicates LCD panel, touch panel and light source signals to a system (not shown) through flexible printed circuit boards 102, 104 and 106. To receive the three types of signals, however, three connecting ports corresponding to the flexible printed circuit boards 102, 104 and 106 are required in the system, thus, it incurring additional fabrication cost and space.

1:11-21

### First Embodiment

Referring to FIG. 2, the signal transmission device of the present invention comprises first, second and third flexible printed circuit boards 102, 104 and 106 electrically connecting the touchscreen display module 10 and a system (not shown). The first flexible printed circuit board 102 communicates display panel signal between the touchscreen display module 10 and the system via the connector 1020. Specifi-

1:60-67

cally, the second and third flexible printed circuit boards 104 and 106 individually communicate a touch panel signal and a light source signal between the touchscreen display module 10 and the system through the first flexible printed circuit board 102.

2:1-5

As the areas A and B in FIG. 2, the second and third flexible printed circuit boards 104 and 106 are joined to the first flexible printed circuit board 102, thereby touch panel and light source signals from the touchscreen display module 10 can be collected in the first flexible printed circuit board 102 and communicated to the system via the connector 1020. That is, the display panel, touch panel and light

2:6-12

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DISPLAY  
MODULE” (cont’d):**

can be applied to each flexible printed circuit board for accurate positioning and connection. As only a single connector is required to communicate the multiple signals between the touchscreen display module 10 and the system, fabrication cost and space required for assembly can be reduced.

3:1-6

# **EXHIBIT L-26**

**EX. L-26**  
**CMO US PATENT NO. 6,734,926**

**INDEX OF DISPUTED TERMS**

<b><u>CLAIM TERMS</u></b>	<b><u>PAGE</u></b>
display apparatus.....	10
upper frame .....	10
an array of light tubes disposed behind the display panel .....	10
being separated from the side portion by a gap .....	1
a circuit board installed within the gap for controlling operations of the display apparatus.....	17
being separated from the side portion of the supporting plate by a gap .....	28
a circuit board installed on the side portion of the reflecting plate for controlling operations of the display apparatus .....	1
a circuit board installed on the side portion of the supporting plate for controlling operations of the display apparatus .....	17
integrated supporting unit .....	28

**EXHIBIT L-26**  
**U.S. PATENT NO. 6,734,926**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 1**

1. A display apparatus comprising:  
an upper frame;  
a display panel installed inside the upper frame for displaying images;  
an array of light tubes disposed behind the display panel for generating light;  
a reflecting plate disposed behind the array of light tubes for reflecting light generated by the array of light tubes, the reflecting plate having a main portion and at least one side portion being tilted with respect to the main portion;  
a supporting frame installed on the reflecting plate for supporting the display panel, the supporting frame comprising a plurality of sub-frames, at least one of the sub-frames being tilted with respect to the main portion of the reflecting plate and **being separated from the side portion by a gap**; and  
a circuit board installed within the gap for controlling operations of the display apparatus.

**LGD's Claim Construction**

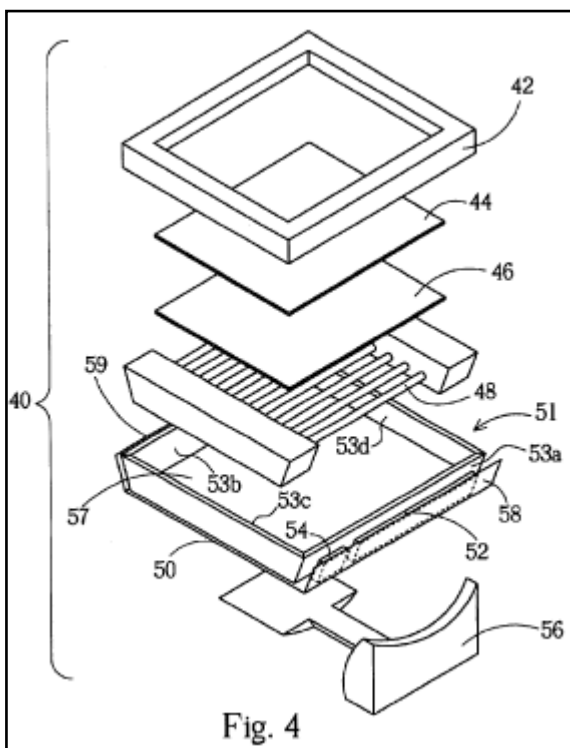
**being separated from the side portion by a gap** – positioned to form a space bounded by a sub-frame and a side portion

**ASSERTED CLAIM 15**

15. A display apparatus comprising:  
an upper frame;  
a display panel installed inside the upper frame for displaying images;  
an array of light tubes disposed behind the display panel for generating light;  
a reflecting plate disposed behind the array of light tubes for reflecting light generated by the array of light tubes, the reflecting plate having a main portion and at least one side portion being tilted with respect to the main portion;  
a supporting frame installed on the reflecting plate for supporting the display panel; and  
**a circuit board installed on the side portion of the reflecting plate for controlling operations of the display apparatus.**

**a circuit board installed on the side portion of the reflecting plate for controlling operations of the display apparatus** – a control circuit board is mounted to the side of the reflecting plate and no control circuit board is located on the back of the reflecting plate

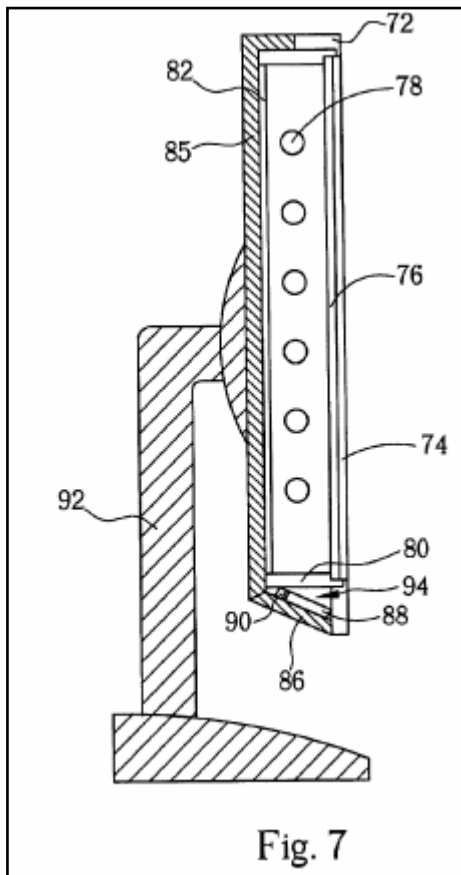
**INTRINSIC EVIDENCE FOR DISPUTED TERM “BEING SEPARATED FROM THE SIDE PORTION BY A GAP”:**



into digital signals. The circuit board 52 can be a rigid circuit board or a printed circuit board. The circuit board 52 could also include an electromagnetic interference shield to shield the electromagnetic radiation generated by the circuit board 52. In this embodiment, the circuit board 52 of the direct-type LCD apparatus 40 is installed onto either the side portion 58 of the reflecting plate 57 or the sub-frame 53a of the supporting frame 51 by making use of the gap 66.

4:33-39

**INTRINSIC EVIDENCE FOR DISPUTED TERM “BEING SEPARATED FROM THE SIDE PORTION BY A GAP” (cont’d):**



The supporting plate 84 has a main portion 85 and at least one side portion 86. The reflecting sheet 82 is positioned onto the main portion 85. As shown in FIG. 6, the side portion 86 is tilted with respect to the main portion 85. A gap 94 exists between the side portion 86 and the supporting frame 80. The LCD apparatus further comprises a circuit board 88 for controlling the display panel 74, and a connector 90 for receiving display data sent by an external display controller such as a VGA card of a computer system. The circuit board 88 is installed within the gap 94.

5:12-21

**INTRINSIC EVIDENCE FOR DISPUTED TERM “BEING SEPARATED FROM THE SIDE PORTION BY A GAP”**

**(cont’d):**

The present invention is not limited by the second preferred embodiment described. For example, one end of the stand assembly 92 can be installed on the bottom side of the upper frame 72 to support the entire LCD apparatus 40. Additionally, the gap 94 can exist in any side of the LCD apparatus 40 through appropriate arrangement of the side portion 86. For example, when the side portion 86 is positioned on the top of the main portion 85, the gap 94 will exist on the top of the LCD apparatus 40. In addition, the

5:37-45

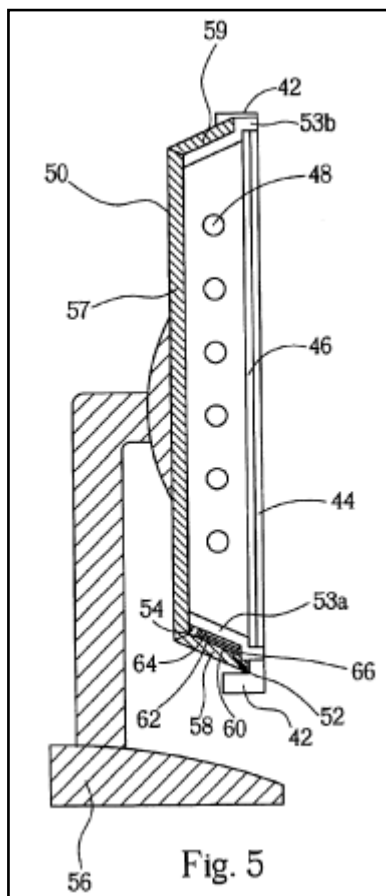
to the main portion 117. The main portion 117 of the reflecting plate 110 along with the supporting frame 111 constitute a reflecting surface, which reflects the light generated by the light tube array 108. It is noteworthy that a gap 126 exists between the side portion 118 and the lower frame 115. Then, the circuit board 112 is installed within the gap 126. The circuit board 112 comprises at least an X-board 120 to drive pixels in the same row for displaying corresponding

6:3-10

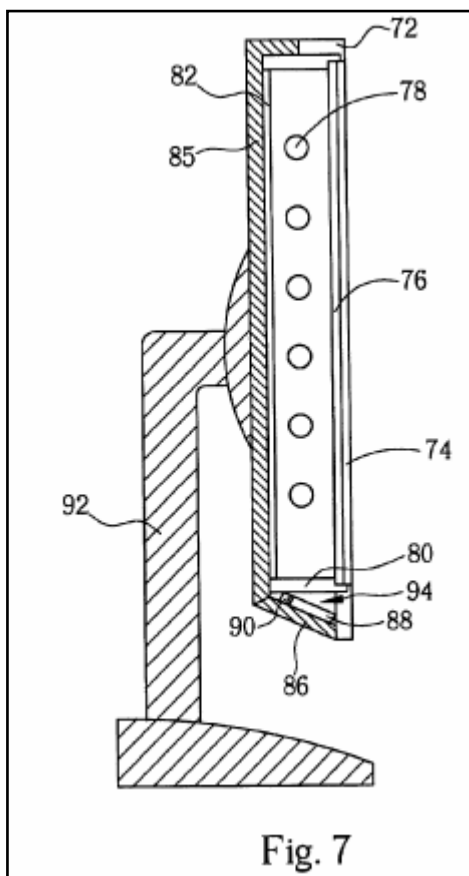
Compared with the prior art direct-type LCD apparatus, the present invention utilizes the space between the side portions of the reflecting plate and the supporting frame (first preferred embodiment), the side portions of the supporting plate and the supporting frame (second preferred embodiment), the side portion of the supporting plate and the lower frame (third and fifth embodiments), or the side portion of the reflecting plate and the lower frame (fourth and sixth embodiments) to house the circuit board and related elements. As a result, the thickness of the direct-type LCD apparatus is reduced without the circuit board and related elements positioned at the back of the LCD apparatus. Therefore, it makes the LCD apparatus more convenient to use. Furthermore, the present invention utilizes the main

8:4-17

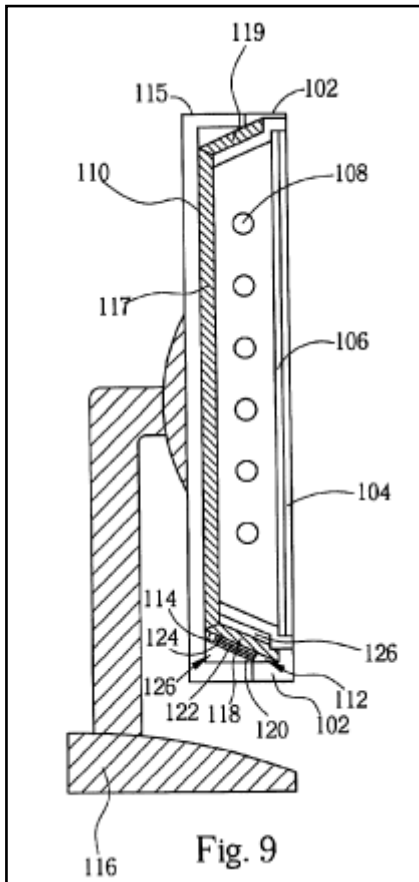
**INTRINSIC EVIDENCE FOR DISPUTED TERM “A CIRCUIT BOARD INSTALLED ON THE SIDE PORTION OF THE REFLECTING PLATE FOR CONTROLLING OPERATIONS OF THE DISPLAY APPARATUS”:**



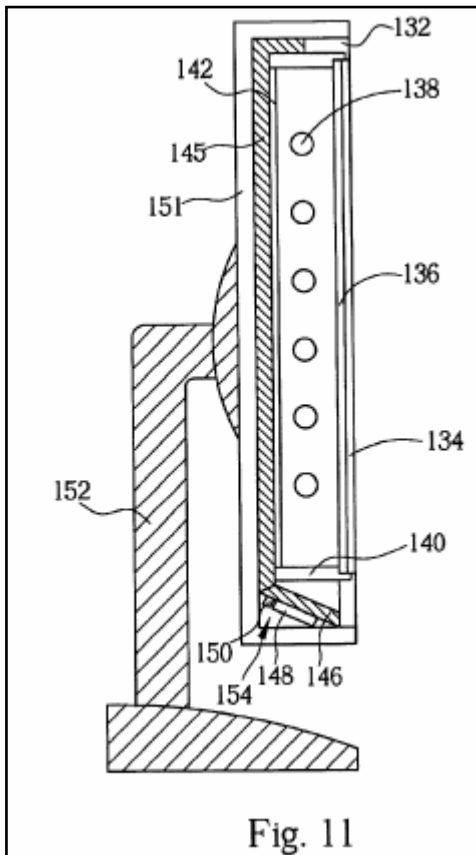
**INTRINSIC EVIDENCE FOR DISPUTED TERM “A CIRCUIT BOARD INSTALLED ON THE SIDE PORTION OF THE REFLECTING PLATE FOR CONTROLLING OPERATIONS OF THE DISPLAY APPARATUS” (cont’d):**



**INTRINSIC EVIDENCE FOR DISPUTED TERM “A CIRCUIT BOARD INSTALLED ON THE SIDE PORTION OF THE REFLECTING PLATE FOR CONTROLLING OPERATIONS OF THE DISPLAY APPARATUS” (cont’d):**



**INTRINSIC EVIDENCE FOR DISPUTED TERM “A CIRCUIT BOARD INSTALLED ON THE SIDE PORTION OF THE REFLECTING PLATE FOR CONTROLLING OPERATIONS OF THE DISPLAY APPARATUS” (cont’d):**



1. Field of the Invention

The present invention relates to a Liquid Crystal Display (LCD) apparatus with a reduced thickness, and more specifically, to an LCD apparatus with no control circuit board installed onto the back of the back light unit.

1:7-11

**INTRINSIC EVIDENCE FOR DISPUTED TERM “A CIRCUIT BOARD INSTALLED ON THE SIDE PORTION OF THE REFLECTING PLATE FOR CONTROLLING OPERATIONS OF THE DISPLAY APPARATUS” (cont’d):**

It is an advantage of the claimed invention, in which no circuit board is installed on the back side of the direct-type back light unit, such that the display apparatus has a simplified frame structure and is therefore slimmer and more convenient to use. It is a further advantage of the claimed invention that production cost of the display apparatus is greatly reduced.

3:18-24

110 and protected by the lower frame 115. The lower frame 115 could be any shape and size to provide protection and/or shield for the circuit board 112 and is not limited to a lower housing case to enclose the whole reflecting plate 110 and supporting frame 111. A stand assembly 116 could be further provided and coupled to either the reflecting plate 117 or the lower frame 115 to support the LCD apparatus 40. Without any circuit board 112 is installed on the back of the reflecting plate 110, the thickness of the LCD apparatus 40 is reduced.

6:19-27

supporting plate 144 and supporting frame 140. A stand assembly 152 could be further provided and coupled to either the supporting plate 144 or the lower frame 151 to support the LCD apparatus 40. Without any circuit board 148 installed on the back side of the reflecting plate 144, the thickness of the LCD apparatus 40 is reduced.

6:59-64

the lower frame (third and fifth embodiments), or the side portion of the reflecting plate and the lower frame (fourth and sixth embodiments) to house the circuit board and related elements. As a result, the thickness of the direct-type LCD apparatus is reduced without the circuit board and related elements positioned at the back of the LCD apparatus. Therefore, it makes the LCD apparatus more convenient to use. Furthermore, the present invention utilizes the main portion of the reflecting plate (first preferred embodiment) or

8:10-18

**EXHIBIT L-25**  
**U.S. PATENT NO. 6,734,926**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 1**

1. A display apparatus comprising:  
an upper frame;  
a display panel installed inside the upper frame for displaying images;  
an array of light tubes disposed behind the display panel for generating light;  
a reflecting plate disposed behind the array of light tubes for reflecting light generated by the array of light tubes, the reflecting plate having a main portion and at least one side portion being tilted with respect to the main portion;  
a supporting frame installed on the reflecting plate for supporting the display panel, the supporting frame comprising a plurality of sub-frames, at least one of the sub-frames being tilted with respect to the main portion of the reflecting plate and being separated from the side portion by a gap; and  
a circuit board installed within the gap for controlling operations of the display apparatus.

**LGD's Claim Construction**

**display apparatus<sup>1</sup>** – a display product, such as a monitor or television

**upper frame<sup>2</sup>** – the outermost front cover for the display product

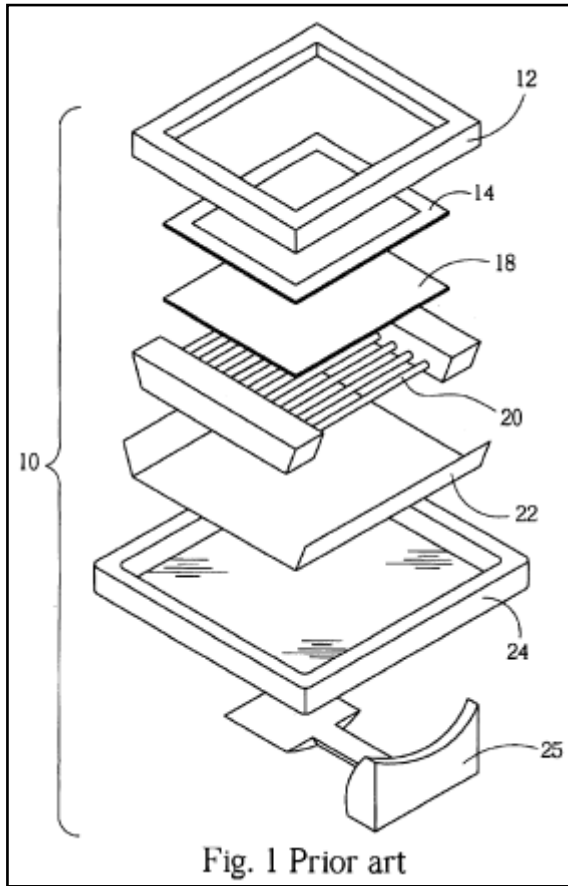
**an array of light tubes disposed behind the display panel<sup>3</sup>** – multiple fluorescent lamps arranged along the back of the direct type backlight unit

<sup>1</sup> Disputed Term “display apparatus” also appears in asserted claims 2-36, 41, and 42 in the same context.

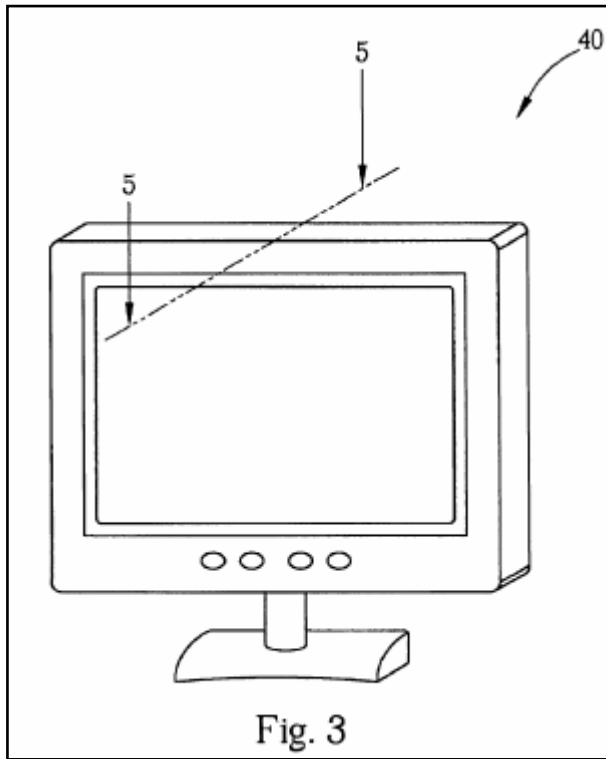
<sup>2</sup> Disputed Term “upper frame” also appears in asserted claims 4, 8, 11, 15, 18, 22, 25, 29, 32, 36, and 39 in the same context.

<sup>3</sup> Disputed Term “an array of light tubes disposed behind the display panel” also appears in asserted claims 8, 15, 22, 29, and 36 in the same context

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DISPLAY APPARATUS”:**



**INTRINSIC EVIDENCE FOR DISPUTED TERM “DISPLAY APPARATUS” (cont’d):**

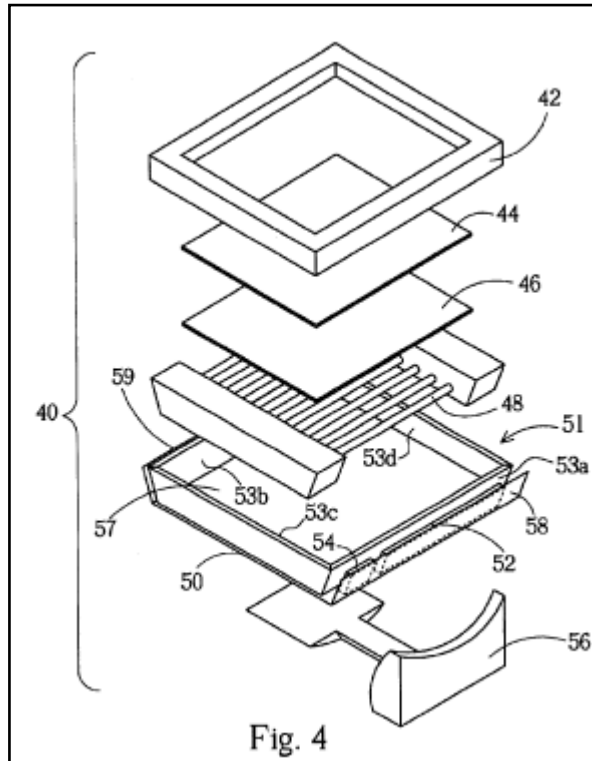


Among various types of LCD apparatuses, direct-type LCD apparatuses, such as direct-type LCD monitors and televisions, are broadly used as large-size display.

Please refer to FIG. 1, which illustrates the constituent components of a well-known direct-type LCD monitor 10. The LCD monitor 10 comprises an upper frame 12 and a

1:36-41

**INTRINSIC EVIDENCE FOR DISPUTED TERM “UPPER FRAME”:**



Please refer to FIG. 1, which illustrates the constituent components of a well-known direct-type LCD monitor 10. The LCD monitor 10 comprises an upper frame 12 and a lower frame 24 which hold in place the internal components of the LCD monitor 10. The internal components comprise an LCD panel 14 for displaying images, a diffuser 18 to equalize light, a light tube array 20 to generate white light, and a reflecting plate 22 to reflect the light generated by the

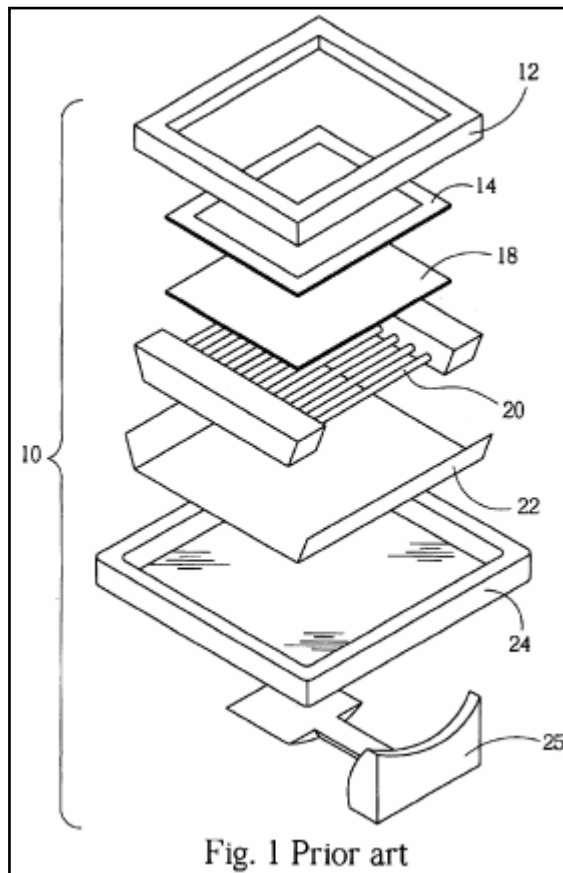
1:40-47

**INTRINSIC EVIDENCE FOR DISPUTED TERM “UPPER FRAME” (cont’d):**

The first preferred embodiment of the claimed invention includes a display apparatus, which comprises an upper frame, a display panel installed in the upper frame to display images, a light tube array behind the display panel to generate light, a reflecting plate disposed behind the light tube array to reflect the light generated by the light tube array, and a supporting frame installed on the reflecting plate to support the display panel. The reflecting plate comprises

2:17-24

**INTRINSIC EVIDENCE FOR DISPUTED TERM “AN ARRAY OF LIGHT TUBES DISPOSED BEHIND THE DISPLAY PANEL”:**



The LCD monitor 10 comprises an upper frame 12 and a lower frame 24 which hold in place the internal components of the LCD monitor 10. The internal components comprise an LCD panel 14 for displaying images, a diffuser 18 to equalize light, a light tube array 20 to generate white light, and a reflecting plate 22 to reflect the light generated by the light tube array 20. A stand assembly 25 is also included to support the LCD monitor 10. When the light emitted by the

1:42-49

**INTRINSIC EVIDENCE FOR DISPUTED TERM “AN ARRAY  
OF LIGHT TUBES DISPOSED BEHIND THE DISPLAY  
PANEL” (cont’d):**

In those direct-type LCD apparatuses, a light tube array 20 illuminates the display panel 14 with no bulky light guide plate and hence the weight of the apparatuses is reduced. However, employing the light tube array 20 requires enough space for diffusion of the light, which rules out the possibility of further slimming direct-type LCD apparatuses in this regard. Besides, existing technology is implemented in

2:1-7

**EXHIBIT L-25**  
**U.S. PATENT NO. 6,734,926**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 1**

1. A display apparatus comprising:  
an upper frame;  
a display panel installed inside the upper frame for displaying images;  
an array of light tubes disposed behind the display panel for generating light;  
a reflecting plate disposed behind the array of light tubes for reflecting light generated by the array of light tubes, the reflecting plate having a main portion and at least one side portion being tilted with respect to the main portion;  
a supporting frame installed on the reflecting plate for supporting the display panel, the supporting frame comprising a plurality of sub-frames, at least one of the sub-frames being tilted with respect to the main portion of the reflecting plate and being separated from the side portion by a gap; and  
a circuit board installed within the gap for controlling operations of the display apparatus.

**ASSERTED CLAIM 22**

22. A display apparatus comprising:  
an upper frame;  
a display panel installed inside the upper frame for displaying images;  
an array of light tubes disposed behind the display panel for generating light;  
a reflecting sheet disposed behind the array of light tubes for reflecting light generated by the array of light tubes;  
a supporting plate having a main portion and at least one side portion being tilted with respect to the main portion, the main portion used for supporting the reflecting sheet;  
a supporting frame installed on the main portion of the supporting plate for supporting the display panel; and  
a circuit board installed on the side portion of the supporting plate for controlling operations of the display apparatus.

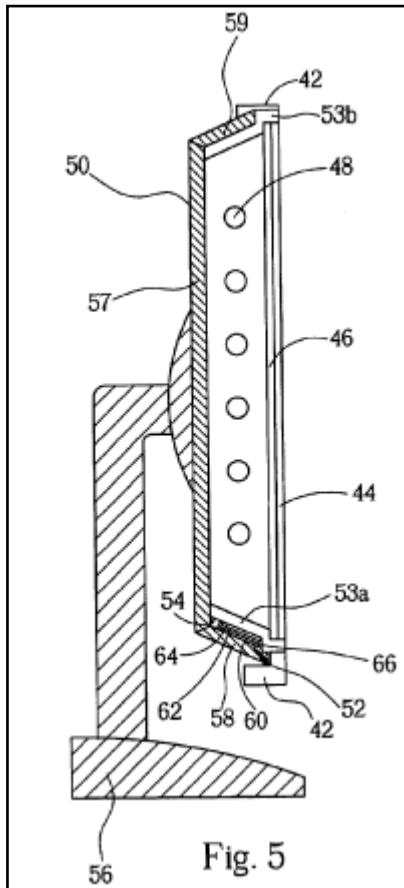
**LGD's Claim Construction**

**a circuit board installed within the gap for controlling operations of the display apparatus<sup>1</sup>** - a control circuit board is mounted in the space bounded by the sub-frame and the side portion and no control circuit board is located on the back of the supporting plate or reflecting plate

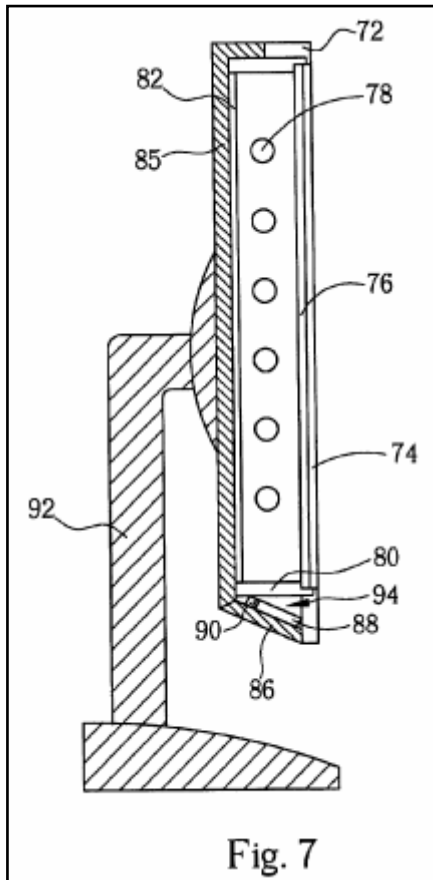
**a circuit board installed on the side portion of the supporting plate for controlling operations of the display apparatus** – a control circuit board is mounted to the side of the supporting plate and no control circuit board is located on the back of the supporting plate or reflecting plate

<sup>1</sup> Disputed Term “a circuit board installed within the gap for controlling operations of the display apparatus” also appears in asserted claim 8 in the same context.

**INTRINSIC EVIDENCE FOR DISPUTED TERM “A CIRCUIT BOARD INSTALLED WITHIN THE GAP FOR CONTROLLING OPERATIONS OF THE DISPLAY APPARATUS”:**



**INTRINSIC EVIDENCE FOR DISPUTED TERM “A CIRCUIT BOARD INSTALLED WITHIN THE GAP FOR CONTROLLING OPERATIONS OF THE DISPLAY APPARATUS” (cont’d):**



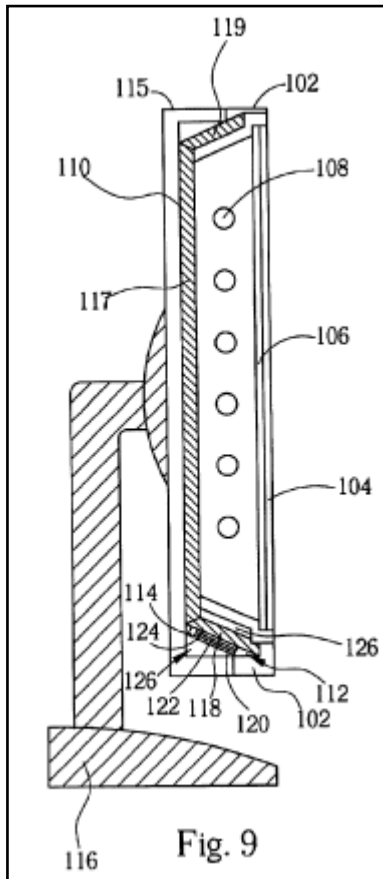
board 88 for controlling the display panel 74, and a connector 90 for receiving display data sent by an external display controller such as a VGA card of a computer system. The circuit board 88 is installed within the gap 94.

In this second preferred embodiment, the circuit board 88 can be a rigid circuit board or a printed circuit board. The circuit board 88 could also include an electromagnetic interference shield to shield the electromagnetic radiation generated by the circuit board 88. For example, a heatsink covering the circuit board 88 not only prevents the circuit board 88 from running under high temperature, but also functions as an electromagnetic interference shield.

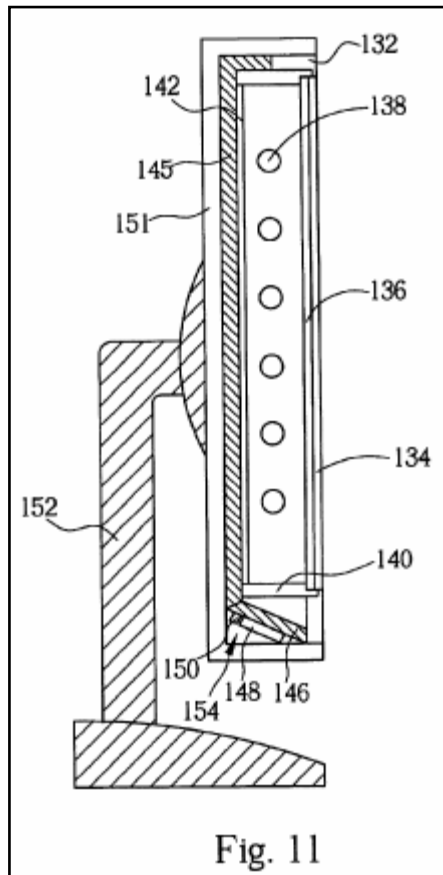
As mentioned above, the circuit board 88 is installed within the gap 94 without increasing thickness of the LCD apparatus 40. Besides, for further reducing the weight, the supporting plate 84 serves a part of the frame of the LCD apparatus 40. A stand assembly 92 could be further provided

5:18-34

**INTRINSIC EVIDENCE FOR DISPUTED TERM “A CIRCUIT BOARD INSTALLED WITHIN THE GAP FOR CONTROLLING OPERATIONS OF THE DISPLAY APPARATUS” (cont’d):**



**INTRINSIC EVIDENCE FOR DISPUTED TERM “A CIRCUIT BOARD INSTALLED WITHIN THE GAP FOR CONTROLLING OPERATIONS OF THE DISPLAY APPARATUS” (cont’d):**



1. Field of the Invention

The present invention relates to a Liquid Crystal Display (LCD) apparatus with a reduced thickness, and more specifically, to an LCD apparatus with no control circuit board installed onto the back of the back light unit.

1:7-11

**INTRINSIC EVIDENCE FOR DISPUTED TERM “A CIRCUIT BOARD INSTALLED WITHIN THE GAP FOR CONTROLLING OPERATIONS OF THE DISPLAY APPARATUS” (cont’d):**

It is an advantage of the claimed invention, in which no circuit board is installed on the back side of the direct-type back light unit, such that the display apparatus has a simplified frame structure and is therefore slimmer and more convenient to use. It is a further advantage of the claimed invention that production cost of the display apparatus is greatly reduced.

3:18-24

supporting frame 111. A stand assembly 116 could be further provided and coupled to either the reflecting plate 117 or the lower frame 115 to support the LCD apparatus 40. Without any circuit board 112 is installed on the back of the reflecting plate 110, the thickness of the LCD apparatus 40 is reduced.

Please refer to FIG. 10 and FIG. 11. FIG. 10 is an exploded perspective view of a fourth embodiment of the present invention and FIG. 11 is a cross-sectional view of the forth embodiment along a line 5-5" shown in FIG. 3. The

6:23-31

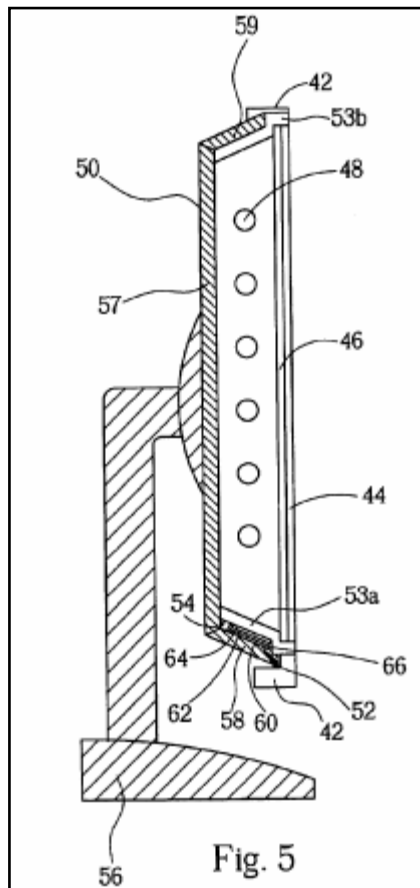
supporting plate 144 and supporting frame 140. A stand assembly 152 could be further provided and coupled to either the supporting plate 144 or the lower frame 151 to support the LCD apparatus 40. Without any circuit board 148 installed on the back side of the reflecting plate 144, the thickness of the LCD apparatus 40 is reduced.

6:59-64

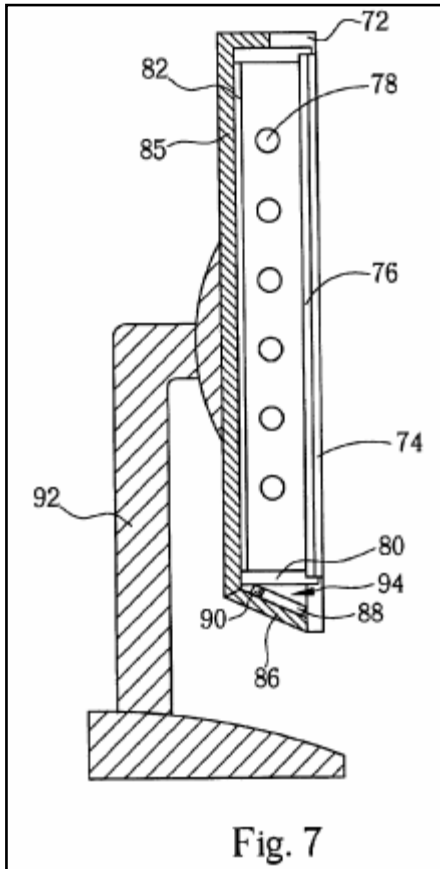
the lower frame (third and fifth embodiments), or the side portion of the reflecting plate and the lower frame (fourth and sixth embodiments) to house the circuit board and related elements. As a result, the thickness of the direct-type LCD apparatus is reduced without the circuit board and related elements positioned at the back of the LCD apparatus. Therefore, it makes the LCD apparatus more convenient to use. Furthermore, the present invention utilizes the main

8:10-17

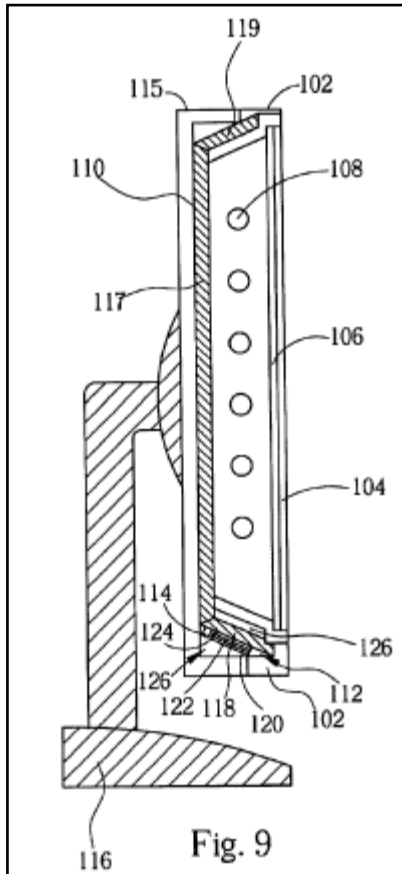
**INTRINSIC EVIDENCE FOR DISPUTED TERM “A CIRCUIT BOARD INSTALLED ON THE SIDE PORTION OF THE SUPPORTING PLATE FOR CONTROLLING OPERATIONS OF THE DISPLAY APPARATUS”:**



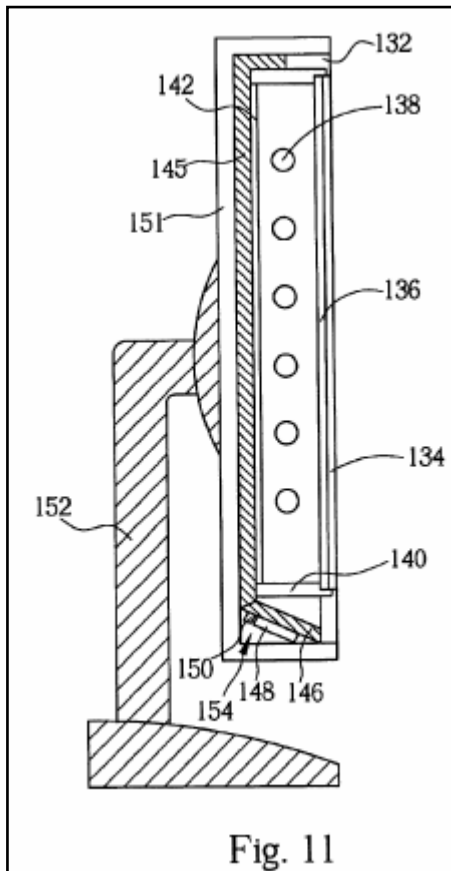
**INTRINSIC EVIDENCE FOR DISPUTED TERM “A CIRCUIT BOARD INSTALLED ON THE SIDE PORTION OF THE SUPPORTING PLATE FOR CONTROLLING OPERATIONS OF THE DISPLAY APPARATUS” (cont’d):**



**INTRINSIC EVIDENCE FOR DISPUTED TERM “A CIRCUIT BOARD INSTALLED ON THE SIDE PORTION OF THE SUPPORTING PLATE FOR CONTROLLING OPERATIONS OF THE DISPLAY APPARATUS” (cont’d):**



**INTRINSIC EVIDENCE FOR DISPUTED TERM “A CIRCUIT BOARD INSTALLED ON THE SIDE PORTION OF THE SUPPORTING PLATE FOR CONTROLLING OPERATIONS OF THE DISPLAY APPARATUS” (cont’d):**



1. Field of the Invention

The present invention relates to a Liquid Crystal Display (LCD) apparatus with a reduced thickness, and more specifically, to an LCD apparatus with no control circuit board installed onto the back of the back light unit.

1:7-11

**INTRINSIC EVIDENCE FOR DISPUTED TERM “A CIRCUIT BOARD INSTALLED ON THE SIDE PORTION OF THE SUPPORTING PLATE FOR CONTROLLING OPERATIONS OF THE DISPLAY APPARATUS” (cont’d):**

It is an advantage of the claimed invention, in which no circuit board is installed on the back side of the direct-type back light unit, such that the display apparatus has a simplified frame structure and is therefore slimmer and more convenient to use. It is a further advantage of the claimed invention that production cost of the display apparatus is greatly reduced.

3:18-24

supporting frame 111. A stand assembly 116 could be further provided and coupled to either the reflecting plate 117 or the lower frame 115 to support the LCD apparatus 40. Without any circuit board 112 is installed on the back of the reflecting plate 110, the thickness of the LCD apparatus 40 is reduced.

Please refer to FIG. 10 and FIG. 11. FIG. 10 is an exploded perspective view of a fourth embodiment of the

6:23-29

supporting plate 144 and supporting frame 140. A stand assembly 152 could be further provided and coupled to either the supporting plate 144 or the lower frame 151 to support the LCD apparatus 40. Without any circuit board 148 installed on the back side of the reflecting plate 144, the thickness of the LCD apparatus 40 is reduced.

6:59-64

the lower frame (third and fifth embodiments), or the side portion of the reflecting plate and the lower frame (fourth and sixth embodiments) to house the circuit board and related elements. As a result, the thickness of the direct-type LCD apparatus is reduced without the circuit board and related elements positioned at the back of the LCD apparatus. Therefore, it makes the LCD apparatus more convenient to use. Furthermore, the present invention utilizes the main

8:10-17

**EXHIBIT L-25**  
**U.S. PATENT NO. 6,734,926**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 8**

8. A display apparatus comprising:  
an upper frame;  
a display panel installed inside the upper frame for displaying images;  
an array of light tubes disposed behind the display panel for generating light;  
a reflecting sheet disposed behind the array of light tubes for reflecting light generated by the array of light tubes;  
a supporting plate having a main portion and at least one side portion being tilted with respect to the main portion, the main portion used for supporting the reflecting sheet;  
a supporting frame disposed on the supporting plate for supporting the display panel, the supporting frame comprising a plurality of sub-frames, at least one of the sub-frames being tilted with respect to the main portion of the supporting plate and being separated from the side portion of the supporting plate by a gap; and  
a circuit board installed within the gap for controlling operations of the display apparatus.

**LGD's Claim Construction**

**being separated from the side portion of the supporting plate by a gap** – positioned to form a space bounded by a sub-frame and a side portion

**ASSERTED CLAIM 29**

29. A display apparatus comprising:  
an upper frame;  
a display panel installed inside the upper frame for displaying images;  
an array of light tubes disposed behind the display panel for generating light;  
an integrated supporting unit disposed behind the array of light tubes having a main portion and at least one side portion being tilted with respect to the main portion for reflecting light generated by the array of light tubes and supporting the display panel; and  
a circuit board installed on at least one of the side portions of the reflecting plate for controlling operations of the display apparatus.

**integrated supporting unit<sup>1</sup>** – a unitary structure that provides support

<sup>1</sup> Disputed Term “integrated supporting unit” also appears in asserted claims 31, 36, and 38 in the same context.

**INTRINSIC EVIDENCE FOR DISPUTED TERM “BEING SEPARATED FROM THE SIDE PORTION OF THE SUPPORTING PLATE BY A GAP”:**

board or a printed circuit board. The circuit board 52 could also include an electromagnetic interference shield to shield the electromagnetic radiation generated by the circuit board 52. In this embodiment, the circuit board 52 of the direct-type LCD apparatus 40 is installed onto either the side portion 58 of the reflecting plate 57 or the sub-frame 53a of the supporting frame 51 by making use of the gap 66.

4:33-39

As mentioned above, the circuit board 88 is installed within the gap 94 without increasing thickness of the LCD apparatus 40. Besides, for further reducing the weight, the supporting plate 84 serves a part of the frame of the LCD apparatus 40. A stand assembly 92 could be further provided and coupled to either the supporting plate 84 to support the LCD apparatus 40.

5:30-36

The present invention is not limited by the second preferred embodiment described. For example, one end of the stand assembly 92 can be installed on the bottom side of the upper frame 72 to support the entire LCD apparatus 40. Additionally, the gap 94 can exist in any side of the LCD apparatus 40 through appropriate arrangement of the side portion 86. For example, when the side portion 86 is positioned on the top of the main portion 85, the gap 94 will exist on the top of the LCD apparatus 40. In addition, the

5:37-45

to the main portion 117. The main portion 117 of the reflecting plate 110 along with the supporting frame 111 constitute a reflecting surface, which reflects the light generated by the light tube array 108. It is noteworthy that a gap 126 exists between the side portion 118 and the lower frame 115. Then, the circuit board 112 is installed within the gap 126. The circuit board 112 comprises at least an X-board 120 to drive pixels in the same row for displaying corresponding

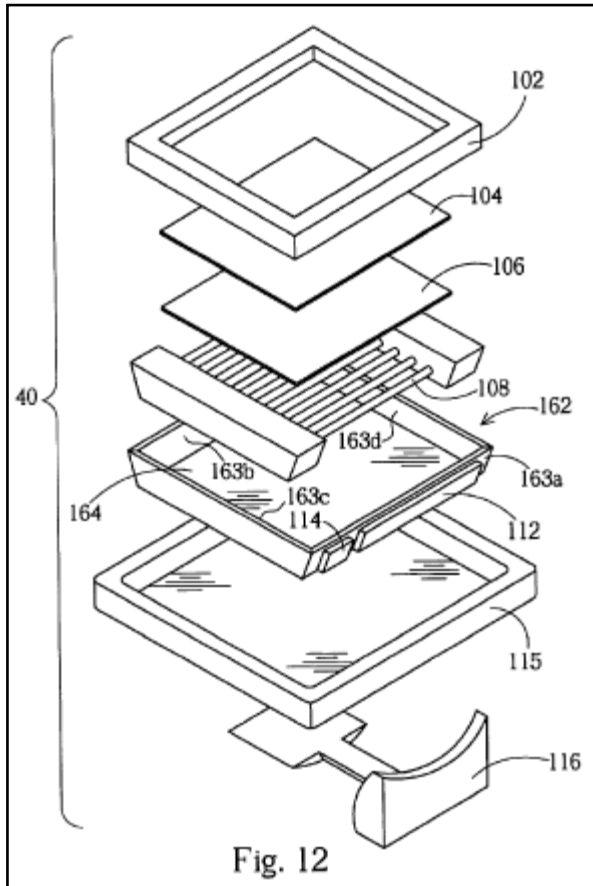
6:3-10

**INTRINSIC EVIDENCE FOR DISPUTED TERM “BEING  
SEPARATED FROM THE SIDE PORTION OF THE  
SUPPORTING PLATE BY A GAP” (cont’d):**

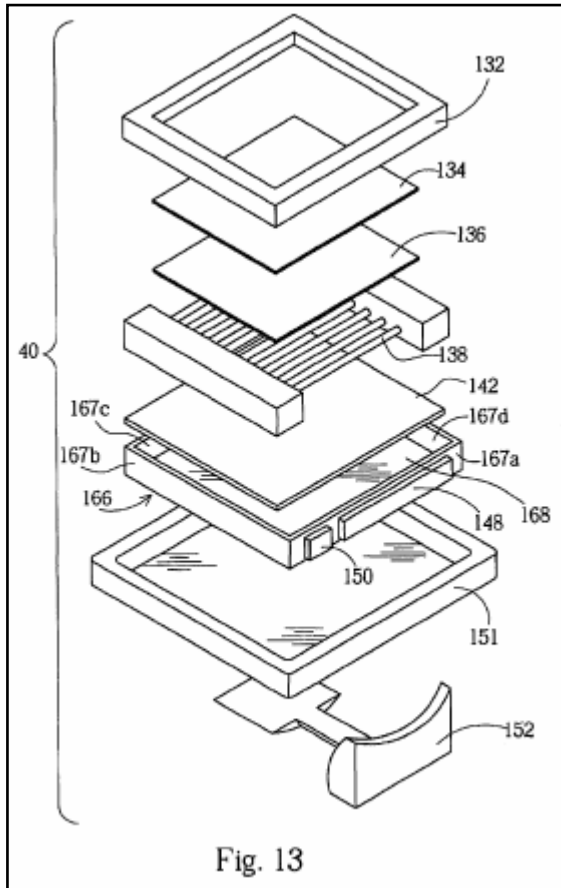
Compared with the prior art direct-type LCD apparatus, the present invention utilizes the space between the side portions of the reflecting plate and the supporting frame (first preferred embodiment), the side portions of the supporting plate and the supporting frame (second preferred embodiment), the side portion of the supporting plate and the lower frame (third and fifth embodiments), or the side portion of the reflecting plate and the lower frame (fourth and sixth embodiments) to house the circuit board and related elements. As a result, the thickness of the direct-type LCD apparatus is reduced without the circuit board and related elements positioned at the back of the LCD apparatus. Therefore, it makes the LCD apparatus more convenient to use. Furthermore, the present invention utilizes the main portion of the reflecting plate (first preferred embodiment) or

8:4-18

**INTRINSIC EVIDENCE FOR DISPUTED TERM**  
**“INTEGRATED SUPPORTING UNIT”:**



**INTRINSIC EVIDENCE FOR DISPUTED TERM**  
**“INTEGRATED SUPPORTING UNIT” (cont’d):**



**INTRINSIC EVIDENCE FOR DISPUTED TERM**  
**“INTEGRATED SUPPORTING UNIT” (cont’d):**

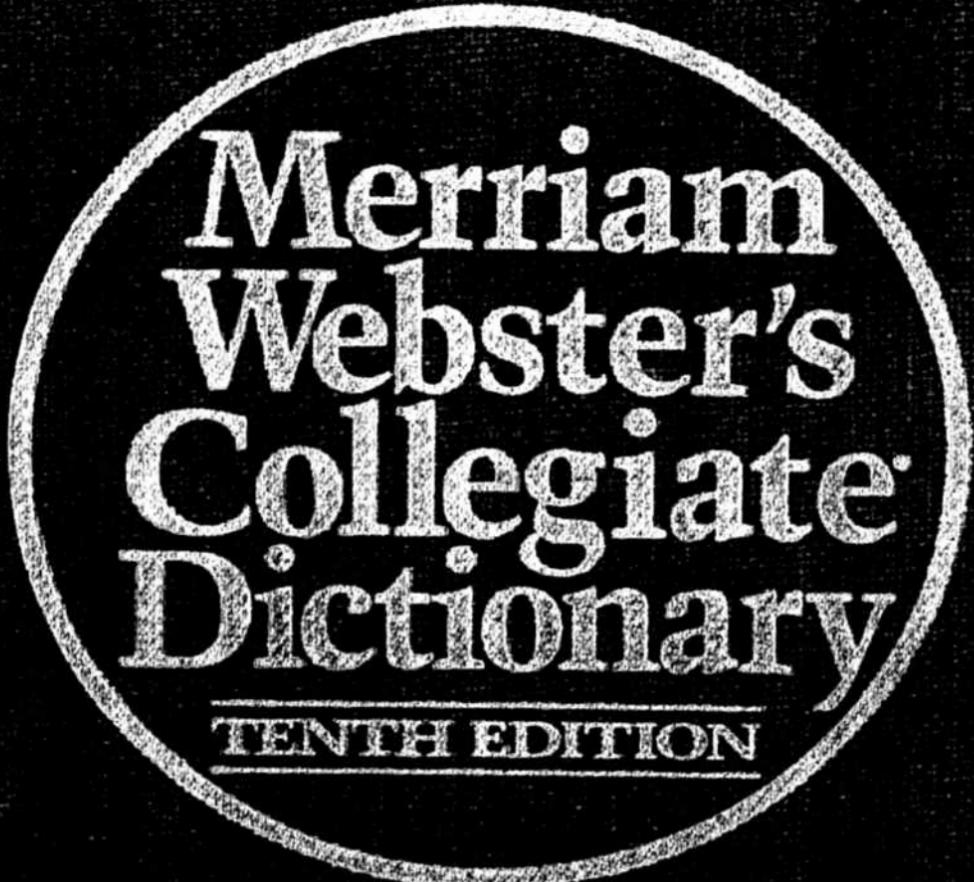
embodiment and the third embodiment is that the reflecting plate 110 shown in FIG. 8 incorporates the supporting frame 111 shown in FIG. 8 to form an integrated supporting unit 162. The integrated supporting unit 162 further simplifies the whole structure of the LCD apparatus 40, and accordingly reduces thickness and cost of the LCD apparatus 40. The integrated supporting unit 162 comprises four sub-frames 163a, 163b, 163c, 163d and a main portion 164. The sub-frames 163a, 163b, 163c, 163d are mainly used to make the LCD apparatus 40 firm and solid. The main portion 164 is mainly used to reflect light generated by the light tube array 108. In other words, the integrated supporting unit 162 in the fifth embodiment has two functions originally provided by the reflecting plate 110 and the supporting frame 111. The connector 114 and the circuit board 112, therefore,

7:1-15

Please refer to FIG. 13, which illustrates components of the LCD apparatus 40 according to a sixth embodiment of the present invention. The only difference between this sixth embodiment and the forth embodiment is that the supporting plate 144 shown in FIG. 10 incorporates the supporting frame 140 shown in FIG. 10 to form an integrated supporting unit 166. The integrated supporting unit 166 further simplifies the whole structure of the LCD apparatus 40, and accordingly reduces thickness and cost of LCD apparatus 40. The integrated supporting unit 166 comprises four sub-frames 167a, 167b, 167c, 167d and a main portion 168. The integrated supporting unit 166 is mainly used to make the LCD apparatus 40 firm and solid. The reflecting sheet 142 for reflecting light generated by the light tube array 138 is positioned onto the main portion 168. The connector 150

7:26-40

# **EXHIBIT L-27(a)**

The image shows the front cover of a Merriam Webster's Collegiate Dictionary. The cover is dark with a fine, woven texture. In the center, there is a large, light-colored circular emblem. Inside this circle, the words "Merriam Webster's Collegiate Dictionary" are printed in a large, bold, serif font, stacked in four lines. Below the main title, the words "TENTH EDITION" are printed in a smaller, all-caps, serif font, flanked by two horizontal lines.

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Library of Congress Cataloging in Publication Data  
Main entry under title:

Merriam-Webster's collegiate dictionary. — 10th ed.

p. cm.

ISBN 0-87779-708-0 (unindexed). — ISBN 0-87779-709-9 (indexed).

— ISBN 0-87779-710-2 (deluxe). — ISBN 0-87779-707-2 (laminated cover).

1. English language—Dictionaries.

PE1628.M36 1994

423—dc20

93-32603

CIP

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## 480 gaol • garnishment

**gaol** \jā(ə)l\, **gaol-er** \jā-lər\ chiefly Brit var of JAIL, JAILER

**gap** \gəp\ *n* [ME, fr. ON, chasm, hole; akin to ON *gapa* to gape] (14c)  
**1 a** : a break in a barrier (as a wall, hedge, or line of military defense)  
**b** : an assailable position **2 a** : a mountain pass **b** : RAVINE **3** : SPARK GAP **4 a** : a separation in space **b** : an incomplete or deficient area (a ~ in her knowledge) **5** : a break in continuity : HIATUS **6** : a break in the vascular cylinder of a plant where a vascular trace departs from the central cylinder **7** : lack of balance : DISPARITY (the ~ between imports and exports) **8** : a wide difference in character or attitude (the generation ~) **9** : a problem caused by some disparity (a communication ~) (credibility ~) — **gap-py** \gə-pē\ *adj*

**gap vb gapped; gap-ping** *vt* (1879) **1** : to make an opening in **2** : to adjust the space between the electrodes of (a spark plug) ~ *vi* : to fall or stand open

**gape** \gəp\ *sometimes* \gəp\ *vi* **gaped; gap-ing** [ME, fr. ON *gapa*; perh. akin to L *hiare* to gape, yawn — more at YAWN] (13c) **1 a** : to open the mouth wide **b** : to open or part widely (holes gaped in the pavement) **2** : to gaze stupidly or in openmouthed surprise or wonder **3** : YAWN — **gap-ing-ly** \gə-pīŋ-lē, -gə-pīŋ-lē\ *adv*

**gape** *n* (1535) **1** : an act of gaping : **a** : YAWN **b** : an openmouthed stare **2** : an unfilled space or extent **3 a** : the median margin-to-margin length of the open mouth **b** : the line along which the mandibles of a bird close **c** : the width of an opening **4 pl** but sing in constr **a** : a disease of birds and esp. young birds in which gapeworms invade and irritate the trachea **b** : a fit of yawning

**gap-er** \gə-pər\ *sometimes* \gə-pər\ *n* (ca. 1637) **1** : one that gapes **2** : any of several large sluggish burrowing clams (families Myacidae and Mactridae) including several used for food

**gape-worm** \gəp-wərm\ *sometimes* \gəp-w\ *n* (1873) : a nematode worm (*Syngamus trachea*) that causes gaps in birds

**gap-ing** \gə-pīŋ\ *adj* (1588) : wide open (a ~ hole)

**gap junction** *n* (1967) : an area of contact between adjacent cells characterized by modification of the cell membranes for intercellular communication or transfer of low molecular-weight substances

**gapped scale** *n* (1910) : a musical scale derived from a larger system of tones by omitting certain tones

**gap-toothed** \gəp-tūth\ *adj* (1567) : having gaps between the teeth

**gar** \gär\ *interj* [euphemism for God] (1598) — used as a mild oath in the phrase by gar

**gar** *n* [short for *garfish*] (1765) : any of various fishes that have an elongate body resembling that of a pike and long and narrow jaws : as **a** : NEEDLEFISH **1 b** : any of several predaceous No. American freshwater bony fishes (family Lepisosteidae) with heavy ganoid scales

**gar-age** \gə-rāzh, -rāj\, chiefly Brit *Eng* -rāzh, -rāj; *Canad* also -rāzh, -rāj; *Brit* usu \gär-ājzh, -āj\, -āj\, -ij\ *n* [F, act of docking, garage, fr. *garer* to dock, of Gmc origin; akin to OHG *biwarōn* to protect — more at WARE] (1902) : a shelter or repair shop for automotive vehicles

**garage** *vt* **gar-aged; gar-rag-ing** (1905) : to keep or put in a garage

**gar-age-man** \-man\ *n* (1919) : one who works in a garage

**garage sale** *n* (1964) : a sale of used household or personal articles (as furniture, tools, or clothing) held on the seller's own premises

**gar-ram ma-sa-la** \gä-räm-mä-sä-lä\ *n* [Hindi *garam masālā*, lit., hot spices] (1970) : a pungent and aromatic mixture of ground spices used in Indian cooking

**Gar-and rifle** \gə-ränd-, -gär-ənd-\ *n* [John C. Garand] (1931) : M1 RIFLE

**garb** \gärb\ *n* [MF or OIt; MF *garbe* graceful contour, grace, fr. OIt *garbo* grace] (1599) **1 obs** : FASHION, MANNER **2 a** : a style of apparel **b** : outward form : APPEARANCE

**garb** *vt* (1846) : to cover with or as if with clothing (~ed in T-shirt and blue jeans)

**gar-bage** \gär-bij\ *n* [ME, offal] (15c) **1 a** : food waste : REFUSE **b** : unwanted or useless material **2 a** : TRASH **1b b** : inaccurate or useless data

**gar-bage-man** \-man\ *n* (1888) : one who collects and hauls away garbage

**gar-ban-zo** \gär-bän-(z)ō, also -ban-\ *n*, *pl* -zos [Sp] (1759) : CHICK-PEA

**garbanzo bean** *n* (1944) : CHICKPEA

**gar-ble** \gär-bəl\ *vt* **gar-bled; gar-bling** \-b(ə-)līŋ\ [ME *garbelen*, fr. OIt *garbellare* to sift, fr. Ar *gharbala*, fr. LL *cribellare*, fr. *cribellum* sieve; akin to L *cernere* to sift — more at CERTAIN] (15c) **1 archaic** : CULL **2** : to sift impurities from **3 a** : to so alter or distort as to create a wrong impression or change the meaning (~ a story) **b** : to introduce textual error into (a message) by inaccurate encipherment, transmission, or decipherment — **gar-bler** \-b(ə-)lər\ *n*

**garble** *n* (1502) **1** : the impurities removed from spices in sifting **2** : an act or an instance of garbling

**gar-board** \gär-börd, -börd\ *n* [obs. D *gaarboord*] (1627) : the strake next to a ship's keel

**gar-boil** \-bōil\ *n* [MF *garbouil*, fr. OIt *garbuglio*] (1548) *archaic* : a confused disordered state : TURMOIL

**gar-çon** \gär-sōŋ\ *n*, *pl* **garçons** \-sōŋ(z)\ [F, boy, servant, fr. OF, of Gmc origin; akin to OHG *hrechjo* fugitive — more at WRETCH] (1788) : WAITER

**garde-man-ger** \gärd-män-'zhā\ *n*, *pl* **garde-mangers** \-'zhā(z)\ [F, lit., one who keeps food] (1928) : a cook who specializes in the preparation of cold foods (as meats, fish, and salads)

**gar-den** \gär-dn\ *n* [ME *gardin*, fr. ONF, of Gmc origin; akin to OHG *gart* enclosure — more at YARD] (13c) **1 a** : a plot of ground where herbs, fruits, flowers, or vegetables are cultivated **b** : a rich well-cultivated region **c** : a container (as a window box) planted with usu. a variety of small plants **2 a** : a public recreation area or park usu. ornamented with plants and trees (a botanical ~) **b** : an open-air eating or drinking place **c** : a large hall for public entertainment — **gar-den-ful** \-fūl\ *adj*

**garden** *vb* **gar-dened; gar-den-ing** \gär-'d-n-īŋ, -gärd-nīŋ\ *vi* (1577) : to lay out or work in a garden ~ *vt* **1** : to make into a garden **2** : to ornament with gardens — **gar-den-er** \gär-dn-ər, -gärd-nər\ *n*

**garden** *adj* (1622) **1** : of, relating to, used in, or frequenting a garden **2 a** : of a kind grown in the open as distinguished from one more delicate (~ plant) **b** : commonly found : GARDEN-VARIETY

**garden apartment** *n* (1946) : a multiple-unit low-rise dwelling having considerable lawn or garden space

**garden city** *n* (1898) : a planned residential community with park and planted areas

**garden cress** *n* (1577) : an annual herb (*Lepidium sativum*) of the mustard family sometimes cultivated for its pungent basal leaves

**garden heliotrope** *n* (ca. 1902) : a tall rhizomatous Old World valerian (*Valeriana officinalis*) widely cultivated for its fragrant tiny flowers and for its roots which yield the drug valerian

**gar-de-nia** \gär-dē-nyā\ *n* [NL, fr. Alexander Garden †1791 Scot. naturalist] (1760) : any of a large genus (*Gardenia*) of Old World tropical trees and shrubs of the madder family with showy fragrant white or yellow flowers

**Garden of Eden** (1535) : EDEN

**garden rocket** *n* (1832) : ARUGULA

**garden-variety** *adj* (1928) : ORDINARY, COMMONPLACE

**garde-robe** \gär-drōb\ *n* [ME, fr. MF; akin to ONF *wardrobe* wardrobe] (15c) **1** : a wardrobe or its contents **2** : a private room : BED-ROOM **3** : PRIVY

**gar-dy-loo** \gär-dē-lü\ *interj* [perh. fr. F *garde à l'eau!* look out for the water!] (1622) — used in Edinburgh as a warning cry when it was customary to throw slops from the windows into the streets

**Gar-eth** \gär-əth\ *n* : a knight of the Round Table and nephew of King Arthur

**gar-fish** \gär-fish\ *n* [ME *garfyshe*] (15c) : GAR

**Gar-gan-tua** \gär-gan(t)-sh(ə)-wə\ *n* [F] : a gigantic king in Rabelais' *Gargantua* having a great capacity for food and drink

**gar-gan-tuan** \-wən\ *adj*, often *cap* [*Gargantua*] (1596) : of tremendous size or volume : GIGANTIC, COLOSSAL (entire cities fleeing before ~ walls of water — William Cleary)

**gar-gle** \gär-gəl\ *vb* **gar-gled; gar-gling** \-g(ə-)līŋ\ [MF *gargouiller*, of imit. origin] *vt* (1527) **1 a** : to hold (a liquid) in the mouth or throat and agitate with air from the lungs **b** : to cleanse or disinfect (the oral cavity) in this manner **2** : to utter with a gargling sound ~ *vi* **1** : to use a gargle **2** : to speak or sing as if gargling

**gargle** *n* (1657) **1** : a liquid used in gargling **2** : a sound of or like that of gargling

**gar-goyle** \gär-göyl\ *n* [ME *gargoyl*, fr. MF *gargouille*; akin to MF *gargouiller*] (13c) **1 a** : a spout in the form of a grotesque human or animal figure projecting from a roof gutter to throw rainwater clear of a building **b** : a grotesquely carved figure **2** : a person with an ugly face — **gar-goyled** \-göild\ *adj*

**gar-i-bal-di** \gär-ə-böl-dē\ *n* (1862) : a woman's blouse copied from the red shirt worn by the Italian patriot Garibaldi

**gar-rigue** \gä-rēg\ *n* [F] (1896) : a low open scrubland with many evergreen shrubs, low trees, aromatic herbs, and bunchgrasses found in poor or dry soil in the Mediterranean region

**gar-ish** \gär-ish, -ger-\ *adj* [origin unknown] (1545) **1** : clothed in vivid colors **2 a** : excessively vivid : FLASHY **b** : offensively or distastefully bright : GLARING **3** : tastelessly showy *syn* see GAUDY — **gar-ish-ly** *adv* — **gar-ish-ness** *n*

**gar-land** \gär-lənd\ *n* [ME, fr. MF *garlande*] (14c) **1** : WREATH, CHAPLET **2** : ANTHOLOGY, COLLECTION

**garland** *vt* (15c) **1** : to form into a garland **2** : to adorn with or as if with a garland

**gar-lic** \gär-lik\ *n* [ME *garlek*, fr. OE *gārleac*, fr. *gār* spear + *leac* leek — more at GORE] (bef. 12c) **1** : a European bulbous herb (*Allium sativum*) of the lily family widely cultivated for its pungent compound bulbs much used in cooking; *broadly* : any plant of the same genus **2** : a bulb of garlic — **gar-licky** \-li-kē\ *adj*

**gar-licked** \gär-lik\ *adj* (1950) : containing or prepared with garlic (a ~ sauce) (~ roast lamb)

**garlic salt** *n* (1927) : a seasoning of ground dried garlic and salt

**gar-ment** \gär-mənt\ *n* [ME, fr. MF *garnement*, fr. OF, fr. *garnir* to equip — more at GARNISH] (14c) : an article of clothing

**garment** *vt* (1547) : to clothe with or as if with a garment

**gar-ner** \gär-nər\ *n* [ME, fr. OF *garnier*, *grenier*, fr. L *granarium*, fr. *granum* grain — more at CORN] (12c) **1 a** : GRANARY **b** : a grain bin **2** : something that is collected : ACCUMULATION

**garner** *vt* **gar-nered; gar-ner-ing** \gärn-rīp, -gär-nə-\ (14c) **1 a** : to gather into storage **b** : to deposit as if in a granary (volumes in which he has ~ed the fruits of his lifetime labors — Reinhold Niebuhr) **2 a** : to acquire by effort : EARN **b** : ACCUMULATE, COLLECT

**gar-net** \gär-nət\ *n* [ME *grenat*, fr. MF, fr. *grenat*, *adj.*, red like a pomegranate, fr. (*pomme*) *grenate* pomegranate] (14c) **1** : a brittle and more or less transparent usu. red silicate mineral that has a vitreous luster, occurs mainly in crystals but also in massive form and in grains, is found commonly in gneiss and mica schist, and is used as a semiprecious stone and as an abrasive **2** : a variable color averaging a dark red — **gar-net-if-er-ous** \gär-nə-'ti-f(ə)-rəs\ *adj*

**garnet paper** *n* (ca. 1902) : an abrasive paper with crushed garnet as the abrasive

**gar-ni-er-ite** \gär-nē-ə-rīt\ *n* [Jules Garnier †1904 Fr. geologist] (1875) : a soft mineral consisting of hydrous nickel magnesium silicate and constituting an important ore of nickel

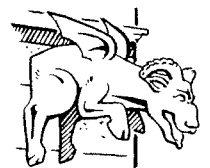
**gar-nish** \gär-nish\ *vt* [ME, fr. MF *garniss-*, stem of *garnir* to warn, equip, garnish, of Gmc origin; akin to OHG *warnōn* to take heed — more at WARN] (14c) **1 a** : DECORATE, EMBELLISH **b** : to add decorative or savory touches to (food or drink) **2** : to equip with accessories : FURNISH **3** : GARNISH *syn* see ADORN

**garnish** *n* (1596) **1** : EMBELLISHMENT, ORNAMENT **2** : something (as lemon wedges or parsley) used to garnish food or drink **3 a** : an unauthorized fee formerly extorted from a new inmate of an English jail **b** : a similar payment required of a new worker

**gar-nish-ee** \gär-nə-'shē\ *n* (1627) : a person who is served with a garnishment

**garnish-ee** *vt* **-eed; -ee-ing** (ca. 1876) **1** : to serve with a garnishment **2** : to take (as a debtor's wages) by legal authority

**gar-nish-ment** \gär-nish-mənt\ *n* (1530) **1** : GARNISH **2** : a legal summons or warning concerning the attachment of property to satisfy a debt **3** : a stoppage of a specified sum from wages to satisfy a creditor



gargoyle 1a

# **EXHIBIT L-28**

**EX. L-28**  
**CMO US PATENT NO. 6,134,092**

**INDEX OF DISPUTED TERMS**

<b><u>CLAIM TERMS</u></b>	<b><u>PAGE</u></b>
peripheral portion.....	6
a series of point light sources.....	1
diffusive reflective surfaces .....	1
oriented relative to the series of point light sources and the waveguide so as to introduce light .....	1
whereby the peripheral portion of the waveguide is substantially uniformly illuminated .....	6
light-emitting diodes mounted on an electrical-conductive strip of material .....	10
mouth .....	10
diffusive reflective optical cavities .....	1
guide members positioned along a periphery of the optical cavity .....	13
whereby light is injected from said exit mouths into a peripheral portion of said optical cavity .....	6

**EXHIBIT L-28**  
**U.S. PATENT NO. 6,134,092**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 1**

1. An illumination device, comprising:  
a waveguide having a peripheral portion;  
a series of point light sources mounted in spaced relationship adjacent the peripheral portion of the waveguide;  
a series of diffusive reflective surfaces adjacent the peripheral portion of the waveguide and between pairs of said point light sources, the diffusive reflective surfaces oriented relative to the series of point light sources and the waveguide so as to introduce light in regions of said waveguide between pairs of said point light sources whereby the peripheral portion of the waveguide is substantially uniformly illuminated.

**ASSERTED CLAIM 12**

12. An illumination device, comprising:  
a series of diffusive reflective optical cavities formed by diffusive reflective surfaces, each of said cavities having an entry mouth sized to receive a point light source and an exit mouth;  
a point light source mounted at each of the entry mouths;  
a pair of surfaces forming a waveguide, said waveguide having a peripheral portion extending along the exit mouths of said diffusive reflective optical cavities.

**LGD's Claim Construction**

**a series of point light sources**

- a sequence of separate components, such as light-emitting diodes, that provide the desired light that illuminates the waveguide or optical cavity

**diffusive reflective surfaces -**

non-transparent boundaries of an object that reflect and scatter light from the point light source

**oriented relative to the series of point light sources and the waveguide so as to introduce light -**

arranged to be substantially perpendicular to the top surface of the waveguide so as to introduce scattered light reflected directly from the point light sources into the waveguide

**diffusive reflective optical**

**cavities<sup>1</sup>** - optical passages having non-transparent surfaces that reflect and scatter light from the point light source

<sup>1</sup> Disputed Term "the diffusive reflective surfaces" also appears in asserted claim 2, 4, 12, 13, 21, 25, 26 and 28 in the same context.

**INTRINSIC EVIDENCE FOR DISPUTED TERM “A SERIES OF POINT LIGHT SOURCES”:**

In accordance with another aspect of the invention, a series of diffusive reflective optical cavities are formed by diffusive reflective surfaces. Each of the cavities has an entry mouth sized to receive a point light source and an exit mouth. A point light source is mounted at each of the entry mouths. A peripheral portion of a waveguide extends along the exit mouth of the diffusive reflective optical cavity.

1:61-65

The series of optical cavities have exit mouths disposed along a side of the aforesaid optical cavity. A series of point sources of light are mounted to emit light into the series of optical cavities, respectively, whereby light is injected from the exit mouth into a peripheral portion of the optical cavity.

2:5-9

described in more detail below. In the illustrated embodiment, each of a pair of LED strips **51**, such as printed circuit boards or electrical-conductive strips, mount the LEDs **50** in a linear array with equidistant spacing. The LEDs **50** within a strip **51** are parallel connected and the two strips **51** are series connected to one another via an electrical conductor **54**. The various components of the illumination

3:22-28

The LED strips **51** are preferably oriented so that an LED **50** is disposed at each of the mouths **71** of the spaces **70** between the guide members **60**. The bent side walls **98** of the heat sink **42** causes the convex portions **104** (FIG. 10) of the side walls **98** to exert pressure against the LED strips **51** to thereby maintain a strong mechanical contact between the heat sink **42** and the LED strips **51**. This facilitates the

6:48-54

rays into the waveguide **46**. This reflected light fills the regions between adjacent LEDs **50** to thereby provide a relatively uniform distribution of light injection from the LED **50** into the peripheral portion **93** of the waveguide **46**. The plurality of LEDs **50** along the length of the side surfaces **94** of the waveguide **46** thus provide a more or less uniform illumination profile along the peripheral portion **93** of the waveguide **46** adjacent the cavities **70**.

7:23-30

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DIFFUSIVE REFLECTIVE SURFACES”:**

An additional aspect of the invention comprises a method of illuminating a waveguide. Light emitted by a first point light source is confined using diffusive reflective surfaces to reflect the light. This confining is repeated for additional point light sources. All of the confined light is spatially arranged to substantially uniformly illuminate a peripheral portion of the waveguide.

2:10-16

walls 84 and 86 of the cover 48. Each of the walls 84 and 86 extends perpendicularly from a top wall 85. Preferably, the interior surfaces formed by the walls 84, 85, and 86 are coated with the same diffusive reflective material as the surface 57 and the surfaces 65. Additionally, the end walls 84 and 86 are sized so that the top wall 85 abuts the tops of the post-shaped guide members 60.

6:1-7

In operation, the LEDs 50 are energized to introduce light into the waveguide 46. Preferably, the LEDs emit light having a wavelength in the range of 400 nm to 700 nm. The portion of the diffusive reflective top surface 57 between the diffusive reflective surfaces 65, together with the diffusive reflective interior surface of the top wall 85 of the frame 80, and the diffusive reflective side surfaces 65 of the guide members 60 form a series of diffusive reflective air filled cavities that confine the emitted light and inject it into the side surfaces 94 of the waveguide 46. Advantageously, the guide members 60 facilitate a uniform distribution of light from the point light sources into a peripheral portion (FIG. 13) of the waveguide 46, adjacent to the cavities.

7:3-15

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “ORIENTED  
RELATIVE TO THE SERIES OF POINT LIGHT SOURCES AND THE  
WAVEGUIDE SO AS TO INTRODUCE LIGHT”:**

substantially uniformly illuminated. Preferably, the diffusive reflective surfaces comprise a series of posts mounted in spaced relationship adjacent the peripheral portion of the waveguide. In the preferred embodiment, the point light sources comprises LEDs, and a heat sink is coupled to the point light sources to draw heat therefrom. An angular spectrum restrictor, such as a brightness enhancing film, is preferably included in combination with a diffuser to enhance the brightness of the output.

1:52-60

An additional aspect of the invention comprises a method of illuminating a waveguide. Light emitted by a first point light source is confined using diffusive reflective surfaces to reflect the light. This confining is repeated for additional point light sources. All of the confined light is spatially arranged to substantially uniformly illuminate a peripheral portion of the waveguide.

2:10-16

A plurality of guide members 60 are disposed in a spaced, side-by-side relationship along each of the side edges 62a and 62b of the planar member 56. In the illustrated embodiment, each of the guide members 60 comprises a post with a triangular cross-section that extends upwardly from the top surface 57 of the planar member 56. The post-shaped guide members 60 on the edge 62a will be referred to as the members 60a and those on the edges 62b will be referred to as the members 60b. The portion of the top surface 57 between the post-shaped guide members 60a and the post-shaped guide members 60b forms a waveguide receiving region.

3:42-53

In operation, the LEDs 50 are energized to introduce light into the waveguide 46. Preferably, the LEDs emit light having a wavelength in the range of 400 nm to 700 nm. The portion of the diffusive reflective top surface 57 between the diffusive reflective surfaces 65, together with the diffusive reflective interior surface of the top wall 85 of the frame 80, and the diffusive reflective side surfaces 65 of the guide members 60 form a series of diffusive reflective air filled cavities that confine the emitted light and inject it into the side surfaces 94 of the waveguide 46. Advantageously, the guide members 60 facilitate a uniform distribution of light from the point light sources into a peripheral portion (FIG. 13) of the waveguide 46, adjacent to the cavities.

7:1-15

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DIFFUSIVE REFLECTIVE OPTICAL CAVITIES”:**

In accordance with another aspect of the invention, a series of diffusive reflective optical cavities are formed by diffusive reflective surfaces. Each of the cavities has an entry mouth sized to receive a point light source and an exit mouth. A point light source is mounted at each of the entry mouths. A peripheral portion of a waveguide extends along the exit mouth of the diffusive reflective optical cavity.

1:61-67

The series of optical cavities have exit mouths disposed along a side of the aforesaid optical cavity. A series of point sources of light are mounted to emit light into the series of optical cavities, respectively, whereby light is injected from the exit mouth into a peripheral portion of the optical cavity.

2:5-9

In operation, the LEDs 50 are energized to introduce light into the waveguide 46. Preferably, the LEDs emit light having a wavelength in the range of 400 nm to 700 nm. The portion of the diffusive reflective top surface 57 between the diffusive reflective surfaces 65, together with the diffusive reflective interior surface of the top wall 85 of the frame 80, and the diffusive reflective side surfaces 65 of the guide members 60 form a series of diffusive reflective air filled cavities that confine the emitted light and inject it into the side surfaces 94 of the waveguide 46. Advantageously, the guide members 60 facilitate a uniform distribution of light from the point light sources into a peripheral portion (FIG. 13) of the waveguide 46, adjacent to the cavities.

7:3-15

**EXHIBIT 27**  
**U.S. PATENT NO. 6,134,092**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 1**

1. An illumination device, comprising:  
a waveguide having a **peripheral portion**;  
a series of point light sources mounted in spaced relationship adjacent the **peripheral portion** of the waveguide;  
a series of diffusive reflective surfaces adjacent the **peripheral portion** of the waveguide and between pairs of said point light sources, the diffusive reflective surfaces oriented relative to the series of point light sources and the waveguide so as to introduce light in regions of said waveguide between pairs of said point light sources **whereby the peripheral portion of the waveguide is substantially uniformly illuminated.**

**LGD's Claim Construction**

**peripheral portion<sup>1</sup>** -  
boundary adjacent a side edge

**whereby the peripheral portion of the waveguide is substantially uniformly illuminated** - such that the same or nearly the same amount of light is provided along a boundary adjacent a side edge of the waveguide

**ASSERTED CLAIM 17**

17. An illumination device, comprising:  
an optical cavity having an output aperture;  
a series of diffusive reflective optical cavities each substantially smaller than said optical cavity and having an exit mouth disposed along a side of said optical cavity;  
a series of point sources of light mounted to emit light into said series of diffusive reflective optical cavities, respectively, **whereby light is injected from said exit mouths into a peripheral portion of said optical cavity.**

**whereby light is injected from said exit mouths into a peripheral portion of said optical cavity** - such that light is injected from said exit mouths into a boundary adjacent a side edge of the optical cavity

<sup>1</sup> Disputed Term "peripheral portion" also appears in asserted claim 2,4,12,17 and 26 in the same context.

## **INTRINSIC EVIDENCE FOR DISPUTED TERM “PERIPHERAL PORTION”:**

In accordance with another aspect of the invention, a series of diffusive reflective optical cavities are formed by diffusive reflective surfaces. Each of the cavities has an entry mouth sized to receive a point light source and an exit mouth. A point light source is mounted at each of the entry mouths. A peripheral portion of a waveguide extends along the exit mouth of the diffusive reflective optical cavity.

1:61-67

With reference to the exploded view of FIG. 2, the illumination device 40 comprises a plurality of components, including a heat sink 42, a light guide 44, a waveguide 46, a cover 48, and a film stack 49. A plurality of point light sources, such as light-emitting diodes (LEDs) 50, are positioned adjacent the peripheral edges of the light guide 44 and are configured to inject light into the waveguide 46, as described in more detail below. In the illustrated

3:15-21

A pair of opposed side surfaces 94a and 94b (referred to collectively as “side surfaces 94”) and a pair of opposed end surfaces 95a and 95b (referred to collectively as “end surfaces 95”) connect the top surface 90 to the bottom surface 92 and define the periphery or perimeter of the waveguide 46. The distance between the top and bottom surfaces 90 and 92 along the side surfaces 94 is substantially equal to the height of the post-shaped guide members 60, which in the disclosed embodiment is approximately 0.067 at the side surfaces 94. Preferably, the waveguide 46 is sized

5:9-18

**INTRINSIC EVIDENCE FOR DISPUTED TERM “WHEREBY THE PERIPHERAL PORTION OF THE WAVEGUIDE IS SUBSTANTIALLY UNIFORMLY ILLUMINATED”:**

of the waveguide. A series of diffusive reflective surfaces are provided adjacent the peripheral portion of the waveguide between pairs of the point light sources. The diffusive reflective surfaces are oriented relative to the series of point light sources and the waveguide so as to introduce light into regions of the waveguide between pairs of the point light sources, such that the peripheral portion of the waveguide is substantially uniformly illuminated. Preferably, the diffusive reflective surfaces comprise a series of posts mounted in spaced relationship adjacent the peripheral portion of the waveguide. In the preferred embodiment, the point light

1:45-55

Such air gap provides a low index substance (i.e., air) along the bottom surface 92 to enhance the waveguiding function of the guide 46. The bottom surface 92 follows a geometric contour that redirects light propagating in the waveguide between the top surface 90 and the bottom surface 92, so that more of the light exits the center portion of the waveguide, thereby providing more uniform illumination from the top surface 90 of the waveguide 46.

5:1-8

having a wavelength in the range of 400 nm to 700 nm. The portion of the diffusive reflective top surface 57 between the diffusive reflective surfaces 65, together with the diffusive reflective interior surface of the top wall 85 of the frame 80, and the diffusive reflective side surfaces 65 of the guide members 60 form a series of diffusive reflective air filled cavities that confine the emitted light and inject it into the side surfaces 94 of the waveguide 46. Advantageously, the guide members 60 facilitate a uniform distribution of light from the point light sources into a peripheral portion (FIG. 13) of the waveguide 46, adjacent to the cavities.

7:3-15

**INTRINSIC EVIDENCE FOR DISPUTED TERM “WHEREBY LIGHT IS INJECTED FROM SAID EXIT MOUTHS INTO A PERIPHERAL PORTION OF SAID OPTICAL CAVITY”:**

A further aspect of the invention comprises an illumination device utilizing an optical cavity having an output aperture and a series of diffusive reflective optical cavities, each substantially smaller than the aforesaid optical cavity. The series of optical cavities have exit mouths disposed along a side of the aforesaid optical cavity. A series of point sources of light are mounted to emit light into the series of optical cavities, respectively, whereby light is injected from the exit mouth into a peripheral portion of the optical cavity.

2:1-9

With reference to FIGS. 3 and 4, the guide members 60 are spaced apart along the side edges 62 so as to define a plurality of spaces 70 between adjacent guide members 60. Each of the spaces 70 is substantially funnel-shaped so as to form a relatively narrow entry mouth 71 adjacent the side edges 62. The spaces 70 gradually widen in size moving from the entry mouths 71 toward the apexes 66 of the guide members 60 to thereby form an exit mouth between the apexes 66 adjacent the boundary of the waveguide receiving section. The exit mouths are wider than the entry mouths 71. Moreover, the entry mouths 71 of the spaces 70 are preferably each configured to receive light from one of the LEDs 50 which are mounted adjacent thereto, as described more fully below.

4:10-23

**EXHIBIT 27**  
**U.S. PATENT NO. 6,134,092**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 5**

5. The device of claim 1, wherein the series of point light sources comprise light-emitting diodes mounted on an electrical-conductive strip of material.

**ASSERTED CLAIM 12**

12. An illumination device, comprising:  
a series of diffusive reflective optical cavities formed by diffusive reflective surfaces, each of said cavities having an entry mouth sized to receive a point light source and an exit mouth;  
a point light source mounted at each of the entry mouths;  
a pair of surfaces forming a waveguide, said waveguide having a peripheral portion extending along the exit mouths of said diffusive reflective optical cavities.

**LGD's Claim Construction**

**light-emitting diodes mounted on an electrical-conductive strip of material-** components, each containing a semiconductor diode chip as part of their structure, that provide the desired light that illuminates the waveguide or optical cavity and that are attached to a strip of material that provides electrical signals to the components

**mouth-** an optical opening through which light passes

<sup>1</sup> Disputed Term "light-emitting diodes mounted on an electrical-conductive strip of material" also appears in asserted claim 20 in the same context.

<sup>2</sup> Disputed Term "mouth" also appears in asserted claim 12,16,17 and 21 in the same context.

**INTRINSIC EVIDENCE FOR DISPUTED TERM “LIGHT-EMITTING DIODES MOUNTED ON AN ELECTRICAL-CONDUCTIVE STRIP OF MATERIAL”:**

are configured to inject light into the waveguide 46, as described in more detail below. In the illustrated embodiment, each of a pair of LED strips 51, such as printed circuit boards or electrical-conductive strips, mount the LEDs 50 in a linear array with equidistant spacing. The LEDs 50 within a strip 51 are parallel connected and the two strips 51 are series connected to one another via an electrical conductor 54. The various components of the illumination device 50 are mechanically coupled to one another, as described more fully below with reference to FIGS. 11 and 12.

3:22-31

**INTRINSIC EVIDENCE FOR DISPUTED TERM “MOUTH”:**

In accordance with another aspect of the invention, a series of diffusive reflective optical cavities are formed by diffusive reflective surfaces. Each of the cavities has an entry mouth sized to receive a point light source and an exit mouth. A point light source is mounted at each of the entry mouths. A peripheral portion of a waveguide extends along the exit mouth of the diffusive reflective optical cavity.

1:61-67

With reference to FIGS. 3 and 4, the guide members 60 are spaced apart along the side edges 62 so as to define a plurality of spaces 70 between adjacent guide members 60. Each of the spaces 70 is substantially funnel-shaped so as to form a relatively narrow entry mouth 71 adjacent the side edges 62. The spaces 70 gradually widen in size moving from the entry mouths 71 toward the apexes 66 of the guide members 60 to thereby form an exit mouth between the apexes 66 adjacent the boundary of the waveguide receiving section. The exit mouths are wider than the entry mouths 71. Moreover, the entry mouths 71 of the spaces 70 are preferably each configured to receive light from one of the LEDs 50 which are mounted adjacent thereto, as described more fully below.

4:10-23

With reference to FIGS. 11 and 12, an LED strip 51 is positioned between each of the side edges 62 of the light guide 44 and each of the side walls 98 of the heat sink 44. The LED strips 51 are preferably oriented so that an LED 50 is disposed at each of the mouths 71 of the spaces 70 between the guide members 60. The bent side walls 98 of the heat sink 42 causes the convex portions 104 (FIG. 10) of the side walls 98 to exert pressure against the LED strips 51 to thereby maintain a strong mechanical contact between the heat sink 42 and the LED strips 51. This facilitates the

6:45-54

**EXHIBIT 27**  
**U.S. PATENT NO. 6,134,092**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 21**

**21.** An illumination device, comprising:  
an optical cavity formed by diffusive reflective surfaces, said cavity having an output region through which light exits said cavity;  
a plurality of guide members formed by diffusive reflective surfaces, the **guide members positioned along a periphery of the optical cavity** such that spaces are defined between each of the guide members, each of the spaces having an entry mouth spaced from the periphery of the optical cavity and an exit mouth wider than the entry mouth and adjacent the periphery of the optical cavity; and  
a light source mounted at the entry mouths of each of the spaces between the guide members.

**LGD's Claim Construction**

**guide members positioned along a periphery of the optical cavity** - separate structures, unattached from one another, each adjacent a side edge of the optical cavity

**INTRINSIC EVIDENCE FOR DISPUTED TERM “GUIDE MEMBERS  
POSITIONED ALONG A PERIPHERY OF THE OPTICAL CAVITY”:**

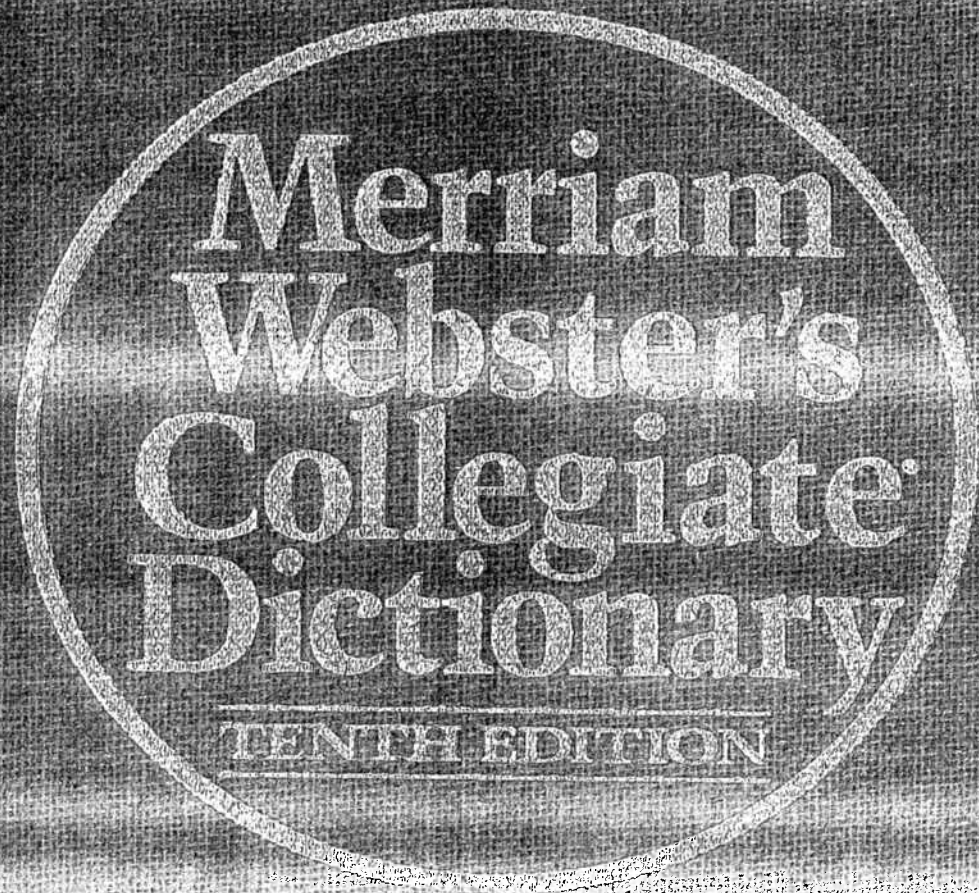
With reference to the exploded view of FIG. 2, the illumination device 40 comprises a plurality of components, including a heat sink 42, a light guide 44, a waveguide 46, a cover 48, and a film stack 49. A plurality of point light sources, such as light-emitting diodes (LEDs) 50, are positioned adjacent the peripheral edges of the light guide 44 and are configured to inject light into the waveguide 46, as described in more detail below. In the illustrated

3:14-22

In operation, the LEDs 50 are energized to introduce light into the waveguide 46. Preferably, the LEDs emit light having a wavelength in the range of 400 nm to 700 nm. The portion of the diffusive reflective top surface 57 between the diffusive reflective surfaces 65, together with the diffusive reflective interior surface of the top wall 85 of the frame 80, and the diffusive reflective side surfaces 65 of the guide members 60 form a series of diffusive reflective air filled cavities that confine the emitted light and inject it into the side surfaces 94 of the waveguide 46. Advantageously, the guide members 60 facilitate a uniform distribution of light from the point light sources into a peripheral portion (FIG. 13) of the waveguide 46, adjacent to the cavities.

7:3-15

# **EXHIBIT L-29(a)**





# Merriam- Webster's Collegiate® Dictionary

TENTH EDITION

Merriam-Webster, Incorporated  
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Library of Congress Cataloging in Publication Data  
Main entry under title:

Merriam-Webster's collegiate dictionary. — 10th ed.

p. cm.

ISBN 0-87779-708-0 (unindexed). — ISBN 0-87779-709-9 (indexed).

— ISBN 0-87779-710-2 (deluxe). — ISBN 0-87779-707-2 (laminated cover).

1. English language—Dictionaries.

PE1628.M36 1994

423—dc20

93-32603

CIP

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tered in the form of its crystalline citrate  $C_{10}H_{21}N_3O_7 \cdot C_6H_8O_7$ , esp. to control human filariasis and large roundworms in dogs and cats

**di-eth-yl ether** \di-ē-thāl-ē n (ca. 1930): ETHER 3a

**di-eth-yl-stil-bes-trol** \stil-ē-bes-trōl, -trōl n [ISV] (1938): a colorless crystalline synthetic compound  $C_{18}H_{20}O_2$  used as a potent estrogen but contraindicated in pregnancy for its tendency to cause cancer or birth defects in offspring — called also *stilbestrol*

**di-eth-yl zinc** n (1952): a volatile pyrophoric liquid organometallic compound  $C_4H_{10}Zn$  used esp. to catalyze polymerization reactions and to deacidify paper

**di-e-ti-tian** or **di-e-ti-cian** \di-ē-ti-shən n [dietitian irreg. fr. *diet* + *-ician*] (ca. 1846): a specialist in dietetics

**dif-fer** \di-far-ē vi **dif-fered**; **dif-fer-ing** \f(-ə-rin) [ME, fr. MF or L; MF *differre* to postpone, be different, fr. L *differre*, fr. *dis-* + *ferre* to carry — more at BEAR] (14c) 1 a: to be unlike or distinct in nature, form, or characteristics (the law of one state ~s from that of another) b: to change from time to time or from one instance to another: VARY (the number of cookies in a box may ~) 2: to be of unlike or opposite opinion: DISAGREE (they ~ on religious matters)

**dif-fer-ence** \di-fərn(t)s, -di-fə-rən(t)s n (14c) 1 a: the quality or state of being different b: an instance of differing in nature, form, or quality c *archaic*: a characteristic that distinguishes one from another or from the average d: the element or factor that separates or distinguishes contrasting situations 2: distinction or discrimination in preference 3 a: disagreement in opinion: DISSENSION b: an instance or cause of disagreement 4: the degree or amount by which things differ in quantity or measure; *specif*: REMAINDER 2b(1) 5: a significant change in or effect on a situation

**difference** vt -enced; -enc-ing (1576): DIFFERENTIATE, DISTINGUISH

**dif-fer-ent** \di-fərn(t), -di-fə-rən(t) adj [MF, fr. L *different-*, *differens*, prp. of *differre*] (14c) 1: partly or totally unlike in nature, form, or quality: DISSIMILAR (could hardly be more ~) — often followed by *from*, *than*, or chiefly Brit. to (small, neat hand, very ~ from the captain's tottery characters — R. L. Stevenson) (vastly ~ in size than it was twenty-five years ago — N. M. Pusey) (a very ~ situation to the ... one under which we live — Sir Winston Churchill) 2: not the same: as a: DISTINCT (~ age groups) b: VARIOUS (~ members of the class) c: ANOTHER (~switched to a ~ TV program) 3: UNUSUAL, SPECIAL (she was ~ and superior) — **dif-fer-ent-ness** n

*syn* DIFFERENT, DIVERSE, DIVERGENT, DISPARATE, VARIOUS mean unlike in kind or character. DIFFERENT may imply little more than separateness but it may also imply contrast or contrariness (~different foods). DIVERSE implies both distinctness and marked contrast (such diverse interests as dancing and football). DIVERGENT implies movement away from each other and unlikelihood of ultimate meeting or reconciliation (went on to pursue divergent careers). DISPARATE emphasizes incongruity or incompatibility (disparate notions of freedom). VARIOUS stresses the number of sorts or kinds (tried various methods).

*usage* Numerous commentators have condemned *different* than in spite of its use since the 17th century by many of the best-known names in English literature. It is nevertheless standard and is even recommended in many handbooks when followed by a clause. *Different from*, the generally safe choice, is more common and is even used in constructions where *than* would work more smoothly.

**different** adv (1744): DIFFERENTLY

**dif-fer-en-tial** \di-fə-rən(t)-sh(ē)-əl n, pl -ti-ae \-shē-ē, -shē-ā [L, *difference*, fr. *different-*, *different*] (1690): an element, feature, or factor that distinguishes one entity, state, or class from another; esp.: a characteristic trait distinguishing a species from other species of the same genus

**dif-fer-en-tial** \di-fə-rən(t)-shāl adj (1647) 1 a: of, relating to, or constituting a difference: DISTINGUISHING b: making a distinction between individuals or classes c: based on or resulting from a differential d: functioning or proceeding differently or at a different rate 2: being, relating to, or involving a differential or differentiation 3 a: relating to quantitative differences b: producing effects by reason of quantitative differences — **dif-fer-en-tial-ly** \-rən(t)-shāl-ē adv

**differential** n (1704) 1 a: the product of the derivative of a function of one variable by the increment of the independent variable b: a sum of products in which each product consists of a partial derivative of a given function of several variables multiplied by the corresponding increment and which contains as many products as there are independent variables in the function 2: a difference between comparable individuals or classes (a price ~); also: the amount of such a difference 3 a: DIFFERENTIAL GEAR b: a case covering a differential gear

**differential calculus** n (1702): a branch of mathematics concerned chiefly with the study of the rate of change of functions with respect to their variables esp. through the use of derivatives and differentials

**differential equation** n (1763): an equation containing differentials or derivatives of functions — compare PARTIAL DIFFERENTIAL EQUATION

**differential gear** n (ca. 1859): an arrangement of gears forming an epicyclic train for connecting two shafts or axles in the same line, dividing the driving force equally between them, and permitting one shaft to revolve faster than the other — called also *differential gearing*

**differential geometry** n (ca. 1909): a branch of mathematics using calculus to study the geometric properties of curves and surfaces

**dif-fer-en-ti-ate** \di-fə-rən(t)-shē-āt vb -at-ed; -at-ing vt (1816) 1: to obtain the mathematical derivative of 2: to mark or show a difference in: constitute a difference that distinguishes 3: to develop differential characteristics in 4: to cause differentiation of in the course of development 5: to express the specific distinguishing quality of: DISCRIMINATE ~ vi 1: to recognize or give expression to a difference 2: to become distinct or different in character 3: to undergo differentiation — **dif-fer-en-ti-a-bil-ity** \-rən(t)-sh(ē)-ə-bi-lə-tē n — **dif-fer-en-ti-a-ble** \-rən(t)-sh(ē)-ə-bəl adj

**dif-fer-en-ti-a-tion** \-rən(t)-shē-ā-shən n (1802) 1: the act or process of differentiating 2: development from the one to the many, the simple to the complex, or the homogeneous to the heterogeneous 3 a: modification of body parts for performance of particular functions b: the sum of the processes whereby apparently indifferent cells, tissues, and structures attain their adult form and function 4: the processes by which various rock types are produced from a common magma

**dif-fer-ent-ly** \di-fərn(t)-lē, -di-fə-rən(t)-lē adv (14c) 1: in a different manner 2: OTHERWISE

**dif-fi-cile** \dē-fi-'sē(ə)\ adj [F, lit., difficult] (1536): STUBBORN, UNREASONABLE

**dif-fi-cult** \di-fi-(k)kəlt adj [ME, back-formation fr. *difficulty*] (14c) 1: hard to do, make, or carry out: ARDUOUS (a ~ climb) 2 a: hard to deal with, manage, or overcome (a ~ child) b: hard to understand: PUZZLING (~ reading) *syn* see HARD — **dif-fi-cult-ly** adv

**dif-fi-cul-ty** \-(k)kəlt-ē n, pl -ties [ME *difficultas*, fr. L *difficultas*, fr. *difficilis* not easy, fr. *dis-* + *facilis* easy — more at FACILE] (14c) 1: the quality or state of being difficult 2: CONTROVERSY, DISAGREEMENT 3: OBJECTION 4: something difficult: IMPEDIMENT 5: EMBARRASSMENT, TROUBLE — usu. used in pl.

**dif-fi-dence** \di-fə-dən(t)s, -fə-den(t)s n (14c): the quality or state of being diffident

**dif-fi-dent** \-dənt, -dənt adj [ME, fr. L *diffident-*, *diffidens*, prp. of *diffidere* to distrust, fr. *dis-* + *fidere* to trust — more at BIDE] (15c) 1: hesitant in acting or speaking through lack of self-confidence 2 *archaic*: DISTRUSTFUL 3: RESERVED, UNASSERTIVE *syn* see SHY — **dif-fi-dent-ly** adv

**dif-fract** \di-'frakt\ vt [back-formation fr. *diffraction*] (1803): to cause to undergo diffraction

**dif-frac-tion** \di-'frak-shən n [NL *diffraction-*, *diffraction*, fr. L *diffingere* to break apart, fr. *dis-* + *frangere* to break — more at BREAK] (1671): a modification which light undergoes in passing by the edges of opaque bodies or through narrow slits or in being reflected from ruled surfaces and in which the rays appear to be deflected and to produce fringes of parallel light and dark or colored bands; also: a similar modification of other waves (as sound waves)

**diffraction grating** n (1867): GRATING 3

**dif-frac-tom-e-ter** \di-'frak-tā-mō-tər n (ca. 1909): an instrument for analyzing the structure of a usu. crystalline substance from the scattering pattern produced when a beam of radiation or particles (as X rays or neutrons) strikes it — **dif-frac-to-met-ric** \di-'frak-tā-'me-trik\ adj — **dif-frac-tom-e-try** \di-'frak-tā-mō-trē n

**dif-fuse** \di-'fyūs\ adj [ME, fr. L *diffusus*, pp. of *diffundere* to spread out, fr. *dis-* + *fundere* to pour — more at FOUND] (15c) 1: being at once verbose and ill-organized 2: not concentrated or localized (~ sclerosis) *syn* see WORDY — **dif-fuse-ly** adv — **dif-fuse-ness** n

**dif-fuse** \di-'fyüz\ vb **dif-fused**; **dif-fus-ing** [ME *diffused*, pp., fr. L *diffusus*, pp.] vt (14c) 1 a: to pour out and permit or cause to spread freely b: EXTEND, SCATTER c: to spread thinly or wastefully 2: to subject to diffusion; esp.: to break up and distribute (incident light) by reflection ~ vi 1: to spread out or become transmitted esp. by contact 2: to undergo diffusion — **dif-fus-ible** \di-'fyüz-ə-bəl\ adj

**dif-fuse-po-rous** \di-'fyūs-'pōr-əs, -'pōr-ə\ adj ['diffuse] (ca. 1902): having vessels more or less evenly distributed throughout an annual ring and not varying greatly in size — compare RING-POROUS

**dif-fu-ser** \di-'fyü-zər n (ca. 1679) 1: one that diffuses: as a: a device (as a reflector) for distributing the light of a lamp evenly b: a screen (as of cloth or frosted glass) for softening lighting (as in photography) c: a device (as slats at different angles) for deflecting air from an outlet in various directions 2: a device for reducing the velocity and increasing the static pressure of a fluid passing through a system

**dif-fu-sion** \di-'fyü-zhən n (14c) 1: the action of diffusing: the state of being diffused 2: PROLIXITY, DIFFUSINESS 3 a: the process whereby particles of liquids, gases, or solids intermingle as the result of their spontaneous movement caused by thermal agitation and in dissolved substances move from a region of higher to one of lower concentration b (1): reflection of light by a rough reflecting surface (2): transmission of light through a translucent material: SCATTERING 4: the spread of cultural elements from one area or group of people to others by contact 5: the softening of sharp outlines in a photographic image — **dif-fu-sion-al** \-fyü-zhə-nəl\ adj

**dif-fu-sion-ist** \-fyü-zhə-nəst n (1938): an anthropologist who emphasizes the role of diffusion in the history of culture rather than independent invention or discovery — **dif-fu-sion-ism** \-fyü-zhə-ni-zəm\ n — **diffusionist** adj

**dif-fu-sive** \di-'fyü-siv, -ziv\ adj (1614): tending to diffuse: characterized by diffusion (~ motion of atoms) — **dif-fu-sive-ly** adv — **dif-fu-sive-ness** n — **dif-fu-siv-ity** \di-'fyü-'si-və-tē, -'zi-ē n

**di-func-tion-al** \di-fan(k)-shənəl, -shə-nəl\ adj (1943): of, relating to, or being a compound with two highly reactive sites in each molecule

**dig** \dig\ vb **dug** \dæg\; **dig-ging** [ME *diggen*] vt (13c) 1 a: to break up, turn, or loosen (earth) with an implement b: to prepare the soil of (~ a garden) 2 a: to bring to the surface by digging: UN-EARTH b: to bring to light or out of hiding (~ up facts) 3: to hollow out or form by removing earth: EXCAVATE 4: to drive down so as to penetrate: THRUST 5: POKE, PROD 6 a: to pay attention to: NOTICE (~ that fancy hat) b: UNDERSTAND, APPRECIATE (if you ... do something subtle ... only one tenth of the audience will ~ it — Nat Hentoff) c: LIKE, ADMIRE (high school students ~ short poetry — David Burmester) ~ vi 1: to turn up, loosen, or remove earth: DELVE 2: to work hard or laboriously 3: to advance by or as if by removing or pushing aside material

**dig** n (1819) 1 a: THRUST, POKE b: a cutting remark 2 pl a: living accommodations b: chiefly Brit.: LODGING, HOTEL 3: an archaeological excavation site; also: the excavation itself

**dig-a-my** \di-gə-mē n, pl -mies [LL *digamia*, fr. LGk, fr. Gk *digamos* married to two people, fr. *di-* + *-gamos* -gamous] (1635): a second marriage after the termination of the first

**di-gas-tric** \di-'gas-trik\ adj [NL *gastricus*, fr. *di-* + *gastricus* gastric] (ca. 1721): of, relating to, or being a muscle with two bellies separated by a median tendon

**di-ge-net-ic** \di-jə-'ne-tik\ adj [NL *Digenetica*, subclass name (syn. of *Digena*), fr. *di-* + *genetica*, neut. pl. of *geneticus* genetic] (ca. 1883): of or relating to a subclass (*Digena*) of trematode worms in which sexual reproduction as an internal parasite of a vertebrate alternates with asexual reproduction in a mollusk

\ə\ about \ə\ kitten, F table \ər\ further \ə\ ash \ā\ ace \ā\ mop, mar  
 \a\ out \ch\ chin \e\ bet \ē\ easy \g\ go \i\ hit \ī\ ice \j\ job  
 \j\ sing \ō\ go \ō\ law \oi\ boy \th\ thin \th\ the \ü\ loot \ū\ foot  
 \y\ yet \zh\ vision \ā, k, ŋ, æ, œ, ʉ, ū, see Guide to Pronunciation

# **EXHIBIT L-30**

**Ex. L-30**  
**CMO US PATENT NO. 6,013,923**

**INDEX OF DISPUTED TERMS**

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**EXHIBIT L-30**  
**U.S. PATENT NO. 6,013,923**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 1**

**1. A method of inhibiting electrostatic discharge damage to an array of semiconductor switches formed on a common substrate and arranged in rows and columns, individual ones of one of the rows or columns of said array being interconnected by source lines and individual ones of the other of the rows or columns of said array being interconnected by gate lines, said method comprising the steps of:**

**during formation of said gate lines, connecting one end of each gate line directly to a shorting element and another end of each gate line to a shorting element via a protection element;**

**during formation of said source lines, connecting one end of each source line directly to a shorting element and connecting another end of each source line to a shorting element via a protection element; and electrically coupling said shorting elements.**

**LGD's Claim Construction**

**shorting element<sup>1</sup>** – a pattern of conductive material for electrically connecting, with low resistance, the gate lines to each other or the source lines to each other

**protection element<sup>2</sup>** - a circuit component designed to protect against electrostatic discharge and to allow for testing

**electrically coupling said shorting elements<sup>3</sup>** - electrically connecting the shorting elements without intervening protection elements

**during formation of said gate lines** - at the same time when the electrically conductive material that forms the gate lines is deposited and etched

**during formation of said source lines** - at the same time when the electrically conductive material that forms the source lines is deposited and etched

<sup>1</sup> Disputed Term "shorting element" also appears in asserted claims 2, 5, 8, and 11 in the same context.

<sup>2</sup> Disputed Term "protection element" also appears in asserted claims 3, 6, 10, and 12 in the same context.

<sup>3</sup> Disputed Term "electrically coupling said shorting elements" also appears in asserted claims 2 and 8 in the same context.

**INTRINSIC EVIDENCE FOR DISPUTED TERM “SHORTING ELEMENT”:**

parasitic capacitance in the TFT switches decrease ESD immunity.

One common ESD damage protection circuit used with TFT switch arrays makes use of closed shorting bars surrounding the TFT switch array to link all of the source lines and the gate lines of the TFT switch array together. The

1:53-58

The prior art ESD protection circuits referred to above all have some common drawbacks. Firstly, none of the ESD protection circuits protect the TFT switch array from the first manufacturing stage (usually gate line formation) to the last manufacturing stage (usually wire bonding). During the manufacture of TFT switch arrays for liquid crystal displays,

3:6-11

These processes are often performed prior to the completion of the TFT switch array structure. Isolating the gate lines before finishing source line metallization as suggested in the prior art may result in the build up of electrostatic charge on the gate lines. Electrostatic charges on the gate lines may become buried under the dielectric film forming the gate insulating layer and incubate until later stages in the manufacturing process. During these later stages, the buried

3:15-22

embodiments, it is preferred that the protection elements are in the form of resistive protection elements.

The present invention provides advantages in that the ESD damage protection is maintained throughout the entire manufacturing and testing process of the semiconductor switch array and is fully compatible with conventional semiconductor switch array fabrication processes.

4:25-31

**INTRINSIC EVIDENCE FOR DISPUTED TERM “SHORTING ELEMENT” (cont’d):**

The ESD damage protection circuit 50 includes a first shorting element in the form of a ring 52 surrounding the TFT switch array and interconnecting all of the gate lines 24 of the TFT switch array 21. Specifically, the shorting ring 52 is connected directly to the wire bonding pads 48 on one side of the TFT switch array 21.

A second shorting element in the form of a ring 56 also surrounds the TFT switch array and interconnects all of the source lines 26 of the TFT switch array 21. The second shorting ring 56 is connected directly to the wire bonding

5:41-51

As can be seen, the ESD damage protection circuit 150 includes a shorting ring 152 interconnecting all of the gate lines 124 of the TFT switch array 121. The shorting ring 152 is connected to only one end of each gate line 124 through wire bonding pads 148. The connections between the shorting ring 152 and the wire bonding pads 148 alternate between opposite sides of the TFT switch array. Shorting ring 152 also interconnects all of the source lines 126 of the TFT switch array through vias formed in the TFT switch array structure. The shorting ring 152 is connected to only one end of each source line 126 through wire bonding pads 146. The connections between the shorting ring 152 and the wire bonding pads 146 also alternate between opposite sides of the TFT switch array 121.

A second shorting ring 156 is connected to the other end of each gate line 124 via resistive protection elements 154. Shorting ring 156 is also connected to the other end of each

7:1-17

As one of skill in the art will appreciate, the ESD damage protection circuits are present from the first manufacturing stage of the TFT switch array (gate line formation) right through to testing and connection of the TFT switch array to peripheral circuits. Because of this, the likelihood of ESD damage occurring to the TFT switch array is reduced as

7:49-54

## **INTRINSIC EVIDENCE FOR DISPUTED TERM "PROTECTION ELEMENT":**

embodiments, it is preferred that the protection elements are in the form of resistive protection elements.

The present invention provides advantages in that the ESD damage protection is maintained throughout the entire manufacturing and testing process of the semiconductor switch array and is fully compatible with conventional semiconductor switch array fabrication processes.

4:25-31

source lines 26 for testing or for wire bonding purposes. Similarly, wire bonding pads 48 are formed at the ends of the gate lines 24. As mentioned previously, during fabrication of the TFT switch array 21, during its testing or when connecting peripheral circuits to the TFT switch array 21 such as gate driver 28 and charge amplifiers 30, ESD damage to the TFT switch array may occur. To reduce the occurrence of ESD damage during fabrication of the TFT switch array 21, an ESD damage protection circuit 50 is also fabricated on the glass substrate as will now be described.

5:32-41

FIG. 1A to expose the wire bonding pads 48 and 49 connected to the source and gate lines extending from one side of the TFT switch array permitting the individual TFT switches 38 in the array to be tested. These scribe lines are marked so that part of each shorting ring 52, 56 remains intact keeping the gate and source lines 24 and 26 interconnected through the resistive protection elements 54 and 58 during the testing stage. If electrostatic charges appear on the gate or source lines resulting in any unbalanced potentials across the dielectric film constituting the gate insulating layer of the TFT switch array, the electrostatic charges will disperse quickly through the resistive protection elements connected to the gate and source lines.

6:22-35

Similar to the previous embodiment, the scribe lines are marked so that after cutting, one end of each of the gate and source lines 124 and 126 remains connected to shorting ring 156 via resistive protection elements 154 and 158 respectively.

Once testing has been completed, the peripheral circuits can be connected to the exposed wire bonding pads 146 and 148 on opposite sides of the TFT switch array 121. After this, the connections between the gate and source lines and the shorting ring 156 can be severed using a programmable laser cutting machine programmed to jump over the gate and source lines 124 and 126 connected to peripheral circuits.

7:34-48

**INTRINSIC EVIDENCE FOR DISPUTED TERM “ELECTRICALLY COUPLING SAID SHORTAGE ELEMENTS”:**

time the gate lines are formed while the shorting bar associated with the source lines is formed at the time the source lines are formed. The two shorting bars are electrically connected through vias formed in the TFT switch array structure. Because the shorting bars connect the gate and

1:60-64

concentrate at a few points or boundary lines causing a breakdown in the dielectric gate insulating layer.

In addition, in some instances since the gate and source lines are interconnected by protection elements, a failure in the connection between a gate or source line and a protection element will result in the gate or source line being isolated from the common electrode.

3:24-30

58. Shorting ring 56 is also connected to each of the wire bonding pads 48 on the other side of the TFT switch array 21 through a resistive protection element 54. The two shorting rings 52 and 56 are electrically connected through vias (not shown) formed in the TFT switch array structure. The resistive protection elements 54, 58 provide current paths for leaking electrostatic charges collected by the gate and source lines 24 and 26 and have resistances at least one order of magnitude greater than the impedance of the gate and source lines.

5:55-64

Shorting ring 156 is also connected to the other end of each source line 126 via resistive protection elements 158. The shorting rings 152 and 156 are electrically connected through vias 160 and 162 formed at the corners of the TFT switch array structure (see FIGS. 7 and 8).

7:17-21

2. The method of claim 1 further comprising the steps of connecting said one and another ends of each of said source lines to a first shorting element, connecting said one end of each of said gate lines to a second shorting element and said another end of each of said gate lines to said first shorting element and electrically coupling said first and second shorting elements.

Claim 2

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DURING FORMATION OF SAID GATE”:**

rounding the TFT switch array to link all of the source lines and the gate lines of the TFT switch array together. The shorting bar associated with the gate lines is formed at the time the gate lines are formed while the shorting bar associated with the source lines is formed at the time the source lines are formed. The two shorting bars are electrically connected through vias formed in the TFT switch array

1:56-63

The prior art ESD protection circuits referred to above all have some common drawbacks. Firstly, none of the ESD protection circuits protect the TFT switch array from the first manufacturing stage (usually gate line formation) to the last manufacturing stage (usually wire bonding). During the manufacture of TFT switch arrays for liquid crystal displays,

3:6-11

These processes are often performed prior to the completion of the TFT switch array structure. Isolating the gate lines before finishing source line metallization as suggested in the prior art may result in the build up of electrostatic charge on the gate lines. Electrostatic charges on the gate lines may become buried under the dielectric film forming the gate insulating layer and incubate until later stages in the manufacturing process. During these later stages, the buried

3:15-22

as for example, TFT switches, TFD's (thin film diodes), zener diodes or photodiodes.

As one of skill in the art will appreciate, the shorting ring 52 is formed when the gate lines 24 are being formed on the substrate of the TFT switch array structure. The shorting ring 56 is formed when the source lines 26 are being formed on the substrate.

6:12-18

As one of skill in the art will appreciate, the ESD damage protection circuits are present from the first manufacturing stage of the TFT switch array (gate line formation) right through to testing and connection of the TFT switch array to peripheral circuits. Because of this, the likelihood of ESD damage occurring to the TFT switch array is reduced as

7:49-54

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DURING FORMATION OF SAID SOURCE”:**

rounding the TFT switch array to link all of the source lines and the gate lines of the TFT switch array together. The shorting bar associated with the gate lines is formed at the time the gate lines are formed while the shorting bar associated with the source lines is formed at the time the source lines are formed. The two shorting bars are electrically connected through vias formed in the TFT switch array

1:56-63

These processes are often performed prior to the completion of the TFT switch array structure. Isolating the gate lines before finishing source line metallization as suggested in the prior art may result in the build up of electrostatic charge on the gate lines. Electrostatic charges on the gate lines may become buried under the dielectric film forming the gate insulating layer and incubate until later stages in the manufacturing process. During these later stages, the buried

3:15-22

as for example, TFT switches, TFD's (thin film diodes), zener diodes or photodiodes.

As one of skill in the art will appreciate, the shorting ring 52 is formed when the gate lines 24 are being formed on the substrate of the TFT switch array structure. The shorting ring 56 is formed when the source lines 26 are being formed on the substrate.

6:12-18

**EXHIBIT 28**  
**U.S. PATENT NO. 6,013,923**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 1**

**1.** A method of inhibiting electrostatic discharge damage to an array of semiconductor switches formed on a common substrate and arranged in rows and columns, individual ones of one of the rows or columns of said array being interconnected by source lines and individual ones of the other of the rows or columns of said array being interconnected by gate lines, said method comprising the steps of:

during formation of said gate lines, connecting one end of each gate line directly to a shorting element and another end of each gate line to a shorting element via a protection element;

during formation of said source lines, connecting one end of each source line directly to a shorting element and connecting another end of each source line to a shorting element via a protection element; and electrically coupling said shorting elements.

**LGD's Claim Construction**

**source line<sup>4</sup>** - a pattern of electrically conductive material that conveys data signals to transistors within the TFT array

**gate line<sup>5</sup>** - a pattern of electrically conductive material that conveys gate signals to transistors within the TFT array

<sup>4</sup> Disputed Term "source lines" also appears in asserted claims 2, 4, 5, 6, 8, 9, 11, and 12 in the same context.

<sup>5</sup> Disputed Term "gate lines" also appears in asserted claim 2, 4, 5, 6, 8, 9, 11, and 12 in the same context.

**INTRINSIC EVIDENCE FOR DISPUTED TERM "SOURCE LINES":**

switch array 21 in the form of a plurality of pixels 22 arranged in rows and columns. Gate lines 24 interconnect the pixels 22 of each row while source lines 26 interconnect the pixels of each column. The gate lines 24 lead to a gate driver circuit 28 which provides pulses to the gate lines in

~

succession in response to input from a control circuit 29. The source lines 26 lead to charge amplifiers 30 which in turn are connected to an analog multiplexer 32. The analog multiplexer provides image output which can be digitized to

4:64 - 5:4

electrode 36. The pixel electrode 36 constitutes the drain electrode of a thin film transistor ("TFT") switch 38. The source electrode of TFT switch 38 is coupled to one of the source lines 26 while the gate electrode of the TFT switch is coupled to one of the gate lines 24.

5:10-14

ducer  $C_{SD}$  to radiation. Once charged, the charge can be read by supplying a gating pulse to the gate terminal of TFT switch 38. When the TFT switch receives the gate pulse, it connects the pixel electrode 36 to the source line 26 allowing

5:19-21

**INTRINSIC EVIDENCE FOR DISPUTED TERM "GATE LINE":**

the pixels 22 of each row while source lines 26 interconnect the pixels of each column. The gate lines 24 lead to a gate driver circuit 28 which provides pulses to the gate lines in

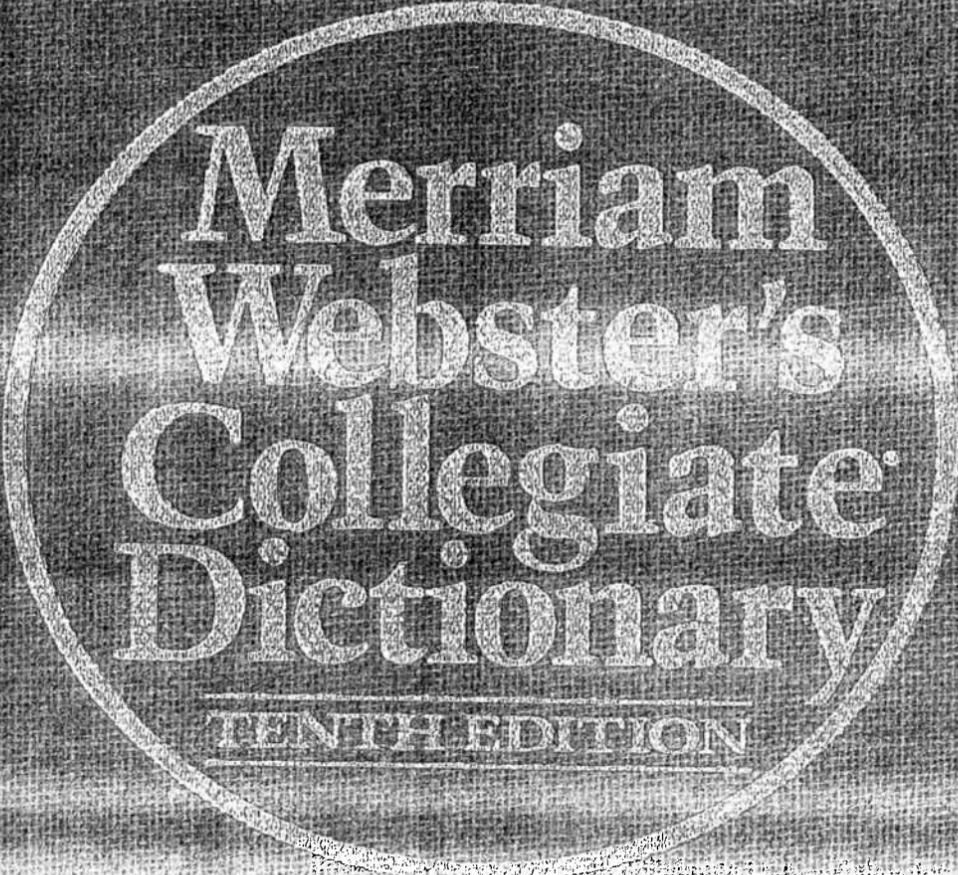
succession in response to input from a control circuit 29. The source lines 26 lead to charge amplifiers 30 which in turn are connected to an analog multiplexer 32. The analog multiplexer provides image output which can be digitized to create a digitized radiation image in response to input from the control circuit 29.

FIG. 2 shows an equivalent circuit of one of the pixels 22. As can be seen, the pixel 22 includes a radiation transducer CS, coupled to a storage capacitor  $C_{ST}$  in the form of a pixel electrode 36. The pixel electrode 36 constitutes the drain electrode of a thin film transistor ("TFT") switch 38. The source electrode of TFT switch 38 is coupled to one of the source lines 26 while the gate electrode of the TFT switch is coupled to one of the gate lines 24.

When the radiation transducer  $C_{SE}$  is biased and is exposed to radiation, it causes the pixel electrode to store a charge proportional to the exposure of the radiation transducer  $C_{SE}$  to radiation. Once charged, the charge can be read by supplying a gating pulse to the gate terminal of TFT switch 38. When the TFT switch receives the gate pulse, it connects the pixel electrode 36 to the source line 26 allowing

4:65 — 5:22

# **EXHIBIT L-31(a)**



Merriam  
Webster's  
Collegiate  
Dictionary  
TENTH EDITION

The image shows the front cover of the Merriam Webster's Collegiate Dictionary, Tenth Edition. The cover has a dark, textured background. In the center, there is a large, light-colored circular emblem. Inside this circle, the title "Merriam Webster's Collegiate Dictionary" is written in a serif font, with "Merriam" and "Webster's" on the first two lines, and "Collegiate Dictionary" on the third and fourth lines. Below the title, the words "TENTH EDITION" are written in a smaller, all-caps serif font, flanked by two horizontal lines. The overall appearance is that of a classic, authoritative reference work.



# Merriam- Webster's Collegiate® Dictionary

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Library of Congress Cataloging in Publication Data  
Main entry under title:

Merriam-Webster's collegiate dictionary. — 10th ed.

p. cm.

ISBN 0-87779-708-0 (unindexed). — ISBN 0-87779-709-9 (indexed).

— ISBN 0-87779-710-2 (deluxe). — ISBN 0-87779-707-2 (laminated cover).

1. English language—Dictionaries.

PE1628.M36 1994

423—dc20

93-32603

CIP

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the best buy 2: to make a search: HUNT ~ vt: to examine the stock or offerings of (the stores for Christmas gift ideas)

**shop-keep-er** \ˈshāp-ke-pər/ n (1530): STOREKEEPER 2

**shop-lift** \-lɪft/ vb [back-formation fr. *shoplifter*] vi (1820): to steal displayed goods from a store ~ vt: to steal (displayed goods) from a store

**shop-lift-er** \-lɪf-tər/ n (1680): one who shoplifts

**shop-per** \ˈshāp-pər/ n (1860) 1: one that shops 2: one whose occupation is shopping as an agent for customers or for an employer 3: a usu. free paper carrying advertising and sometimes local news

**shopping bag** n (1886): a bag (as of strong paper) that has handles and is intended for carrying purchases

**shopping center** n (1898): a group of retail stores and service establishments usu. with ample parking facilities and usu. designed to serve a community or neighborhood — called also *shopping plaza*

**shopping list** n (1913): a list of items to be purchased; broadly: a list of related items (the biggest possible *shopping list* of budget cuts — Leonard Silk)

**shopping mall** n (1959): MALL 3

**shop steward** n (1904): a union member elected as the union representative of a shop or department in dealings with the management

**shop-talk** \ˈshāp-tɔk/ n (1881): the jargon or subject matter peculiar to an occupation or a special area of interest

**shop-win-dow** \-wɪn-(-)dɔ/ n (15c): a display window of a store

**shop-worn** \-wɔrn, -wɔrn/ adj (1838) 1: faded, soiled, or otherwise impaired by remaining too long in a store 2: stale from excessive use or familiarity (~ clichés) 3: WORN-OUT (think of himself as a ~ Hollywood cynic — A. H. Johnston)

**shore** \ˈshɔr, ˈshɔr/ n, often attrib [ME, fr. (assumed) OE *scor*; akin to MLG *schor* foreland and perh. to OE *scieran* to cut — more at SHEAR] (14c) 1: the land bordering a usu. large body of water; specif: COAST 2: a boundary or the country or place that it bounds (hold him accountable for difficulties beyond our ~s that he could do nothing about — Dorothy Fosdick) 3: land as distinguished from the sea (shipboard and ~ duty)

**shore** vt shored; **shoring** [ME; akin to ON *skortha* to prop] (14c) 1: to support by a shore: PROP 2: to give support to: BRACE — usu. used with *up*

**shore** n (14c): a prop for preventing sinking or sagging

**shore-bird** \ˈshɔr-bɜrd, ˈshɔr-/ n (ca. 1672): any of a suborder (Charadrii) of birds (as a plover or snipe) that frequent the seashore

**shore dinner** n (1892): a dinner consisting chiefly of seafoods

**shore-front** \-frɒnt/ n (1919): land along a shore; specif: BEACH-FRONT

**shore leave** n (1888): a leave of absence to go on shore granted to a sailor or naval officer

**shore-line** \-lɪn/ n (1852) 1: the line where a body of water and the shore meet 2: the strip of land along the shoreline

**shore patrol** n (1917) 1: a branch of a navy that exercises guard and police functions — compare MILITARY POLICE 2: petty officers detailed to perform police duty while a ship is in port

**shore-side** \-sɪd/ adj (1883): situated at or near a shore

**shore-ward** \-wɜrd/ or **shore-wards** \-wɜrdz/ adv (ca. 1691): toward the shore

**shoring** \ˈshɔr-ɪŋ, ˈshɔr-/ n (15c) 1: the act of supporting with or as if with a prop 2: a system or group of shores

**shorn** past part of SHEAR

**short** \ˈshɔrt/ adj [ME, fr. OE *scort*; akin to OHG *scurz* short, ON *skortr* lack] (bef. 12c) 1 a: having little length b: not tall or high: LOW 2 a: not extended in time: BRIEF (a ~ vacation) b: not retentive (a ~ memory) c: EXPEDITIOUS, QUICK (made ~ work of the problem) d: seeming to pass quickly (made great progress in just a few ~ years) 3 a of a speech sound: having a relatively short duration b: being the member of a pair of similarly spelled vowel or vowel-containing sounds that is descended from a vowel that was short in duration but is no longer so and that does not necessarily have duration as its chief distinguishing feature (~ i in *sin*) c of a syllable in prosody (1): of relatively brief duration (2): UNSTRESSED 4: limited in distance (a ~ trip) 5 a: not coming up to a measure or requirement: INSUFFICIENT (in ~ supply) b: not reaching far enough (the throw to first was ~) c: enduring privation d: insufficiently supplied (~ of cash) (~ on brains) 6 a: ABRUPT, CURT b: quickly provoked 7: CHOPPY 8: payable at an early date 9 a: containing or cooked with shortening; also: FLAKY (~ pastry) b of metal: brittle under certain conditions 10 a: not lengthy or drawn out b: made briefer: ABBREVIATED 11 a: not having goods or property that one has sold in anticipation of a fall in prices b: consisting of or relating to a sale of securities or commodities that the seller does not possess or has not contracted for at the time of the sale (~ sale) 12: near the end of a tour of duty — **short-ish** \ˈshɔr-tɪʃ/ adj — in **short order**: with dispatch: QUICKLY

**short adv** (14c) 1: in a curt manner 2: for or during a brief time (*short-lasting*) 3: at a disadvantage: UNAWARES (caught ~) 4: in an abrupt manner: SUDDENLY (the car stopped ~) 5: at some point or degree before a goal or limit aimed at or under consideration (the shells fell ~) (quit a month ~ of graduation) 6: clean across (the axle was snapped ~) 7: by or as if by a short sale

**short n** (ca. 1586) 1: the sum and substance: UPSHOT 2 a: a short syllable b: a short sound or signal 3 pl a: a by-product of wheat milling that includes the germ, fine bran, and some flour b: refuse, clippings, or trimmings discarded in various manufacturing processes 4 a: knee-length or less than knee-length trousers — usu. used in pl. b pl: short drawers c: a size in clothing for short men 5 a: one who operates on the short side of the market b pl: short-term bonds 6 pl: DEFICIENCIES 7: SHORT CIRCUIT 8: SHORTSTOP 9 a: SHORT SUBJECT b: a brief story or article (as in a newspaper) — **for short**: as an abbreviation (named Katherine or Kate *for short*) — in **short**: by way of summary: BRIEFLY

**short vt** (1904) 1: SHORT-CIRCUIT 2: SHORTCHANGE, CHEAT

**short account** n (ca. 1902): the total of open short sales in a given subject of trade or in the market as a whole

**short-age** \ˈshɔr-tij/ n (1868): LACK, DEFICIT

**short ballot** n (1909): a ballot limiting the number of elective offices to the most important legislative and executive posts and leaving minor positions to be filled by appointment

**short-bread** \ˈshɔrt-bred/ n (1801): a thick cookie made of flour, sugar, and a large amount of shortening

**short-cake** \-kāk/ n (1594) 1: a crisp and often unsweetened biscuit or cookie 2 a: a dessert made typically of very short baking-powder-biscuit dough spread with sweetened fruit b: a dish consisting of a rich biscuit split and covered with a meat mixture

**short-change** \ˈchānj/ vt (1903) 1: to give less than the correct amount of change to 2: to deprive of or give less than something due: CHEAT — **short-changer** n

**short-circuit** vt (1867) 1: to apply a short circuit to or establish a short circuit in 2: BYPASS 3: FRUSTRATE, IMPEDE

**short circuit** n (1854): a connection of comparatively low resistance accidentally or intentionally made between points on a circuit between which the resistance is normally much greater

**short-coming** \ˈshɔrt-kə-mɪŋ, ˈshɔrt-/ n (15c): DEFICIENCY, DEFECT

**short-cut** \ˈshɔrt-kət also ˈkət/ n (1637) 1: a route more direct than the one ordinarily taken 2: a method of doing something more directly and quickly than and often not so thoroughly as by ordinary procedure

**shortcut** vb -cut; -cut-ting vt (1915): to shorten (as a route or procedure) by use of a shortcut; also: CIRCUMVENT ~ vi: to take or use a shortcut

**short-day** \ˈshɔrt-dā/ adj (1920): responding to or relating to a short photoperiod — used esp. of a plant; compare DAY-NEUTRAL, LONG-DAY

**short division** n (ca. 1890): mathematical division in which the successive steps are performed without writing out the remainders

**short-eared owl** \ˈshɔrt-ɪrd-/ n (1766): a medium-sized nearly cosmopolitan owl (*Asio flammeus*) that has very short ear tufts and usu. nests on the ground

**short-en** \ˈshɔr-tɪn/ vb **short-ened**; **short-en-ing** \ˈshɔrt-nɪŋ, ˈshɔr-tɪn-ɪŋ/ vt (14c) 1 a: to reduce the length or duration of b: to cause to seem short 2 a: to reduce in power or efficiency (is my hand ~ed, that it cannot redeem — Isa 50:2 (RSV)) b obs: to deprive of effect 3: to add fat to (as pastry dough) in order to make tender and flaky ~ vi: to become short or shorter — **short-en-er** \ˈshɔrt-nər, ˈshɔr-tɪn-ər/ n

**syn** SHORTEN, CURTAIL, ABBREVIATE, ABRIDGE, RETRENCH mean to reduce in extent. SHORTEN implies reduction in length or duration (*shorten a speech*). CURTAIL adds an implication of cutting that in some way deprives of completeness or adequacy (ceremonies *curtailed* because of rain). ABBREVIATE implies a making shorter usu. by omitting some part (using an *abbreviated title*). ABRIDGE implies a reduction in compass or scope with retention of essential elements and a relative completeness in the result (the *abridged* version of the novel). RETRENCH suggests a reduction in extent or costs of something felt to be excessive (declining business forced the company to *retrench*).

**short-en-ing** \ˈshɔrt-nɪŋ, ˈshɔr-tɪn-ɪŋ/ n (1538) 1: the action or process of making or becoming short; specif: the dropping of the latter part of a word so as to produce a new and shorter word of the same meaning 2: an edible fat used to shorten baked goods

**short-fall** \ˈshɔrt-fɔl/ n (1895): a failure to come up to expectation or need; also: the amount of such failure

**short-grass prairie** \ˈshɔrt-gras-/ n (1844): PRAIRIE 2b

**short-hair** \-hɑr, -her/ n (1903): a domestic cat with a short thick coat; esp: a member of any of several breeds of muscular medium- to large-sized cats with a short plushy coat — **short-haired** adj

**short-hand** \-hand/ n (1636) 1: a method of writing rapidly by substituting characters, abbreviations, or symbols for letters, sounds, words, or phrases: STENOGRAPHY 2: a system or instance of rapid or abbreviated communication or representation — **shorthand** adj

**short-handed** \ˈshɔrt-han-dəd/ adj (1794): having, working with, or done with fewer than the regular or necessary number of people

**short-haul** \ˈshɔrt-hɔl/ adj (1895): traveling or involving a short distance (~ flights)

**short-horn** \-hɔrn/ n, often cap (1847): any of a breed of red, roan, or white beef cattle originating in the north of England and including good milk-producing strains — called also *Durham*

**short-horned grasshopper** \ˈshɔrt-hɔrn(d)-/ n (ca. 1890): any of a family (Acrididae) of grasshoppers with short antennae

**short hundredweight** n (1924): HUNDREDWEIGHT 1

**short-leaf pine** \ˈshɔrt-lɛf-/ n (1796): a pine (*Pinus echinata*) of the southeastern U.S. that has short flexible needles usu. in clusters of two and reddish brown bark; also: its yellow wood

**short line** n (ca. 1917): a transportation system (as a railroad) operating over a relatively short distance

**short-list** \ˈshɔrt-lɪst/ n (1927): a list of candidates for final consideration (as for a position or a prize) — **short-list** vt, chiefly Brit

**short-lived** \ˈshɔrt-lɪvd also ˈlɪvd/ adj (1588): not living or lasting long (~ insects) (~ joy)

**short loin** n (ca. 1923): a portion of the hindquarter of beef immediately behind the ribs that is usu. cut into steaks — see BEEF illustration

**short-ly** \ˈshɔrt-lɪ/ adv (bef. 12c) 1 a: in a few words: BRIEFLY b: in an abrupt manner 2 a: in a short time (we will be there ~) b: at a short interval (~ after sunset)

**short-ness** \-nəs/ n (bef. 12c): the quality or state of being short

**short-nosed cattle louse** \ˈshɔrt-nɔzd(-)-/ n (1942): a large bluish sucking louse (*Haematopinus eurysternus*) that attacks domestic cattle

**short-order** \ˈshɔrt-ɔr-dər, -ɔr-/ adj (1920): preparing or serving food that can be cooked quickly to a customer's order (a ~ cook)

**short-range** \ˈshɔrt-rænj/ adj (1869) 1: involving or taking into account a short period of time (~ plans) 2: relating to or fit for short distances

**short ribs** n pl (1912): a cut of beef consisting of rib ends between the rib roast and the plate — see BEEF illustration

**short run** n (1879): a relatively brief period of time — often used in the phrase *in the short run* — **short-run** adj

**short shrift** n (1594) 1: barely adequate time for confession before execution 2 a: little or no attention or consideration b: quick work — usu. used in the phrase *make short shrift of*

**short sight** n (ca. 1829): MYOPIA

# **EXHIBIT L-32**

**Ex. L-32**  
**CMO US PATENT No. 5,619,352**

**INDEX OF DISPUTED TERMS**

<b><u>CLAIM TERMS</u></b>	<b><u>PAGE</u></b>
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optical symmetry axis .....	1
tilt angle varies along an axis normal to said layer .....	1

**EXHIBIT L-32**  
**U.S. PATENT NO. 5,619,352**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 3**

3. A compensator for a liquid crystal display, said compensator comprising a layer of a birefringent material having an optical symmetry axis defined by a tilt angle, measured relative to the plane of the layer, and an azimuthal angle, measured relative to a reference axis in the plane of the layer, wherein said tilt angle varies along an axis normal to said layer, and said azimuthal angle is substantially fixed along an axis normal to said layer.

**LGD's Claim Construction**

**a layer of birefringent material** – a thickness of material including positively birefringent molecules that are uniaxial or near uniaxial in character

**optical symmetry axis**<sup>1</sup> – the extraordinary axis of the molecules

or

indefinite

**tilt angle varies along an axis normal to said layer** – the tilt angle of the compensator varies along an axis normal to the layer of birefringent material and is limited to values between approximately 25 degrees and approximately 65 degrees

<sup>1</sup> Disputed Term “optical symmetry axis” also appears in asserted claim 9 in the same context.

**INTRINSIC EVIDENCE FOR DISPUTED TERM “A  
LAYER OF A BIREFRINGENT MATERIAL”:**

Many of the materials discussed in this document are birefringent. That is to say, they have varying indices of refraction depending on the direction of the electric vector of the light propagating through the material. The index of refraction is the ratio of the speed of light in a vacuum to that in the material. Materials such as liquid crystals that have different optical properties along different axes are said to be optically anisotropic. Materials without such angular variation are said to be isotropic. A uniaxial optical material has only one axis, the extraordinary axis, along which the electric vector of light interacts to yield a unique index of refraction ( $n_e$ ). This index will either be the highest or lowest found in the material. In a uniaxial material all possible axes perpendicular to the extraordinary axis will yield the same index of refraction (called the ordinary index,  $n_o$ ) for light

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whose electric vector lies in those directions; the material has ellipsoidal symmetry. If the extraordinary axis has the highest associated refractive index value of any axis the material is said to be positively birefringent. If it has the lowest refractive index, the material is said to be negatively birefringent. Light traversing a material such that its electric vector has components along both ordinary and extraordinary axes will have one polarized component retarded in its velocity as compared to the other. If a material has a unique axis which is associated with the highest refractive index, but the axes perpendicular to it have associated refractive indices which differ one to the other, the material is said to be optically biaxial and we will refer to the axis with the associated highest index as the principal optic axis. In this document the term “optical symmetry axis” will be defined to mean the extraordinary axis in uniaxial materials and the principal optic axis in biaxial materials.

2:53-3:17

**INTRINSIC EVIDENCE FOR DISPUTED TERM “A  
LAYER OF A BIREFRINGENT MATERIAL” (cont’d):**

To eliminate reversal of gray levels and improve gray scale stability, a birefringent O-plate compensator can be used. The O-plate compensator principle, as described in pending U.S. patent application Ser. No. 223,251 filed on Apr. 4, 1994 utilizes a positive birefringent material with its principal optic axis oriented at a substantially oblique angle with respect to the plane of the display (hence the term “O-plate”). “Substantially oblique” implies an angle appreciably greater than  $0^\circ$  and less than  $90^\circ$ . O-plates have been utilized, for example, with angles relative to the plane of the display between  $35^\circ$  and  $55^\circ$ , typically at  $45^\circ$ . Moreover, O-plates with either uniaxial or biaxial materials can be used. O-plate compensators can be placed in a variety of locations between a LCD’s polarizer layer and analyzer layer.

7:8-15

**INTRINSIC EVIDENCE FOR DISPUTED TERM “A LAYER OF A BIREFRINGENT MATERIAL” (cont’d):**

The compensator design of this invention, which includes a positively birefringent twisted and/or splayed O-plate layer, makes possible a significant improvement in the gray scale properties and contrast ratios of liquid crystal displays (LCDs) over a wide range of viewing angles. By making use of polymerized thin films of organic liquid crystal materials the compensators are able to duplicate the performance of existing biaxial inorganic O-plate compensators, but at reduced cost and with more design flexibility.

An O-plate compensator comprising an organic liquid crystal polymer thin film, and methods for fabricating the same, are disclosed. On the microscopic scale the film is composed of a polymerized birefringent liquid crystal material which is uniaxial or near uniaxial in character. The liquid

10:51-64

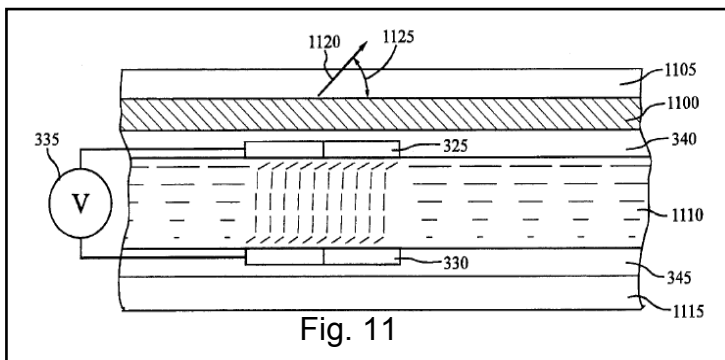
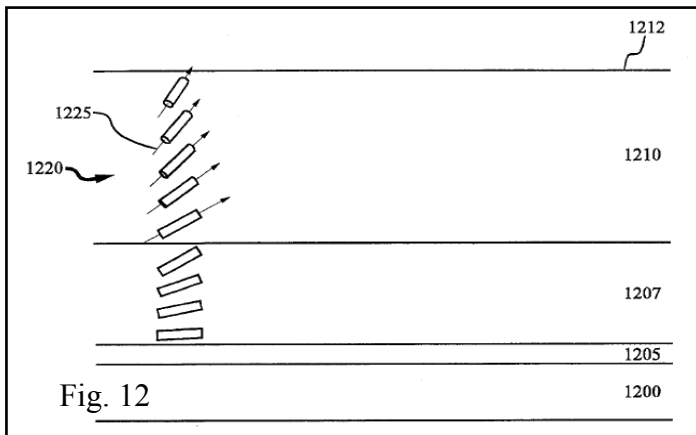


FIG. 11 shows an illustrative embodiment of a liquid crystal display (LCD) system in accordance with the invention, that uses a single twisted and/or splayed O-plate compensator 1100 disposed between a polarizer 1105 and a liquid crystal layer 1110. The O-plate layer 1100 comprises birefringent liquid crystal polymer layer having an optical symmetry axis 1120 oriented, on average, at a tilt angle 1125, relative to the surface of the liquid crystal polymer layer 1110, of approximately 20° to 80°. Alternatively, the O-plate layer could be located between liquid crystal layer 1110 and an analyzer 1115, or in both locations. More details on the structure of the twisted and/or splayed O-plate layer are given below.

12:45-50

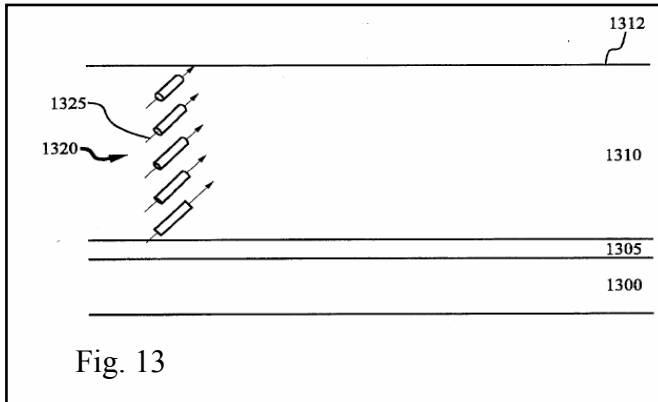
**INTRINSIC EVIDENCE FOR DISPUTED TERM “A  
LAYER OF A BIREFRINGENT MATERIAL” (cont’d):**



Another illustrative embodiment, shown in FIG. 12, includes a rigid glass substrate 1200, an alignment layer 1205, a polymerized pretilt nematic liquid crystal layer 1207, an alignment/pretilt layer interface 1205/1207, a polymerized nematic liquid crystal monomer layer 1210, a pretilt/liquid crystal layer interface 1207/1210 and a nematic/air interface 1212. The nematic material in the layer 1210 has been doped with a chiral dopant to yield a cholesteric pitch approximately 12 times the layer thickness, yielding a twist angle of approximately 30 degrees in the layer 1210. The liquid crystal layers are deposited in the form of polymerizable nematic monomer compounds doped with approximately 0.5% of Igracure-651, a photoinitiator.

13:8-20

**INTRINSIC EVIDENCE FOR DISPUTED TERM “A LAYER OF A BIREFRINGENT MATERIAL” (cont’d):**



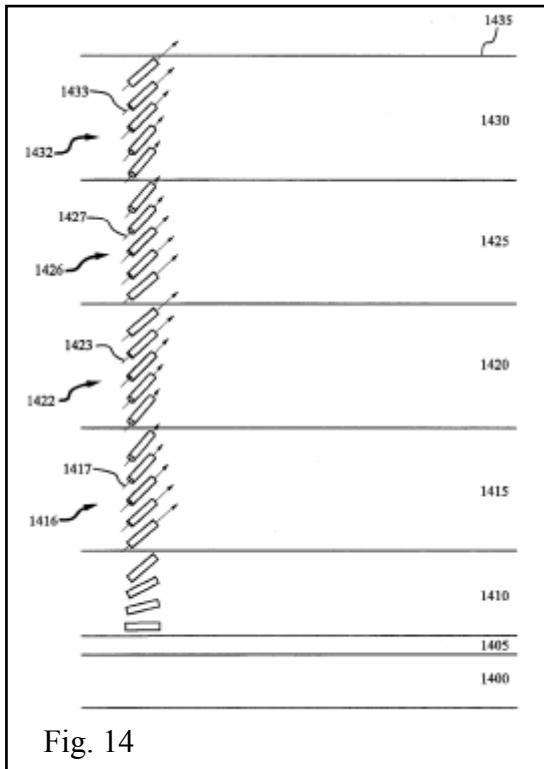
An alternative embodiment is shown in FIG. 13. As before, the compensator system comprises a rigid glass substrate **1300**, an alignment layer **1305**, a polymerized liquid crystal layer **1310**, a liquid crystal/alignment layer interface **1305/1310**, and a liquid crystal/air interface **1315**. In this embodiment, however, the polymerized liquid crystal layer **1310** has a smectic C phase and a smectic C intralayer tilt angle of 45°. As such, the desired intralayer tilt angle (45°) of the liquid crystal layer **1310** remains constant through the layer **1310**.

14:47-57

Upon obtaining the desired intralayer tilt angle in the liquid crystal film and the desired azimuthal orientation, the liquid crystal monomer film is irradiated with ultraviolet light that is sufficient to polymerize the monomer to a polymeric film **1310** in which the order of the smectic liquid crystal is preserved, typically 4–10 J/cm<sup>2</sup>. Other polymerization techniques for thin films are well known in the art and may also be used. The result of this process is a thin film or liquid crystal layer **1310** of liquid crystal polymer that is positively birefringent and has an optical symmetry axis that is oriented at a polar tilt angle of approximately 45° with a twist angle of approximately 30°.

15:63-67

**INTRINSIC EVIDENCE FOR DISPUTED TERM “A  
LAYER OF A BIREFRINGENT MATERIAL” (cont’d):**



A further illustrative liquid crystal display system, see FIG. 14, includes a rigid glass substrate 1400, an alignment layer 1405, polymerized nematic liquid crystal pretilt layer 1410, polymerized nematic liquid crystal layers 1415, 1420, 1425, and 1430; a liquid crystal/alignment layer interface 1405/1410, liquid crystal/liquid crystal interfaces 1410/1415, 1415/1420, 1420/1425, and 1425/1430; and a liquid crystal/air interface 1435.

16:3-10

**INTRINSIC EVIDENCE FOR DISPUTED TERM “A  
LAYER OF A BIREFRINGENT MATERIAL” (cont’d):**

The distinction is further evident from Haas’ use of both positively and negatively birefringent compensators, whereas the O-plate compensator of the present invention is always positively birefringent. Some confusion may exist, however, because of the use of the term “oblique” to discuss these compensator angles in both the present application and in Haas. In order to clearly distinguish the compensator orientations in the claimed invention from the teachings of Haas, Claims 1, 7, 8, and 9 have been amended to recite a positively birefringent O-plate compensator layer with its optic axis oriented “at a substantially oblique angle of between 25 and 65 degrees with respect to the normal axis”. With this amendment, the range of angle orientation about the 45°

App 08/223,251, 8/23/1995 Response to Office Action, page 7.

In the present application, however, the tilt orientation at the center of the liquid crystal focuses on a much different operating region, as shown by curves 304-316 in Figure 3 (reproduced above), none of which reach the 90° orientation. Yeh’s teaching involves only a negative birefringent compensator, which improves contrast but actually has a detrimental effect on gray scale.

App 08/223,251, 8/23/1995 Response to Office Action, page 9.

**INTRINSIC EVIDENCE FOR DISPUTED TERM**  
**“OPTICAL SYMMETRY AXIS”:**

Many of the materials discussed in this document are birefringent. That is to say, they have varying indices of refraction depending on the direction of the electric vector of the light propagating through the material. The index of refraction is the ratio of the speed of light in a vacuum to that in the material. Materials such as liquid crystals that have different optical properties along different axes are said to be optically anisotropic. Materials without such angular variation are said to be isotropic. A uniaxial optical material has only one axis, the extraordinary axis, along which the electric vector of light interacts to yield a unique index of refraction ( $n_e$ ). This index will either be the highest or lowest found in the material. In a uniaxial material all possible axes perpendicular to the extraordinary axis will yield the same index of refraction (called the ordinary index,  $n_o$ ) for light

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whose electric vector lies in those directions; the material has ellipsoidal symmetry. If the extraordinary axis has the highest associated refractive index value of any axis the material is said to be positively birefringent. If it has the lowest refractive index, the material is said to be negatively birefringent. Light traversing a material such that its electric vector has components along both ordinary and extraordinary axes will have one polarized component retarded in its velocity as compared to the other. If a material has a unique axis which is associated with the highest refractive index, but the axes perpendicular to it have associated refractive indices which differ one to the other, the material is said to be optically biaxial and we will refer to the axis with the associated highest index as the principal optic axis. In this document the term “optical symmetry axis” will be defined to mean the extraordinary axis in uniaxial materials and the principal optic axis in biaxial materials.

2:53-3:17

**INTRINSIC EVIDENCE FOR DISPUTED TERM**  
**“OPTICAL SYMMETRY AXIS” (cont’d):**

Computer modeling and display cell measurements show the optical behavior of the biaxial O-plate based compensators produced from  $Ta_2O_5$  to be qualitatively different from that of compensators produced from uniaxial polymerized liquid crystal materials. For some applications, gray-scale stability and contrast over field of view properties produced by the biaxial components are preferred. However, organic compensator films based on uniaxial liquid crystal polymers are very attractive because they both make a wider range of material parameters accessible and also allow the possibility of inexpensive mass production of compensator components. Therefore a goal of further compensator development has been to produce a thin film organic O-plate layer which shows biaxial character.

It is believed that biaxial compensator components produce qualitatively different optical performance because the deformation structure of the partially selected liquid crystal layer in a twisted nematic display has some biaxial character itself. In the nonselect state the liquid crystal has a helical structure which rotates the polarization state of incident light by means of the process of adiabatic waveguiding as described above. As the electric field across the liquid crystal layer is increased the helical structure is distorted and the efficiency of the waveguide decreases. Some portion of the light is no longer efficiently rotated and begins as a result to lag the rotation of the liquid crystal helical structure. This light encounters a medium intermediate in refractive index between the ordinary and extraordinary index values. The net result is that the medium appears biaxial.

The O-plate solution to the compensation of the twisted nematic display was based on the approximate model described above that the liquid crystal layer in the select state of the twisted nematic display could be divided into three regions, two A-plate-like regions and a central region of pseudo-homeotropic character. O-plate compensated displays, however, operate with the full-on black state accessible at voltages considerably reduced from the black state voltage in uncompensated displays. At these reduced drive voltages, the liquid crystal layer central region is unlikely to have completely deformed to the pseudo-homeotropic state, and the three region model becomes even more approximate. At these intermediate voltages the liquid crystal layer central region will still be significantly splayed and twisted yielding the biaxial character described in the above paragraph.

9:38-10:16

**INTRINSIC EVIDENCE FOR DISPUTED TERM**  
**“OPTICAL SYMMETRY AXIS” (cont’d):**

The compensator design of this invention, which includes a positively birefringent twisted and/or splayed O-plate layer, makes possible a significant improvement in the gray scale properties and contrast ratios of liquid crystal displays (LCDs) over a wide range of viewing angles. By making use of polymerized thin films of organic liquid crystal materials the compensators are able to duplicate the performance of existing biaxial inorganic O-plate compensators, but at reduced cost and with more design flexibility.

An O-plate compensator comprising an organic liquid crystal polymer thin film, and methods for fabricating the same, are disclosed. On the microscopic scale the film is composed of a polymerized birefringent liquid crystal material which is uniaxial or near uniaxial in character. The liquid

10:51-64

**INTRINSIC EVIDENCE FOR DISPUTED TERM “TILT  
ANGLE VARIES ALONG AN AXIS NORMAL TO SAID  
LAYER”:**

To eliminate reversal of gray levels and improve gray scale stability, a birefringent O-plate compensator can be used. The O-plate compensator principle, as described in pending U.S. patent application Ser. No. 223,251 filed on Apr. 4, 1994 utilizes a positive birefringent material with its principal optic axis oriented at a substantially oblique angle with respect to the plane of the display (hence the term “O-plate”). “Substantially oblique” implies an angle appreciably greater than  $0^\circ$  and less than  $90^\circ$ . O-plates have been utilized, for example, with angles relative to the plane of the display between  $35^\circ$  and  $55^\circ$ , typically at  $45^\circ$ . Moreover, O-plates with either uniaxial or biaxial materials can be used. O-plate compensators can be placed in a variety of locations between a LCD’s polarizer layer and analyzer layer.

7:8-22

mate. At these intermediate voltages the liquid crystal layer central region will still be significantly splayed and twisted yielding the biaxial character described in the above paragraph.

The intuitive approach to compensator development has been that like compensates like, i.e., compensators should have similar or complementary optical symmetries to the liquid crystal layers they are intended to compensate. Based

10:13-20

**INTRINSIC EVIDENCE FOR DISPUTED TERM “TILT  
ANGLE VARIES ALONG AN AXIS NORMAL TO SAID  
LAYER” (cont’d):**

rial which is uniaxial or near uniaxial in character. The liquid crystal material is constrained such that its optical symmetry axis is, on average, oriented obliquely with the surface of the film. Within this constraint, the direction of the material's

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optical symmetry axis is allowed to vary continuously along the axis normal to the film surface. If the variation is in the tilt angle of the optical symmetry axis relative to the film surface the liquid crystal material will have splayed structure. If the variation is in the azimuthal angle of the optical symmetry axis the material will have twisted structure. The invention can comprise either angular variation or both in combination.

The oblique orientation of the liquid crystal director, which is parallel to the optical symmetry axis, is achieved by casting an organic thin film onto a surface specially prepared for orienting liquid crystal monomers, such as oblique SiO<sub>2</sub>, mechanically rubbed polymers, etc. The variation in tilt angle through the layer is achieved by selecting a liquid crystalline material such that its tilt angle at the substrate surface is substantially different from that at the liquid crystal air interface. The variation in azimuthal angle through the layer is achieved by doping the liquid crystal monomer with a chiral additive in sufficient quantity so as to provide the proper helical pitch along the axis normal to the film surface. The film can either be cast from a solution of

10:64-11:21

Illustrative embodiments of the invention are described below as they might be implemented using polymeric liquid crystalline thin films to create a twisted and/or splayed O-plate compensator. In the interest of clarity, not all fea-

12:23-26

**INTRINSIC EVIDENCE FOR DISPUTED TERM “TILT ANGLE VARIES ALONG AN AXIS NORMAL TO SAID LAYER” (cont’d):**

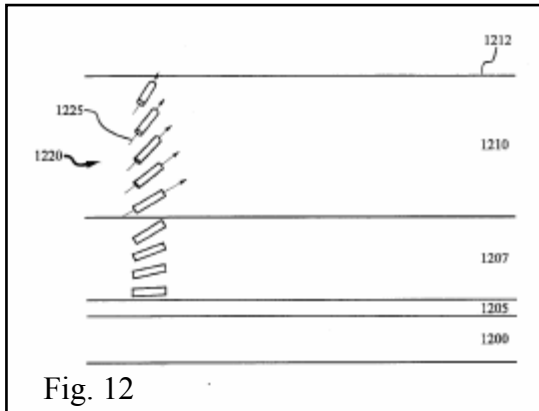


Fig. 12

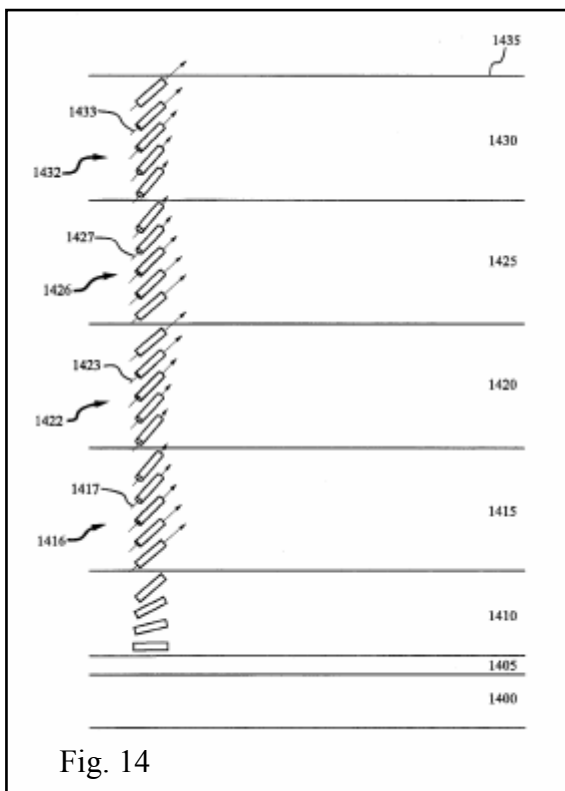
Other possible alignment layer materials could be substituted for the layers **1205** and **1207** to give the required 30° pretilt angle and azimuthal alignment for the liquid crystal layer **1210**. Such materials could include, for example,

14:4-7

In this particular embodiment, the material used to produce the layer **1210** has been chosen to have a tilt angle of 60° at the nematic/air interface **1212** (the 30° pretilt angle at the **1207/1210** interface plus a 30° splay angle through the layer **1210**). The solution concentration of the nematic monomer, concentration of prepolymerized nematic polymer, and the deposition parameters are selected such that the layer **1210** is of the proper thickness to provide the required retardation value, on the order of 1  $\mu\text{m}$ . A splayed/twisted O-plate layer prepared in this way will have a varying optical symmetry axis with a splay angle of 30°, a twist angle of 30°, and an average tilt angle of 45°.

14:33-44

**INTRINSIC EVIDENCE FOR DISPUTED TERM “TILT  
ANGLE VARIES ALONG AN AXIS NORMAL TO SAID  
LAYER” (cont’d):**



crystal layer 1415 is applied. As in the nematic embodiment above, the function of the layer 1410 is to increase the pretilt of the layer 1415 to 40° without altering the azimuthal orientation of the moieties 1416 in the layer 1415. The liquid

16:16-20

**INTRINSIC EVIDENCE FOR DISPUTED TERM “TILT  
ANGLE VARIES ALONG AN AXIS NORMAL TO SAID  
LAYER” (cont’d):**

- (c) each of [(i) A] said tilt angle [ $\phi$ , relative to the plane of the layer,] and [(ii) an] said azimuthal angle [ $\theta$ , relative to a reference axis in the plane of the layer, of said optical symmetry axis] varies along an axis normal to said layer, said tilt angle limited to values between approximately 25 degrees and approximately 65 degrees; and

App 08/313,476, 1/22/1996 Amendment and Response to  
Office Action of 21 September 1995, page 2.

2  
5. (Amended) [The compensator of claim 2] A compensator for a liquid crystal display, said compensator comprising a layer of a birefringent material having an optical symmetry axis defined by a tilt angle, measured relative to the plane of the layer, and an azimuthal angle, measured relative to a reference axis in the plane of the layer, wherein [an] said azimuthal angle [ $\theta$ , relative to a reference axis in the plane of the layer, of said optical symmetry axis] varies along an axis normal to said layer, and said tilt angle is substantially fixed at an angle between approximately 25 degrees and approximately 65 degrees, along an axis normal to said layer.

App 08/313,476, 1/22/1996 Amendment and Response to  
Office Action of 21 September 1995, page 3.

In contrast, a compensator in accordance with any one of claims 5, 6, and 7 has a birefringent layer whose optical axis (either tilt angle, or azimuthal angle, or both) varies. A further distinction between a compensator in accordance with any of claims 5, 6, and 7 and Heynderickx et al. is that the tilt angle is substantially greater than zero; “between approximately 25 degrees and approximately 65 degrees.” (See amended claim 5.) Specifically, Heynderickx

App 08/313,476, 1/22/1996 Amendment and Response to  
Office Action of 21 September 1995, page 9.

# **EXHIBIT L-33**

**Ex. L-33**  
**CMO US PATENT NO. 6,008,786**

**INDEX OF DISPUTED TERMS**

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delaying any uncorrected gray scale signal related to the other colors for the time delay caused by said corrected gray scale data signal being corrected .....	29
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changing the level of gray scale data signals related to at least one of the multicolors supplied to the display cell to create a corrected gray scale data signal with a level different from the inputted gray scale data signal .....	1
delaying the output for at least one other of the multicolor by the time taken for correction of said at least one color .....	29
simultaneously output the gray scale data of all said multicolors .....	52
calculation logic . . . for changing the level of the gray scale data signals of said at least one color to a different gray scale level .....	24
driver circuit for any other of the colors without the calculation logic in its driver circuit.....	46
delaying the gray scale signals for the other of the colors .....	46
changing the gray scale data signals related to one of the multicolors .....	24
delaying the output for any other color of the multicolors with gray scale data signals not subject to a correction by the amount of time taken for correction of the one color .....	49
synchronize the timing of the gray scale data signals for all said multicolors .....	52

**EXHIBIT L-33**  
**U.S. PATENT NO. 6,008,786**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 1**

1. A liquid crystal color display comprising:

- a) a display cell containing a light transmitting medium,
- b) **driver means** connected to said display cell for driving the display cell with sets of grey scale data signals each signal for a different color, and
- c) **data control means** for receiving gray scale data signals related to the setting of a gray scale for the display cell and outputting said gray scale data signals to said driver with a predetermined timing, wherein said data control means includes:
  - i) **computing means for changing the level of the gray scale data signals for at least one color relative to the other colors to a different gray scale level to compensate for a variation in intensity between the colors due to wavelength related differences in transmissivity between the colors through the light transmitting medium, and**
  - ii) **buffer means for delaying any uncorrected gray scale signal related to the other colors for the time delay caused by said corrected gray scale data signal being corrected.**

**ASSERTED CLAIM 5**

5. A method of gray scale data control for eliminating the effect wavelength dependency of transmissivity of light in a multicolor display cell comprising:

**changing the level of gray scale data signals related to at least one of the multicolors supplied to the display cell to create a corrected gray scale data signal with a level different from the inputted gray scale data signal to compensate for differences in transmissivity of the colors that result from wavelength dependence, and synchronizing the output of the gray scale data signals by delaying the output for at least one other of the multicolor by the time taken for correction of said at least one color to simultaneously output the gray scale data of all said multicolors.**

**LGD's Claim Construction**

**changing the level of the gray scale data signals for at least one color relative to the other colors to a different gray scale level – adding or subtracting compensation values to modify the gray scale levels of one or more, but not all, color video signals**

**changing the level of gray scale data signals related to at least one of the multicolors supplied to the display cell to create a corrected gray scale data signal with a level different from the inputted gray scale data signal – adding or subtracting compensation values to modify the gray scale levels of one or more, but not all, input color video signals**

**INTRINSIC EVIDENCE FOR DISPUTED TERM “CHANGING THE LEVEL OF THE GRAY SCALE DATA SIGNALS FOR AT LEAST ONE COLOR RELATIVE TO THE OTHER COLORS TO A DIFFERENT GRAY SCALE LEVEL”:**

transmissivity/applied voltage characteristics. However, the circuits needed to independently control the reference voltages, raise the cost and cause difficulties in the implementation. Another method that falls within this second category, is to use the voltage for one of the colors of R/G/B as a reference voltage, and use offset voltages for each of other colors. This methods has the same problems as the method in which the reference voltages are separately applied, and in addition, cannot accomplish desired effect if the gradients of the curves showing the transmissivity/applied voltage characteristics of R/G/B vary with applied voltage. That is, in accordance with the offset voltage method, correction is carried out by applying a uniform offset voltage for all applied voltages, and thus the correction cannot be effectively performed unless the gradients of the curves showing the transmissivity/applied voltage characteristics are the same over the whole applied voltage range.

2:50-67

Japanese Published Unexamined Patent Application No. 01-101586 discloses a technique in which different liquid crystal driving voltage levels are set for each of the colors, and that level is applied to each pixel. Japanese Published Unexamined Patent Application No. 03-6986 discloses a technique in which the driving voltage is made to vary a predetermined voltage from color to color to obtain uniformity in transmissivity. Japanese Published Unexamined Patent Application No. 03-290618 discloses a technique in which a similar object is accomplished by independently inputting a gray scale control signal for each color.

Therefore, first object of the subject invention is to provide a driving method for a TFTLCD in which the dependency on color of the transmissivity/applied voltage characteristics is effectively corrected.

A second object of the subject invention is to realize the effective correction using a very simple method which enables the above described correction to be made without increase in complexity of the control method, and the restrictions on the implementation by addition of circuits.

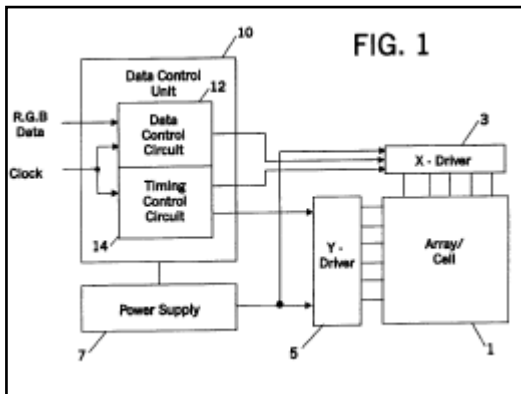
3:1-21

**INTRINSIC EVIDENCE FOR DISPUTED TERM “CHANGING THE LEVEL OF THE GRAY SCALE DATA SIGNALS FOR AT LEAST ONE COLOR RELATIVE TO THE OTHER COLORS TO A DIFFERENT GRAY SCALE LEVEL” (cont’d):**

**SUMMARY OF THE INVENTION**

In accordance with the present invention, the above described problems are solved by gray scale data (a bit string for a color liquid crystal display) wherein the data control means includes a computing circuit for performing an addition or subtraction of the gray scale related to at least one color to generate a corrected gray scale, and also includes delay means for delaying the outputting of the uncorrected gray scales, during the time which the gray scale of the one color is being corrected.

3:24-32

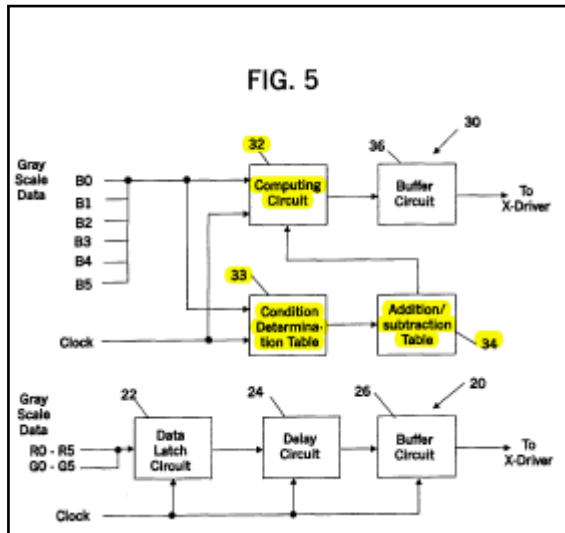


**PREFERRED EMBODIMENT**

The subject invention can be realized by improving the data control unit 10 of FIG. 1 as is shown in FIG. 5. In the background art, the data control unit consists only of a latch and a buffer. However, in the subject invention, the gray scale data related to a color, that is to be corrected, is temporarily inputted to a computing circuit. An addition or subtraction operation is applied to that gray scale data to shift it by one or more gray scale levels, to thereby achieve transmissivity equivalent to the other colors which are not to be corrected.

3:64-4:6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “CHANGING THE LEVEL OF THE GRAY SCALE DATA SIGNALS FOR AT LEAST ONE COLOR RELATIVE TO THE OTHER COLORS TO A DIFFERENT GRAY SCALE LEVEL” (cont’d):**



A portion 20 to which gray scale data related to R and G are inputted includes a data latch circuit 22 and a buffer circuit 26, like that in the data control unit in the background art. However, in addition to the data control unit in the background art, it includes a delay circuit 24. This is to compensate for the time during which the gray scale data B0 to B5 related to B is operated on by a computing circuit 32 in accordance with a condition determination table 36, as described later. The delay circuit 25 thereby assumes the outputting of the R and G gray scale data to the driver with the same timing as the corrected B gray scale data.

The gray data B0 to B5 for blue is a bit string for representing a 64-level gray scale. It is comprised of a bit string (B0, B1, B2, B3, B4, B5). For instance, if the gray scale is “4”, (B0, B1, B2, B3, B4, B5)=(001000), and if the gray scale is “28”, (B0, B1, B2, B3, B4, B5)=(001110). The same applied for R0 to R5 or G0 to G5 which are the gray scale data for reg or green, respectively.

4:11-29

**INTRINSIC EVIDENCE FOR DISPUTED TERM “CHANGING THE LEVEL OF THE GRAY SCALE DATA SIGNALS FOR AT LEAST ONE COLOR RELATIVE TO THE OTHER COLORS TO A DIFFERENT GRAY SCALE LEVEL” (cont’d):**

Gray Scale	Condition
0 - 3	A
4 - 10	B
11 - 53	C
54 - 60	B
61 - 63	A

FIG. 6

Further, the gray scale data for Blue is also supplied to a condition determination table 33. The condition determination table 33 determines the amount of the adjustment of the gray scale data. A diagrammatic representation of the condition determination table 33 is shown in FIG. 6. As shown, conditions A to C, corresponding to various gray scale levels, are set in the condition determination table 33. The

4:38-43

**INTRINSIC EVIDENCE FOR DISPUTED TERM “CHANGING THE LEVEL OF THE GRAY SCALE DATA SIGNALS FOR AT LEAST ONE COLOR RELATIVE TO THE OTHER COLORS TO A DIFFERENT GRAY SCALE LEVEL” (cont’d):**

FIG. 7

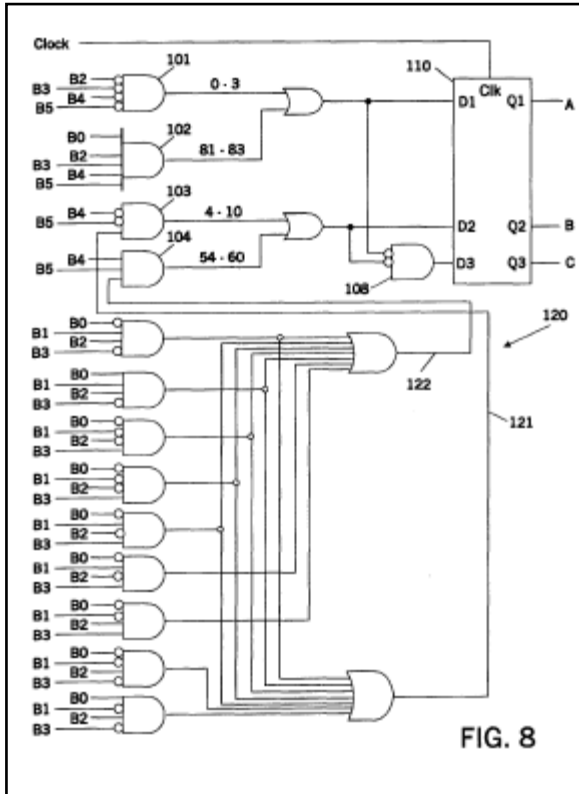
Condition	Addition/ Subtraction Amount
A	0
B	-2
C	-4
⋮	⋮

levels, are set in the condition determination table 33. The condition corresponding to a gray scale is outputted from the condition determination table 33 to an addition/subtraction table 34. The addition/subtraction table 34 has the function of setting the actual amount of the addition or subtraction. A diagrammatic representation of the addition/subtraction table 34 is shown in FIG. 7. That is, the addition/subtraction tables set the amount to be added or subtracted according to the condition provided from the condition determination table 33. The amount of the addition or subtraction to correct the gray scale is supplied to the computing circuit 32.

The condition determination table 33 and the addition/subtraction table 34 can be implemented by software. The

4:44-56

**INTRINSIC EVIDENCE FOR DISPUTED TERM “CHANGING THE LEVEL OF THE GRAY SCALE DATA SIGNALS FOR AT LEAST ONE COLOR RELATIVE TO THE OTHER COLORS TO A DIFFERENT GRAY SCALE LEVEL” (cont’d):**



The condition determination table 33 and the addition/subtraction table 34 can be implemented by software. The condition determination table can also be implemented by hardware by using the logic circuit shown in FIG. 8. To implement the specific conditions represented in FIG. 6, the gray scale data B0 to B5 are inputted to the logic circuit as shown. The gray scale data of B2 to B5 are inverted and inputted to an AND circuit 101 to create a condition corresponding to condition A in FIG. 6 for gray scale levels 0 to 3. Similarly, the gray scale data B0, B2 to B5 for gray scale levels 61 to 63 corresponding to condition A is inputted into AND circuit 102. The outputs of the AND circuit 101 and the AND circuit 102 are inputted to an OR circuit 106, and

4:55-67

**INTRINSIC EVIDENCE FOR DISPUTED TERM “CHANGING THE LEVEL OF THE GRAY SCALE DATA SIGNALS FOR AT LEAST ONE COLOR RELATIVE TO THE OTHER COLORS TO A DIFFERENT GRAY SCALE LEVEL” (cont’d):**

the condition A is outputted by circuit **110**. AND circuit **103** and AND circuit **104** are circuits for generating condition B. Inputted to ANDs **103** and **104** is an output **122** separately created in a group of logic circuits **120**, to thereby output the condition B for desired gray scale data levels **4** to **10** and **54** to **60**. If there is no output from OR circuits **106** and **107**, condition C is set. In this case, an output is provided by an AND circuit **108** to the circuit **110** to achieve the generation of condition C. Conditions A, B, and C are outputted from Q1 to Q3 of the circuit **110**.

5:1-10

Operation of the circuit **30** to which gray scale data for blue is inputted, and of the circuit **20** to which gray scale data related to Red and Green are inputted is as follows. When a gray scale level “2” is received, or (B0, B1, B2, B3, B4, B5)=(010000) is inputted, the input to the display is determined by the condition determination table **33**. As shown in FIG. 6, in the condition determination table **33**, the condition A is outputted to the addition/subtraction table **34**, and thereafter, in the addition/subtraction table **34**, “0” is outputted to the computing circuit as the addition or subtraction amount as shown in FIG. 7. Accordingly, the gray scale “2” is provided unconnected to the X-driver via a buffer circuit **36**. The above described processing causes a predetermined delay. Thus, the gray scale data for Red and Green corresponding to the gray scale data related to Blue are delayed for time taken for the processing by a delay circuit **24**. As a result, the gray scale data related to B is outputted from the buffer circuit **36** to the X-driver is synchronized with the gray scale data for Red and Green for simultaneous output from the buffer circuit **26** to the X-driver.

5:11-29

**INTRINSIC EVIDENCE FOR DISPUTED TERM “CHANGING THE LEVEL OF THE GRAY SCALE DATA SIGNALS FOR AT LEAST ONE COLOR RELATIVE TO THE OTHER COLORS TO A DIFFERENT GRAY SCALE LEVEL” (cont’d):**

Where the gray scale data level is “20,” or the grey scale level signal (B0, B1, B2, B3, B4, B5)=(001010), the condition determination table 33 provides condition C signal to the addition/subtraction table 34 as shown in FIG. 6. In response, the addition/subtraction table 34 provides a signal to the computing circuit to subtract four grey scale levels (the amount as shown as -4 in FIG. 7). Accordingly, the gray scale level “20” is corrected by the computing circuit 32 to a gray scale level “16”(20-4=16) which level is provided to the X-driver via the buffer circuit 36. In this way, corrections are made to the transmissivity/applied voltage characteristics where, as shown in FIG. 3, they are not uniform for each color.

5:30-42

With the method of the subject invention, only an additional circuit such as a computing circuit, is needed to effectively correct the differences in the transmissivity/applied voltage characteristics for colors. The above correction is made while avoiding the problems in complexity of control methods in the background art. That is, to implement

5:58-63

In using TFTLCDs to display pictures, it is necessary to provide gray scale data of the picture to the LCD to drive the LCD. FIG. 1 shows the construction of the control unit of the TFTLCD. The array/cell portion 1 of the LCD is connected to an X-driver 3 and a Y-driver 5. The X-driver 3, when it is supplied with gray scale data, applies a voltage corresponding to the gray scale data to the cell. The Y-driver 5 is connected to the gate of a switching element, and conducts/does not conduct the voltage applied to the cell by the X-driver 3 at a predetermined time.

Gray scale data is supplied to the X-driver by data control unit 10. The data control unit 10 consists of a data control circuit 12 for latching and storing the externally supplied R/G/B data in a buffer, and a timing control circuit 14 for outputting the gray scale data stored in the buffer to the X-driver 3 at a predetermined time. A clock signal is externally supplied to the data control circuit 12 and the timing control circuit 14 to control the timing. A power supply 7 is connected to the X-driver, Y-driver 5, and data control unit 10.

1:27-46

**INTRINSIC EVIDENCE FOR DISPUTED TERM “CHANGING THE LEVEL OF THE GRAY SCALE DATA SIGNALS FOR AT LEAST ONE COLOR RELATIVE TO THE OTHER COLORS TO A DIFFERENT GRAY SCALE LEVEL” (cont’d):**

The claims in the application are rejected under 35 USC §103(a) as being unpatentable over Kennedy in view of Kanie et al. The Examiner points out that the Kennedy patent fails to teach the use of a buffer to eliminate phase shifts in color transmission. From what the applicants' attorney can see, there is a reason for this. There is no apparent delay of the gray scale levels from one color relative to the other colors resulting from the gray scale signals being transmitted through the apparatus of Kennedy. Each of the R, G & B channels in Kennedy is subjected to the same correction. Therefore, there is no need to delay the gray scale data of one relative to another. In fact, such a delay, with respect to one color, would be detrimental since it would skew the timing of information for that one color relative to the other colors. The purpose of the apparatus in the Kennedy patent is to make the incoming gray scale signals each conform to the same standard binary range of 000 (lowest intensity) to 111 (maximum intensity). The purpose of the present invention is to vary the level of at least one of the gray scale signals relative to the other gray scale signals to compensate for differences in transmissivity through the display device.

Group 2700

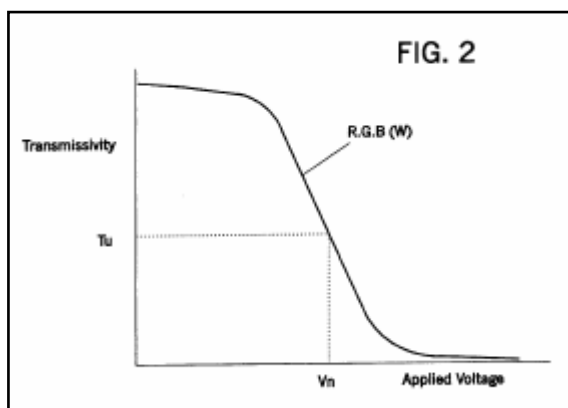
App. 08/832,640, 04/02/1999 Office  
Action, pgs. 5-6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “CHANGING THE LEVEL OF THE GRAY SCALE DATA SIGNALS FOR AT LEAST ONE COLOR RELATIVE TO THE OTHER COLORS TO A DIFFERENT GRAY SCALE LEVEL” (cont’d):**

Reasons for allowance	
1.	Claims 1-13 are allowed.
2.	The following is an examiner's statement of reasons for allowance:
	None of the references, either singularly or in combination, teach or fairly suggests:
	<i>A liquid crystal color display comprising:</i>
a)	<i>a display cell containing a light transmitting medium,</i>
b)	<i>driver means connected to said display cell for driving the display cell with sets of gray scale data signals each signal for a different color, and</i>
c)	<i>data control means for receiving gray scale data signals related to the setting of a gray scale for the display cell and outputting said gray scale data signals to said driver with a predetermined timing, wherein said data control means includes:</i>
i)	<i>computing means for changing the level of the gray scale data signals for at least one color relative to the other colors to a different gray scale level to compensate for a variation in intensity between the colors due to wavelength related differences in transmissivity between the colors through the light transmitting medium, and</i>
ii)	<i>buffer means for delaying any uncorrected gray scale signal related to the other colors for the time delay caused by said corrected gray scale data signal being corrected.</i>

App. 08/832,640, 04/02/1999 Office  
Action, pgs. 5-6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “CHANGING THE LEVEL OF GRAY SCALE DATA SIGNALS RELATED TO AT LEAST ONE OF THE MULTICOLORS SUPPLIED TO THE DISPLAY CELL TO CREATE A CORRECTED GRAY SCALE DATA SIGNAL WITH A LEVEL DIFFERENT FROM THE INPUTTED GRAY SCALE DATA SIGNAL”:**



to the respective gray scale data. Ideally, the same transmissivity can be achieved for all the colors when the voltage corresponding to a particular gray scale is used. The relationship for this is shown in FIG. 2. In FIG. 2, transmissivity is plotted on the ordinate, and applied voltage is plotted on the abscissa. Applied voltage is determined by the gray scale data. Accordingly, when a certain gray scale  $n$  is chosen, the applied voltage  $V_n$  is determined by that gray scale. Then, according to the relationship of FIG. 2, transmissivity  $T_n$  for the gray scale  $V_n$  is achieved.

1:56-65

**INTRINSIC EVIDENCE FOR DISPUTED TERM “CHANGING THE LEVEL OF GRAY SCALE DATA SIGNALS RELATED TO AT LEAST ONE OF THE MULTICOLORS SUPPLIED TO THE DISPLAY CELL TO CREATE A CORRECTED GRAY SCALE DATA SIGNAL WITH A LEVEL DIFFERENT FROM THE INPUTTED GRAY SCALE DATA SIGNAL” (cont’d):**

Ideally, the relationship between gray scale, applied voltage, and transmissivity is the same for each of the R/G/B colors. However in actuality, the gray scale and the achieved transmissivity have a slight difference depending on color. This is because the degree of light modulation for the specific twist of the twisted noematic liquid crystal is slightly different depending on wavelength. That is, even though a light passes through a liquid crystal layer in a similarly twisted state, the degree of the modulation given to the passing light is wavelength dependent, and thus the scattering of brightness that occurs for a given gray scale is color dependent. This is shown in FIG. 3. The transmissivity

1:66-2:10

As an example of the second category (2), is a method in which the reference voltage (gray scale voltage) given to the data driver is tailored to the characteristics for each color. This method can compensate for the color dependency of the transmissivity/applied voltage characteristics. However, the circuits needed to independently control the reference voltages, raise the cost and cause difficulties in the implementation. Another method that falls within this second category, is to use the voltage for one of the colors of R/G/B as a reference voltage, and use offset voltages for each of other colors. This methods has the same problems as the method in which the reference voltages are separately applied, and in addition, cannot accomplish desired effect if the gradients of the curves showing the transmissivity/applied voltage characteristics of R/G/B vary with applied voltage. That is, in accordance with the offset voltage method, correction is carried out by applying a uniform offset voltage for all applied voltages, and thus the correction cannot be effectively performed unless the gradients of the curves showing the transmissivity/applied voltage characteristics are the same over the whole applied voltage range.

2:46-67

**INTRINSIC EVIDENCE FOR DISPUTED TERM “CHANGING THE LEVEL OF GRAY SCALE DATA SIGNALS RELATED TO AT LEAST ONE OF THE MULTICOLORS SUPPLIED TO THE DISPLAY CELL TO CREATE A CORRECTED GRAY SCALE DATA SIGNAL WITH A LEVEL DIFFERENT FROM THE INPUTTED GRAY SCALE DATA SIGNAL” (cont’d):**

Japanese Published Unexamined Patent Application No. 01-101586 discloses a technique in which different liquid crystal driving voltage levels are set for each of the colors, and that level is applied to each pixel. Japanese Published Unexamined Patent Application No. 03-6986 discloses a technique in which the driving voltage is made to vary a predetermined voltage from color to color to obtain uniformity in transmissivity. Japanese Published Unexamined Patent Application No. 03-290618 discloses a technique in which a similar object is accomplished by independently inputting a gray scale control signal for each color.

Therefore, first object of the subject invention is to provide a driving method for a TFTLCD in which the dependency on color of the transmissivity/applied voltage characteristics is effectively corrected.

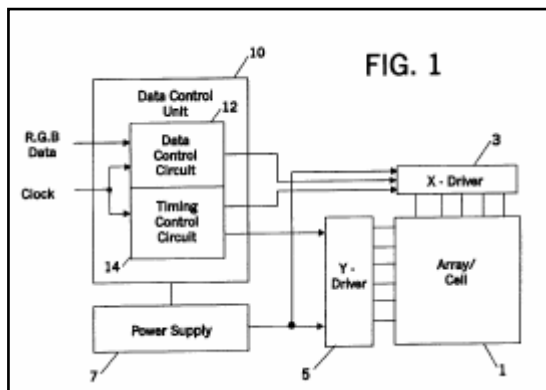
A second object of the subject invention is to realize the effective correction using a very simple method which enables the above described correction to be made without increase in complexity of the control method, and the restrictions on the implementation by addition of circuits.

**SUMMARY OF THE INVENTION**

In accordance with the present invention, the above described problems are solved by gray scale data (a bit string for a color liquid crystal display) wherein the data control means includes a computing circuit for performing an addition or subtraction of the gray scale related to at least one color to generate a corrected gray scale, and also includes delay means for delaying the outputting of the uncorrected gray scales, during the time which the gray scale of the one color is being corrected.

3:1-32

**INTRINSIC EVIDENCE FOR DISPUTED TERM “CHANGING THE LEVEL OF GRAY SCALE DATA SIGNALS RELATED TO AT LEAST ONE OF THE MULTICOLORS SUPPLIED TO THE DISPLAY CELL TO CREATE A CORRECTED GRAY SCALE DATA SIGNAL WITH A LEVEL DIFFERENT FROM THE INPUTTED GRAY SCALE DATA SIGNAL” (cont’d):**

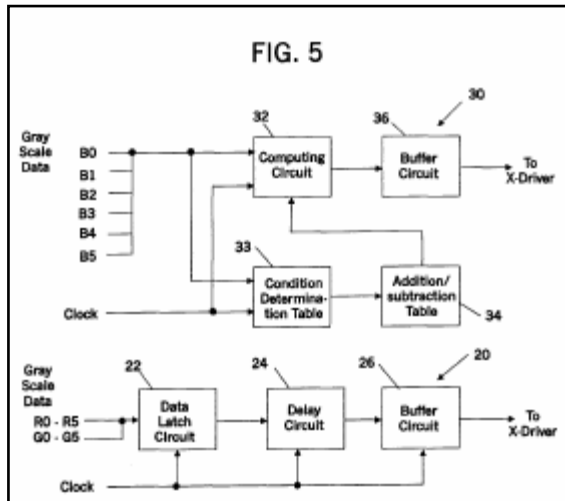


**PREFERRED EMBODIMENT**

The subject invention can be realized by improving the data control unit 10 of FIG. 1 as is shown in FIG. 5. In the background art, the data control unit consists only of a latch and a buffer. However, in the subject invention, the gray scale data related to a color, that is to be corrected, is temporarily inputted to a computing circuit. An addition or subtraction operation is applied to that gray scale data to shift it by one or more gray scale levels, to thereby achieve transmissivity equivalent to the other colors which are not to be corrected.

3:64-4:6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “CHANGING THE LEVEL OF GRAY SCALE DATA SIGNALS RELATED TO AT LEAST ONE OF THE MULTICOLORS SUPPLIED TO THE DISPLAY CELL TO CREATE A CORRECTED GRAY SCALE DATA SIGNAL WITH A LEVEL DIFFERENT FROM THE INPUTTED GRAY SCALE DATA SIGNAL” (cont’d):**



In FIG. 5, the color to be corrected is blue (B), and the colors which are not to be corrected are red (R) and green (G). The gray scale data related to R or G are shown by R0 to R5 or G0 to G5 in FIG. 5.

A portion 20 to which gray scale data related to R and G are inputted includes a data latch circuit 22 and a buffer circuit 26, like that in the data control unit in the background art. However, in addition to the data control unit in the background art, it includes a delay circuit 24. This is to compensate for the time during which the gray scale data B0 to B5 related to B is operated on by a computing circuit 32 in accordance with a condition determination table 36, as described later. The delay circuit 25 thereby assumes the outputting of the R and G gray scale data to the driver with the same timing as the corrected B gray scale data.

The gray data B0 to B5 for blue is a bit string for representing a 64-level gray scale. It is comprised of a bit string (B0, B1, B2, B3, B4, B5). For instance, if the gray scale is “4”, (B0, B1, B2, B3, B4, B5)=(001000), and if the gray scale is “28”, (B0, B1, B2, B3, B4, B5)=(001110). The same applied for R0 to R5 or G0 to G5 which are the gray scale data for red or green, respectively.

4:7-29

**INTRINSIC EVIDENCE FOR DISPUTED TERM “CHANGING THE LEVEL OF GRAY SCALE DATA SIGNALS RELATED TO AT LEAST ONE OF THE MULTICOLORS SUPPLIED TO THE DISPLAY CELL TO CREATE A CORRECTED GRAY SCALE DATA SIGNAL WITH A LEVEL DIFFERENT FROM THE INPUTTED GRAY SCALE DATA SIGNAL” (cont’d):**

Gray Scale	Condition
0 - 3	A
4 - 10	B
11 - 53	C
54 - 60	B
61 - 63	A

FIG. 6

Further, the gray scale data for Blue is also supplied to a condition determination table 33. The condition determination table 33 determines the amount of the adjustment of the gray scale data. A diagrammatic representation of the condition determination table 33 is shown in FIG. 6. As shown, conditions A to C, corresponding to various gray scale levels, are set in the condition determination table 33. The

4:38-44

**INTRINSIC EVIDENCE FOR DISPUTED TERM “CHANGING THE LEVEL OF GRAY SCALE DATA SIGNALS RELATED TO AT LEAST ONE OF THE MULTICOLORS SUPPLIED TO THE DISPLAY CELL TO CREATE A CORRECTED GRAY SCALE DATA SIGNAL WITH A LEVEL DIFFERENT FROM THE INPUTTED GRAY SCALE DATA SIGNAL” (cont’d):**

FIG. 7

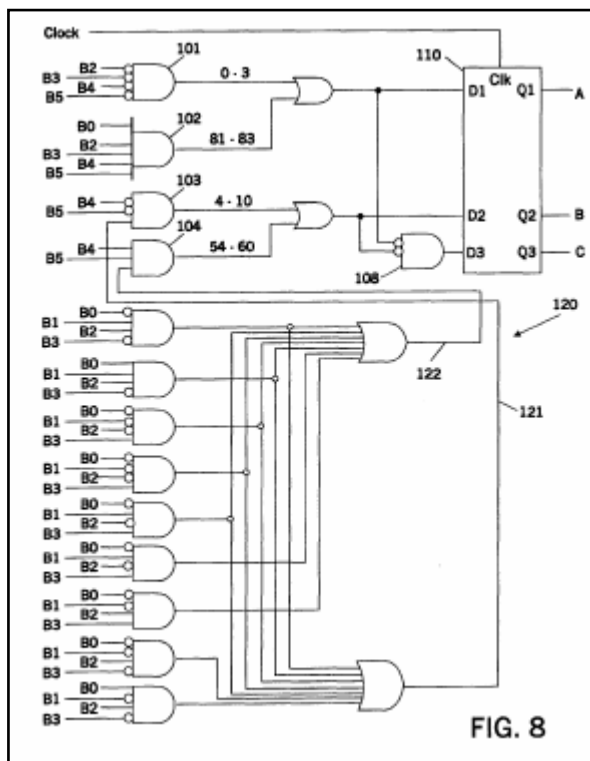
Condition	Addition/ Subtraction Amount
A	0
B	-2
C	-4
⋮	⋮

levels, are set in the condition determination table 33. The condition corresponding to a gray scale is outputted from the condition determination table 33 to an addition/subtraction table 34. The addition/subtraction table 34 has the function of setting the actual amount of the addition or subtraction. A diagrammatic representation of the addition/subtraction table 34 is shown in FIG. 7. That is, the addition/subtraction tables set the amount to be added or subtracted according to the condition provided from the condition determination table 33. The amount of the addition or subtraction to correct the gray scale is supplied to the computing circuit 32.

The condition determination table 33 and the addition/subtraction table 34 can be implemented by software. The

4:45-56

**INTRINSIC EVIDENCE FOR DISPUTED TERM “CHANGING THE LEVEL OF GRAY SCALE DATA SIGNALS RELATED TO AT LEAST ONE OF THE MULTICOLORS SUPPLIED TO THE DISPLAY CELL TO CREATE A CORRECTED GRAY SCALE DATA SIGNAL WITH A LEVEL DIFFERENT FROM THE INPUTTED GRAY SCALE DATA SIGNAL” (cont’d):**



The condition determination table 33 and the addition/subtraction table 34 can be implemented by software. The condition determination table can also be implemented by hardware by using the logic circuit shown in FIG. 8. To implement the specific conditions represented in FIG. 6, the gray scale data B0 to B5 are inputted to the logic circuit as shown. The gray scale data of B2 to B5 are inverted and inputted to an AND circuit 101 to create a condition corresponding to condition A in FIG. 6 for gray scale levels 0 to 3. Similarly, the gray scale data B0, B2 to B5 for gray scale levels 61 to 63 corresponding to condition A is inputted into AND circuit 102. The outputs of the AND circuit 101 and the AND circuit 102 are inputted to an OR circuit 106, and

4:45-67

**INTRINSIC EVIDENCE FOR DISPUTED TERM “CHANGING THE LEVEL OF GRAY SCALE DATA SIGNALS RELATED TO AT LEAST ONE OF THE MULTICOLORS SUPPLIED TO THE DISPLAY CELL TO CREATE A CORRECTED GRAY SCALE DATA SIGNAL WITH A LEVEL DIFFERENT FROM THE INPUTTED GRAY SCALE DATA SIGNAL” (cont’d):**

the condition A is outputted by circuit 110. AND circuit 103 and AND circuit 104 are circuits for generating condition B. Inputted to ANDs 103 and 104 is an output 122 separately created in a group of logic circuits 120, to thereby output the condition B for desired gray scale data levels 4 to 10 and 54 to 60. If there is no output from OR circuits 106 and 107, condition C is set. In this case, an output is provided by an AND circuit 108 to the circuit 110 to achieve the generation of condition C. Conditions A, B, and C are outputted from Q1 to Q3 of the circuit 110.

5:1-10

Operation of the circuit 30 to which gray scale data for blue is inputted, and of the circuit 20 to which gray scale data related to Red and Green are inputted is as follows. When a gray scale level “2” is received, or (B0, B1, B2, B3, B4, B5)=(010000) is inputted, the input to the display is determined by the condition determination table 33. As shown in FIG. 6, in the condition determination table 33, the condition A is outputted to the addition/subtraction table 34, and thereafter, in the addition/subtraction table 34, “0” is outputted to the computing circuit as the addition or subtraction amount as shown in FIG. 7. Accordingly, the gray scale “2” is provided unconnected to the X-driver via a buffer circuit 36. The above described processing causes a predetermined delay. Thus, the gray scale data for Red and Green corresponding to the gray scale data related to Blue are delayed for time taken for the processing by a delay circuit 24. As a result, the gray scale data related to B is outputted from the buffer circuit 36 to the X-driver is synchronized with the gray scale data for Red and Green for simultaneous output from the buffer circuit 26 to the X-driver.

5:11-30

**INTRINSIC EVIDENCE FOR DISPUTED TERM “CHANGING THE LEVEL OF GRAY SCALE DATA SIGNALS RELATED TO AT LEAST ONE OF THE MULTICOLORS SUPPLIED TO THE DISPLAY CELL TO CREATE A CORRECTED GRAY SCALE DATA SIGNAL WITH A LEVEL DIFFERENT FROM THE INPUTTED GRAY SCALE DATA SIGNAL” (cont’d):**

Where the gray scale data level is “20,” or the grey scale level signal (B0, B1, B2, B3, B4, B5)=(001010), the condition determination table 33 provides condition C signal to the addition/subtraction table 34 as shown in FIG. 6. In response, the addition/subtraction table 34 provides a signal to the computing circuit to subtract four grey scale levels (the amount as shown as -4 in FIG. 7). Accordingly, the gray scale level “20” is corrected by the computing circuit 32 to a gray scale level “16”(20-4=16) which level is provided to the X-driver via the buffer circuit 36. In this way, corrections are made to the transmissivity/applied voltage characteristics where, as shown in FIG. 3, they are not uniform for each color.

5:31-43

With the method of the subject invention, only an additional circuit such as a computing circuit, is needed to effectively correct the differences in the transmissivity/applied voltage characteristics for colors. The above correction is made while avoiding the problems in complexity of control methods in the background art. That is, to implement

5:58-63

**INTRINSIC EVIDENCE FOR DISPUTED TERM “CHANGING THE LEVEL OF GRAY SCALE DATA SIGNALS RELATED TO AT LEAST ONE OF THE MULTICOLORS SUPPLIED TO THE DISPLAY CELL TO CREATE A CORRECTED GRAY SCALE DATA SIGNAL WITH A LEVEL DIFFERENT FROM THE INPUTTED GRAY SCALE DATA SIGNAL” (cont’d):**

The claims in the application are rejected under 35 USC §103(a) as being unpatentable over Kennedy in view of Kanie et al. The Examiner points out that the Kennedy patent fails to teach the use of a buffer to eliminate phase shifts in color transmission. From what the applicants' attorney can see, there is a reason for this. There is no apparent delay of the gray scale levels from one color relative to the other colors resulting from the gray scale signals being transmitted through the apparatus of Kennedy. Each of the R, G & B channels in Kennedy is subjected to the same correction. Therefore, there is no need to delay the gray scale data of one relative to another. In fact, such a delay, with respect to one color, would be detrimental since it would skew the timing of information for that one color relative to the other colors. The purpose of the apparatus in the Kennedy patent is to make the incoming gray scale signals each conform to the same standard binary range of 000 (lowest intensity) to 111 (maximum intensity). The purpose of the present invention is to vary the level of at least one of the gray scale signals relative to the other gray scale signals to compensate for differences in transmissivity through the display device.

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**INTRINSIC EVIDENCE FOR DISPUTED TERM “CHANGING THE LEVEL OF GRAY SCALE DATA SIGNALS RELATED TO AT LEAST ONE OF THE MULTICOLORS SUPPLIED TO THE DISPLAY CELL TO CREATE A CORRECTED GRAY SCALE DATA SIGNAL WITH A LEVEL DIFFERENT FROM THE INPUTTED GRAY SCALE DATA SIGNAL”**

Reasons for allowance	
1.	Claims 1-13 are allowed.
2.	The following is an examiner's statement of reasons for allowance:
	None of the references, either singularly or in combination, teach or fairly suggests:
	<i>A liquid crystal color display comprising:</i>
a)	<i>a display cell containing a light transmitting medium,</i>
b)	<i>driver means connected to said display cell for driving the display cell with sets of gray scale data signals each signal for a different color, and</i>
c)	<i>data control means for receiving gray scale data signals related to the setting of a gray scale for the display cell and outputting said gray scale data signals to said driver with a predetermined timing, wherein said data control means includes:</i>
i)	<i>computing means for changing the level of the gray scale data signals for at least one color relative to the other colors to a different gray scale level to compensate for a variation in intensity between the colors due to wavelength related differences in transmissivity between the colors through the light transmitting medium, and</i>
ii)	<i>buffer means for delaying any uncorrected gray scale signal related to the other colors for the time delay caused by said corrected gray scale data signal being corrected.</i>

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**EXHIBIT S**  
**U.S. PATENT NO. 6,008,786**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 7**

7. A liquid crystal multicolor display comprising:  
a) display cells containing a light transmitting medium,  
b) driver circuits connected to said display cells for driving the display cells with sets of gray scale data signals each driver circuit for a different one of the colors,

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i) calculation logic in the driver circuit of at least one color for changing the level of the gray scale data signals of said at least one color to a different gray scale level to compensate for color distortion due to wavelength related differences in transmissivity between the colors through the light transmitting medium, and  
ii) delay logic in the driver circuit for any other of the colors without the calculation logic in its driver circuit for delaying the gray scale signals for the other of the colors to synchronize the provision of the sets of gray scale data signals by compensating for the delay caused by the calculation logic.

**LGD's Claim Construction**

**calculation logic ... for changing the level of the gray scale data signals of said at least one color to a different gray scale level** – calculation logic ... for adding or subtracting compensation values to modify one or more, but not all, color video signals

**changing the gray scale data signals related to one of the multicolors** – adding or subtracting compensation values to modify the gray scale level of one of the color video signals

**ASSERTED CLAIM 12**

12. A method of gray scale data control for reducing the effect wavelength dependency on transmissivity of light in cells of a multicolor display comprising:  
changing the gray scale data signals related to one of the multicolors to correct for the wavelength dependency of transmissivity and thereby create a corrected gray scale data signal different from the inputted gray scale data signal for that color, and synchronizing the timing of the gray scale data signals by delaying the output for any other color of the multicolors with gray scale data signals not subject to a correction by the amount of time taken for correction of the one color to synchronize the timing of the gray scale data signals for all said multicolors.

**INTRINSIC EVIDENCE FOR DISPUTED TERM “CALCULATION LOGIC ... FOR CHANGING THE LEVEL OF THE GRAY SCALE DAYS SIGNALS OF SAID AT LEAST ONE COLOR TO A DIFFERENT GRAY SCALE LEVEL”:**

The claims in the application are rejected under 35 USC §103(a) as being unpatentable over Kennedy in view of Kanie et al. The Examiner points out that the Kennedy patent fails to teach the use of a buffer to eliminate phase shifts in color transmission. From what the applicants' attorney can see, there is a reason for this. There is no apparent delay of the gray scale levels from one color relative to the other colors resulting from the gray scale signals being transmitted through the apparatus of Kennedy. Each of the R, G & B channels in Kennedy is subjected to the same correction. Therefore, there is no need to delay the gray scale data of one relative to another. In fact, such a delay, with respect to one color, would be detrimental since it would skew the timing of information for that one color relative to the other colors. The purpose of the apparatus in the Kennedy patent is to make the incoming gray scale signals each conform to the same standard binary range of 000 (lowest intensity) to 111 (maximum intensity). The purpose of the present invention is to vary the level of at least one of the gray scale signals relative to the other gray scale signals to compensate for differences in transmissivity through the display device.

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**INTRINSIC EVIDENCE FOR DISPUTED TERM “CALCULATION LOGIC ... FOR CHANGING THE LEVEL OF THE GRAY SCALE DAYS SIGNALS OF SAID AT LEAST ONE COLOR TO A DIFFERENT GRAY SCALE LEVEL” (cont’d):**

Reasons for allowance	
1.	Claims 1-13 are allowed.
2.	The following is an examiner's statement of reasons for allowance:
	None of the references, either singularly or in combination, teach or fairly suggests:
	<i>A liquid crystal color display comprising:</i>
a)	<i>a display cell containing a light transmitting medium,</i>
b)	<i>driver means connected to said display cell for driving the display cell with sets of gray scale data signals each signal for a different color, and</i>
c)	<i>data control means for receiving gray scale data signals related to the setting of a gray scale for the display cell and outputting said gray scale data signals to said driver with a predetermined timing, wherein said data control means includes:</i>
i)	<i>computing means for changing the level of the gray scale data signals for at least one color relative to the other colors to a different gray scale level to compensate for a variation in intensity between the colors due to wavelength related differences in transmissivity between the colors through the light transmitting medium, and</i>
ii)	<i>buffer means for delaying any uncorrected gray scale signal related to the other colors for the time delay caused by said corrected gray scale data signal being corrected.</i>

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**INTRINSIC EVIDENCE FOR DISPUTED TERM “CHANGING THE GRAY SCALE DATA SIGNALS RELATED TO ONE OF THE MULTICOLORS”:**

The claims in the application are rejected under 35 USC §103(a) as being unpatentable over Kennedy in view of Kanie et al. The Examiner points out that the Kennedy patent fails to teach the use of a buffer to eliminate phase shifts in color transmission. From what the applicants' attorney can see, there is a reason for this. There is no apparent delay of the gray scale levels from one color relative to the other colors resulting from the gray scale signals being transmitted through the apparatus of Kennedy. Each of the R, G & B channels in Kennedy is subjected to the same correction. Therefore, there is no need to delay the gray scale data of one relative to another. In fact, such a delay, with respect to one color, would be detrimental since it would skew the timing of information for that one color relative to the other colors. The purpose of the apparatus in the Kennedy patent is to make the incoming gray scale signals each conform to the same standard binary range of 000 (lowest intensity) to 111 (maximum intensity). The purpose of the present invention is to vary the level of at least one of the gray scale signals relative to the other gray scale signals to compensate for differences in transmissivity through the display device.

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**INTRINSIC EVIDENCE FOR DISPUTED TERM “CHANGING THE GRAY SCALE DATA SIGNALS RELATED TO ONE OF THE MULTICOLORS”(cont’d):**

Reasons for allowance	
1.	Claims 1-13 are allowed.
2.	The following is an examiner's statement of reasons for allowance:
	None of the references, either singularly or in combination, teach or fairly suggests:
	<i>A liquid crystal color display comprising:</i>
a)	<i>a display cell containing a light transmitting medium,</i>
b)	<i>driver means connected to said display cell for driving the display cell with sets of gray scale data signals each signal for a different color, and</i>
c)	<i>data control means for receiving gray scale data signals related to the setting of a gray scale for the display cell and outputting said gray scale data signals to said driver with a predetermined timing, wherein said data control means includes:</i>
i)	<i>computing means for changing the level of the gray scale data signals for at least one color relative to the other colors to a different gray scale level to compensate for a variation in intensity between the colors due to wavelength related differences in transmissivity between the colors through the light transmitting medium, and</i>
ii)	<i>buffer means for delaying any uncorrected gray scale signal related to the other colors for the time delay caused by said corrected gray scale data signal being corrected.</i>

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**EXHIBIT S**  
**U.S. PATENT NO. 6,008,786**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 1**

**1. A liquid crystal color display comprising:**  
a) a display cell containing a light transmitting medium,  
b) driver means connected to said display cell for driving the display cell with sets of grey scale data signals each signal for a different color, and  
c) data control means for receiving gray scale data signals related to the setting of a gray scale for the display cell and outputting said gray scale data signals to said driver with a predetermined timing, wherein said data control means includes:  
i) computing means for changing the level of the gray scale data signals for at least one color relative to the other colors to a different gray scale level to compensate for a variation in intensity between the colors due to wavelength related differences in transmissivity between the colors through the light transmitting medium, and  
ii) buffer means for **delaying any uncorrected gray scale signal related to the other colors for the time delay caused by said corrected gray scale data signal being corrected.**

**5. A method of gray scale data control for eliminating the effect wavelength dependency of transmissivity of light in a multicolor display cell comprising:**  
changing the level of gray scale data signals related to at least one of the multicolors supplied to the display cell to create a corrected gray scale data signal with a level different from the inputted gray scale data signal to compensate for differences in transmissivity of the colors that result from wavelength dependence, and synchronizing the output of the gray scale data signals by **delaying the output for at least one other of the multicolor by the time taken for correction of said at least one color to simultaneously output the gray scale data of all said multicolors.**

**LGD's Claim Construction**

**delaying any uncorrected gray scale signal related to the other colors for the time delay caused by said corrected gray scale data signal being corrected**<sup>1</sup> – holding or deferring at least on color video signal that is not subjected to a compensation value by the amount of time taken to modify another color video signal

**delaying the output for at least one other of the multicolor by the time taken for correction of said at least one color**<sup>2</sup> – holding or deferring the output of at least one color video signal that is not subject to a compensation value by the amount of time taken to modify another color video signal

<sup>1</sup> Disputed Term “delaying any uncorrected gray scale signal related to the other colors for the time delay caused by said corrected gray scale data signal being corrected ” also appears in asserted claim 1 in the same context.

<sup>2</sup> Disputed Term “delaying the output for at least one other of the multicolor by the time taken for correction of said at least one color ” also appears in asserted claim 5 in the same context.

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DELAYING ANY UNCORRECTED GRAY SCALE SIGNAL RELATED TO THE OTHER COLORS FOR THE TIME DELAY CAUSED BY SAID CORRECTED GRAY SCALE DATA SIGNAL BEING CORRECTED”:**

As an example of the second category (2), is a method in which the reference voltage (gray scale voltage) given to the data driver is tailored to the characteristics for each color. This method can compensate for the color dependency of the transmissivity/applied voltage characteristics. However, the circuits needed to independently control the reference voltages, raise the cost and cause difficulties in the implementation. Another method that falls within this second category, is to use the voltage for one of the colors of R/G/B as a reference voltage, and use offset voltages for each of other colors. This methods has the same problems as the method in which the reference voltages are separately applied, and in addition, cannot accomplish desired effect if the gradients of the curves showing the transmissivity/applied voltage characteristics of R/G/B vary with applied voltage. That is, in accordance with the offset voltage method, correction is carried out by applying a uniform offset voltage for all applied voltages, and thus the correction cannot be effectively performed unless the gradients of the curves showing the transmissivity/applied voltage characteristics are the same over the whole applied voltage range.

2:46-67

Japanese Published Unexamined Patent Application No. 01-101586 discloses a technique in which different liquid crystal driving voltage levels are set for each of the colors, and that level is applied to each pixel. Japanese Published Unexamined Patent Application No. 03-6986 discloses a technique in which the driving voltage is made to vary a predetermined voltage from color to color to obtain uniformity in transmissivity. Japanese Published Unexamined Patent Application No. 03-290618 discloses a technique in which a similar object is accomplished by independently inputting a gray scale control signal for each color.

3:1-11

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DELAYING ANY UNCORRECTED GRAY SCALE SIGNAL RELATED TO THE OTHER COLORS FOR THE TIME DELAY CAUSED BY SAID CORRECTED GRAY SCALE DATA SIGNAL BEING CORRECTED” (cont’d):**

Therefore, first object of the subject invention is to provide a driving method for a TFTLCD in which the dependency on color of the transmissivity/applied voltage characteristics is effectively corrected.

A second object of the subject invention is to realize the effective correction using a very simple method which enables the above described correction to be made without increase in complexity of the control method, and the restrictions on the implementation by addition of circuits.

2:46-67

**SUMMARY OF THE INVENTION**

In accordance with the present invention, the above described problems are solved by gray scale data (a bit string for a color liquid crystal display) wherein the data control means includes a computing circuit for performing an addition or subtraction of the gray scale related to at least one color to generate a corrected gray scale, and also includes delay means for delaying the outputting of the uncorrected gray scales, during the time which the gray scale of the one color is being corrected.

3:23-32

**PREFERRED EMBODIMENT**

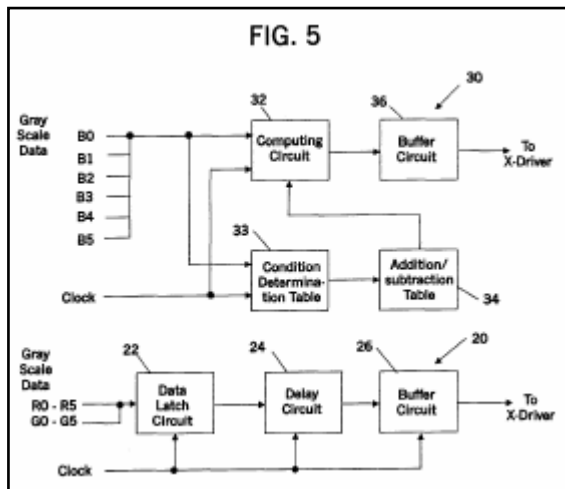
The subject invention can be realized by improving the data control unit 10 of FIG. 1 as is shown in FIG. 5. In the background art, the data control unit consists only of a latch and a buffer. However, in the subject invention, the gray

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scale data related to a color, that is to be corrected, is temporarily inputted to a computing circuit. An addition or subtraction operation is applied to that gray scale data to shift it by one or more gray scale levels, to thereby achieve transmissivity equivalent to the other colors which are not to be corrected.

3:63-4:6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DELAYING ANY UNCORRECTED GRAY SCALE SIGNAL RELATED TO THE OTHER COLORS FOR THE TIME DELAY CAUSED BY SAID CORRECTED GRAY SCALE DATA SIGNAL BEING CORRECTED” (cont’d):**



In FIG. 5, the color to be corrected is blue (B), and the colors which are not to be corrected are red (R) and green (G). The gray scale data related to R or G are shown by R0 to R5 or G0 to G5 in FIG. 5.

A portion 20 to which gray scale data related to R and G are inputted includes a data latch circuit 22 and a buffer circuit 26, like that in the data control unit in the background art. However, in addition to the data control unit in the background art, it includes a delay circuit 24. This is to compensate for the time during which the gray scale data B0 to B5 related to B is operated on by a computing circuit 32 in accordance with a condition determination table 36, as described later. The delay circuit 25 thereby assumes the outputting of the R and G gray scale data to the driver with the same timing as the corrected B gray scale data.

The gray data B0 to B5 for blue is a bit string for representing a 64-level gray scale. It is comprised of a bit string (B0, B1, B2, B3, B4, B5). For instance, if the gray scale is “4”, (B0, B1, B2, B3, B4, B5)=(001000), and if the gray scale is “28”, (B0, B1, B2, B3, B4, B5)=(001110). The same applied for R0 to R5 or G0 to G5 which are the gray scale data for red or green, respectively.

4:7-29

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DELAYING ANY UNCORRECTED GRAY SCALE SIGNAL RELATED TO THE OTHER COLORS FOR THE TIME DELAY CAUSED BY SAID CORRECTED GRAY SCALE DATA SIGNAL BEING CORRECTED” (cont’d):**

Gray Scale	Condition
0 - 3	A
4 - 10	B
11 - 53	C
54 - 60	B
61 - 63	A

FIG. 6

Further, the gray scale data for Blue is also supplied to a condition determination table 33. The condition determination table 33 determines the amount of the adjustment of the gray scale data. A diagrammatic representation of the condition determination table 33 is shown in FIG. 6. As shown, conditions A to C, corresponding to various gray scale levels, are set in the condition determination table 33. The

4:38-44

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DELAYING ANY UNCORRECTED GRAY SCALE SIGNAL RELATED TO THE OTHER COLORS FOR THE TIME DELAY CAUSED BY SAID CORRECTED GRAY SCALE DATA SIGNAL BEING CORRECTED” (cont’d):**

FIG. 7

Condition	Addition/ Subtraction Amount
A	0
B	-2
C	-4
⋮	⋮

levels, are set in the condition determination table 33. The condition corresponding to a gray scale is outputted from the condition determination table 33 to an addition/subtraction table 34. The addition/subtraction table 34 has the function of setting the actual amount of the addition or subtraction. A diagrammatic representation of the addition/subtraction table 34 is shown in FIG. 7. That is, the addition/subtraction tables set the amount to be added or subtracted according to the condition provided from the condition determination table 33. The amount of the addition or subtraction to correct the gray scale is supplied to the computing circuit 32.

The condition determination table 33 and the addition/subtraction table 34 can be implemented by software. The

4:45-56

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DELAYING ANY UNCORRECTED GRAY SCALE SIGNAL RELATED TO THE OTHER COLORS FOR THE TIME DELAY CAUSED BY SAID CORRECTED GRAY SCALE DATA SIGNAL BEING CORRECTED” (cont’d):**

Operation of the circuit 30 to which gray scale data for blue is inputted, and of the circuit 20 to which gray scale data related to Red and Green are inputted is as follows. When a gray scale level “2” is received, or (B0, B1, B2, B3, B4, B5)=(010000) is inputted, the input to the display is determined by the condition determination table 33. As shown in FIG. 6, in the condition determination table 33, the condition A is outputted to the addition/subtraction table 34, and thereafter, in the addition/subtraction table 34, “0” is outputted to the computing circuit as the addition or subtraction amount as shown in FIG. 7. Accordingly, the gray scale “2” is provided uncorrected to the X-driver via a buffer circuit 36. The above described processing causes a predetermined delay. Thus, the gray scale data for Red and Green corresponding to the gray scale data related to Blue are delayed for time taken for the processing by a delay circuit 24. As a result, the gray scale data related to B is outputted from the buffer circuit 36 to the X-driver is synchronized with the gray scale data for Red and Green for simultaneous output from the buffer circuit 26 to the X-driver.

Where the gray scale data level is “20,” or the grey scale level signal (B0, B1, B2, B3, B4, B5)=(001010), the condition determination table 33 provides condition C signal to the addition/subtraction table 34 as shown in FIG. 6. In response, the addition/subtraction table 34 provides a signal to the computing circuit to subtract four grey scale levels (the amount as shown as -4 in FIG. 7). Accordingly, the gray scale level “20” is corrected by the computing circuit 32 to a gray scale level “16”(20-4=16) which level is provided to the X-driver via the buffer circuit 36. In this way, corrections are made to the transmissivity/applied voltage characteristics where, as shown in FIG. 3, they are not uniform for each color.

5:10-43

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DELAYING ANY UNCORRECTED GRAY SCALE SIGNAL RELATED TO THE OTHER COLORS FOR THE TIME DELAY CAUSED BY SAID CORRECTED GRAY SCALE DATA SIGNAL BEING CORRECTED” (cont’d):**

The claims in the application are rejected under 35 USC §103(a) as being unpatentable over Kennedy in view of Kanie et al. The Examiner points out that the Kennedy patent fails to teach the use of a buffer to eliminate phase shifts in color transmission. From what the applicants' attorney can see, there is a reason for this. There is no apparent delay of the gray scale levels from one color relative to the other colors resulting from the gray scale signals being transmitted through the apparatus of Kennedy. Each of the R, G & B channels in Kennedy is subjected to the same correction. Therefore, there is no need to delay the gray scale data of one relative to another. In fact, such a delay, with respect to one color, would be detrimental since it would skew the timing of information for that one color relative to the other colors. The purpose of the apparatus in the Kennedy patent is to make the incoming gray scale signals each conform to the same standard binary range of 000 (lowest intensity) to 111 (maximum intensity). The purpose of the present invention is to vary the level of at least one of the gray scale signals relative to the other gray scale signals to compensate for differences in transmissivity through the display device.

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**INTRINSIC EVIDENCE FOR DISPUTED TERM “DELAYING ANY UNCORRECTED GRAY SCALE SIGNAL RELATED TO THE OTHER COLORS FOR THE TIME DELAY CAUSED BY SAID CORRECTED GRAY SCALE DATA SIGNAL BEING CORRECTED” (cont’d):**

Reasons for allowance	
1.	Claims 1-13 are allowed.
2.	The following is an examiner's statement of reasons for allowance:
	None of the references, either singularly or in combination, teach or fairly suggests:
	<i>A liquid crystal color display comprising:</i>
a)	<i>a display cell containing a light transmitting medium,</i>
b)	<i>driver means connected to said display cell for driving the display cell with sets of gray scale data signals each signal for a different color, and</i>
c)	<i>data control means for receiving gray scale data signals related to the setting of a gray scale for the display cell and outputting said gray scale data signals to said driver with a predetermined timing, wherein said data control means includes:</i>
i)	<i>computing means for changing the level of the gray scale data signals for at least one color relative to the other colors to a different gray scale level to compensate for a variation in intensity between the colors due to wavelength related differences in transmissivity between the colors through the light transmitting medium, and</i>
ii)	<i>buffer means for delaying any uncorrected gray scale signal related to the other colors for the time delay caused by said corrected gray scale data signal being corrected.</i>

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**INTRINSIC EVIDENCE FOR DISPUTED TERM “DELAYING THE OUTPUT FOR AT LEAST ONE OTHER OF THE MULTICOLOR BY THE TIME TAKEN FOR CORRECTION OF SAID AT LEAST ONE COLOR”:**

As an example of the second category (2), is a method in which the reference voltage (gray scale voltage) given to the data driver is tailored to the characteristics for each color. This method can compensate for the color dependency of the transmissivity/applied voltage characteristics. However, the circuits needed to independently control the reference voltages, raise the cost and cause difficulties in the implementation. Another method that falls within this second category, is to use the voltage for one of the colors of R/G/B as a reference voltage, and use offset voltages for each of other colors. This methods has the same problems as the method in which the reference voltages are separately applied, and in addition, cannot accomplish desired effect if the gradients of the curves showing the transmissivity/applied voltage characteristics of R/G/B vary with applied voltage. That is, in accordance with the offset voltage method, correction is carried out by applying a uniform offset voltage for all applied voltages, and thus the correction cannot be effectively performed unless the gradients of the curves showing the transmissivity/applied voltage characteristics are the same over the whole applied voltage range.

2:46-67

Japanese Published Unexamined Patent Application No. 01-101586 discloses a technique in which different liquid crystal driving voltage levels are set for each of the colors, and that level is applied to each pixel. Japanese Published Unexamined Patent Application No. 03-6986 discloses a technique in which the driving voltage is made to vary a predetermined voltage from color to color to obtain uniformity in transmissivity. Japanese Published Unexamined Patent Application No. 03-290618 discloses a technique in which a similar object is accomplished by independently inputting a gray scale control signal for each color.

3:1-11

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DELAYING THE OUTPUT FOR AT LEAST ONE OTHER OF THE MULTICOLOR BY THE TIME TAKEN FOR CORRECTION OF SAID AT LEAST ONE COLOR” (cont’d):**

Therefore, first object of the subject invention is to provide a driving method for a TFTLCD in which the dependency on color of the transmissivity/applied voltage characteristics is effectively corrected.

A second object of the subject invention is to realize the effective correction using a very simple method which enables the above described correction to be made without increase in complexity of the control method, and the restrictions on the implementation by addition of circuits.

**SUMMARY OF THE INVENTION**

In accordance with the present invention, the above described problems are solved by gray scale data (a bit string for a color liquid crystal display) wherein the data control means includes a computing circuit for performing an addition or subtraction of the gray scale related to at least one color to generate a corrected gray scale, and also includes delay means for delaying the outputting of the uncorrected gray scales, during the time which the gray scale of the one color is being corrected.

3:12-32

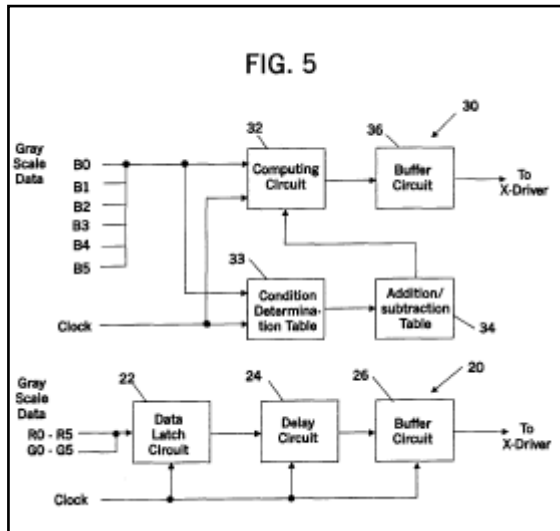
**PREFERRED EMBODIMENT**

The subject invention can be realized by improving the data control unit **10** of FIG. 1 as is shown in FIG. 5. In the background art, the data control unit consists only of a latch and a buffer. However, in the subject invention, the gray

scale data related to a color, that is to be corrected, is temporarily inputted to a computing circuit. An addition or subtraction operation is applied to that gray scale data to shift it by one or more gray scale levels, to thereby achieve transmissivity equivalent to the other colors which are not to be corrected.

3:63-4:6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DELAYING THE OUTPUT FOR AT LEAST ONE OTHER OF THE MULTICOLOR BY THE TIME TAKEN FOR CORRECTION OF SAID AT LEAST ONE COLOR” (cont’d):**



In FIG. 5, the color to be corrected is blue (B), and the colors which are not to be corrected are red (R) and green (G). The gray scale data related to R or G are shown by R0 to R5 or G0 to G5 in FIG. 5.

A portion 20 to which gray scale data related to R and G are inputted includes a data latch circuit 22 and a buffer circuit 26, like that in the data control unit in the background art. However, in addition to the data control unit in the background art, it includes a delay circuit 24. This is to compensate for the time during which the gray scale data B0 to B5 related to B is operated on by a computing circuit 32 in accordance with a condition determination table 36, as described later. The delay circuit 25 thereby assumes the outputting of the R and G gray scale data to the driver with the same timing as the corrected B gray scale data.

The gray data B0 to B5 for blue is a bit string for representing a 64-level gray scale. It is comprised of a bit string (B0, B1, B2, B3, B4, B5). For instance, if the gray scale is “4”, (B0, B1, B2, B3, B4, B5)=(001000), and if the gray scale is “28”, (B0, B1, B2, B3, B4, B5)=(001110). The same applied for R0 to R5 or G0 to G5 which are the gray scale data for red or green, respectively.

4:7-29

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DELAYING THE OUTPUT FOR AT LEAST ONE OTHER OF THE MULTICOLOR BY THE TIME TAKEN FOR CORRECTION OF SAID AT LEAST ONE COLOR” (cont’d):**

Gray Scale	Condition	FIG. 6
0 - 3	A	
4 - 10	B	
11 - 53	C	
54 - 60	B	
61 - 63	A	

Further, the gray scale data for Blue is also supplied to a condition determination table 33. The condition determination table 33 determines the amount of the adjustment of the gray scale data. A diagrammatic representation of the condition determination table 33 is shown in FIG. 6. As shown, conditions A to C, corresponding to various gray scale levels, are set in the condition determination table 33. The

4:38-43

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DELAYING THE OUTPUT FOR AT LEAST ONE OTHER OF THE MULTICOLOR BY THE TIME TAKEN FOR CORRECTION OF SAID AT LEAST ONE COLOR” (cont’d):**

FIG. 7

Condition	Addition/ Subtraction Amount
A	0
B	-2
C	-4
⋮	⋮

levels, are set in the condition determination table 33. The condition corresponding to a gray scale is outputted from the condition determination table 33 to an addition/subtraction table 34. The addition/subtraction table 34 has the function of setting the actual amount of the addition or subtraction. A diagrammatic representation of the addition/subtraction table 34 is shown in FIG. 7. That is, the addition/subtraction tables set the amount to be added or subtracted according to the condition provided from the condition determination table 33. The amount of the addition or subtraction to correct the gray scale is supplied to the computing circuit 32.

The condition determination table 33 and the addition/subtraction table 34 can be implemented by software. The

4:44-57

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DELAYING THE OUTPUT FOR AT LEAST ONE OTHER OF THE MULTICOLOR BY THE TIME TAKEN FOR CORRECTION OF SAID AT LEAST ONE COLOR” (cont’d):**

Operation of the circuit 30 to which gray scale data for blue is inputted, and of the circuit 20 to which gray scale data related to Red and Green are inputted is as follows. When a gray scale level “2” is received, or (B0, B1, B2, B3, B4, B5)=(010000) is inputted, the input to the display is determined by the condition determination table 33. As shown in FIG. 6, in the condition determination table 33, the condition A is outputted to the addition/subtraction table 34, and thereafter, in the addition/subtraction table 34, “0” is outputted to the computing circuit as the addition or subtraction amount as shown in FIG. 7. Accordingly, the gray scale “2” is provided unconnected to the X-driver via a buffer circuit 36. The above described processing causes a predetermined delay. Thus, the gray scale data for Red and Green corresponding to the gray scale data related to Blue are delayed for time taken for the processing by a delay circuit 24. As a result, the gray scale data related to B is outputted from the buffer circuit 36 to the X-driver is synchronized with the gray scale data for Red and Green for simultaneous output from the buffer circuit 26 to the X-driver.

Where the gray scale data level is “20,” or the grey scale level signal (B0, B1, B2, B3, B4, B5)=(001010), the condition determination table 33 provides condition C signal to the addition/subtraction table 34 as shown in FIG. 6. In response, the addition/subtraction table 34 provides a signal to the computing circuit to subtract four grey scale levels (the amount as shown as -4 in FIG. 7). Accordingly, the gray scale level “20” is corrected by the computing circuit 32 to a gray scale level “16”(20-4=16) which level is provided to the X-driver via the buffer circuit 36. In this way, corrections are made to the transmissivity/applied voltage characteristics where, as shown in FIG. 3, they are not uniform for each color.

5:11-43

With the method of the subject invention, only an additional circuit such as a computing circuit, is needed to effectively correct the differences in the transmissivity/applied voltage characteristics for colors. The above correction is made while avoiding the problems in complexity of control methods in the background art. That is, to implement

5:58-63

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DELAYING THE OUTPUT FOR AT LEAST ONE OTHER OF THE MULTICOLOR BY THE TIME TAKEN FOR CORRECTION OF SAID AT LEAST ONE COLOR” (cont’d):**

The claims in the application are rejected under 35 USC §103(a) as being unpatentable over Kennedy in view of Kanie et al. The Examiner points out that the Kennedy patent fails to teach the use of a buffer to eliminate phase shifts in color transmission. From what the applicants' attorney can see, there is a reason for this. There is no apparent delay of the gray scale levels from one color relative to the other colors resulting from the gray scale signals being transmitted through the apparatus of Kennedy. Each of the R, G & B channels in Kennedy is subjected to the same correction. Therefore, there is no need to delay the gray scale data of one relative to another. In fact, such a delay, with respect to one color, would be detrimental since it would skew the timing of information for that one color relative to the other colors. The purpose of the apparatus in the Kennedy patent is to make the incoming gray scale signals each conform to the same standard binary range of 000 (lowest intensity) to 111 (maximum intensity). The purpose of the present invention is to vary the level of at least one of the gray scale signals relative to the other gray scale signals to compensate for differences in transmissivity through the display device.

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**INTRINSIC EVIDENCE FOR DISPUTED TERM “DELAYING THE OUTPUT FOR AT LEAST ONE OTHER OF THE MULTICOLOR BY THE TIME TAKEN FOR CORRECTION OF SAID AT LEAST ONE COLOR”:**

Reasons for allowance	
1.	Claims 1-13 are allowed.
2.	The following is an examiner's statement of reasons for allowance:
	None of the references, either singularly or in combination, teach or fairly suggests:
	<i>A liquid crystal color display comprising:</i>
a)	<i>a display cell containing a light transmitting medium,</i>
b)	<i>driver means connected to said display cell for driving the display cell with sets of gray scale data signals each signal for a different color, and</i>
c)	<i>data control means for receiving gray scale data signals related to the setting of a gray scale for the display cell and outputting said gray scale data signals to said driver with a predetermined timing, wherein said data control means includes:</i>
i)	<i>computing means for changing the level of the gray scale data signals for at least one color relative to the other colors to a different gray scale level to compensate for a variation in intensity between the colors due to wavelength related differences in transmissivity between the colors through the light transmitting medium, and</i>
ii)	<i>buffer means for delaying any uncorrected gray scale signal related to the other colors for the time delay caused by said corrected gray scale data signal being corrected.</i>

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**EXHIBIT S**  
**U.S. PATENT NO. 6,008,786**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 7**

7. A liquid crystal multicolor display comprising:  
a) display cells containing a light transmitting medium,  
b) driver circuits connected to said display cells for driving the display cells with sets of gray scale data signals each driver circuit for a different one of the colors,

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- i) calculation logic in the driver circuit of at least one color for changing the level of the gray scale data signals of said at least one color to a different gray scale level to compensate for color distortion due to wavelength related differences in transmissivity between the colors through the light transmitting medium, and
- ii) delay logic in the driver circuit for any other of the colors without the calculation logic in its driver circuit for delaying the gray scale signals for the other of the colors to synchronize the provision of the sets of gray scale data signals by compensating for the delay caused by the calculation logic.

**LGD's Claim Construction**

**driver circuit for any other of the colors without the calculation logic in its driver circuit**<sup>1</sup> – at least one color video signal path that does not include calculation logic

**delaying the gray scale signals for the other of the colors**<sup>2</sup> – holding or deferring the output of the unmodified color video signals

<sup>1</sup> Disputed Term “driver circuit for any other of the colors without the calculation logic in its driver circuit ” also appears in asserted claim 7 in the same context.

<sup>2</sup> Disputed Term “delaying the gray scale signals for the other of the colors ” also appears in asserted claim 7 in the same context.

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “DRIVER CIRCUIT FOR ANY OTHER OF THE COLORS WITHOUT THE CALCULATION LOGIC IN ITS DRIVER CIRCUIT” AND “DELAYING THE GRAY SCALE SIGNALS FOR THE OTHER OF THE COLORS”:**

The claims in the application are rejected under 35 USC §103(a) as being unpatentable over Kennedy in view of Kanie et al. The Examiner points out that the Kennedy patent fails to teach the use of a buffer to eliminate phase shifts in color transmission. From what the applicants' attorney can see, there is a reason for this. There is no apparent delay of the gray scale levels from one color relative to the other colors resulting from the gray scale signals being transmitted through the apparatus of Kennedy. Each of the R, G & B channels in Kennedy is subjected to the same correction. Therefore, there is no need to delay the gray scale data of one relative to another. In fact, such a delay, with respect to one color, would be detrimental since it would skew the timing of information for that one color relative to the other colors. The purpose of the apparatus in the Kennedy patent is to make the incoming gray scale signals each conform to the same standard binary range of 000 (lowest intensity) to 111 (maximum intensity). The purpose of the present invention is to vary the level of at least one of the gray scale signals relative to the other gray scale signals to compensate for differences in transmissivity through the display device.

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**INTRINSIC EVIDENCE FOR DISPUTED TERMS “DRIVER CIRCUIT FOR ANY OTHER OF THE COLORS WITHOUT THE CALCULATION LOGIC IN ITS DRIVER CIRCUIT” AND “DELAYING THE GRAY SCALE SIGNALS FOR THE OTHER OF THE COLORS” (cont’d):**

Reasons for allowance	
1.	Claims 1-13 are allowed.
2.	The following is an examiner's statement of reasons for allowance:
	None of the references, either singularly or in combination, teach or fairly suggests:
	<i>A liquid crystal color display comprising:</i>
a)	<i>a display cell containing a light transmitting medium,</i>
b)	<i>driver means connected to said display cell for driving the display cell with sets of gray scale data signals each signal for a different color, and</i>
c)	<i>data control means for receiving gray scale data signals related to the setting of a gray scale for the display cell and outputting said gray scale data signals to said driver with a predetermined timing, wherein said data control means includes:</i>
i)	<i>computing means for changing the level of the gray scale data signals for at least one color relative to the other colors to a different gray scale level to compensate for a variation in intensity between the colors due to wavelength related differences in transmissivity between the colors through the light transmitting medium, and</i>
ii)	<i>buffer means for delaying any uncorrected gray scale signal related to the other colors for the time delay caused by said corrected gray scale data signal being corrected.</i>

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**EXHIBIT S**  
**U.S. PATENT NO. 6,008,786**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 12**

**12.** A method of gray scale data control for reducing the effect wavelength dependency on transmissivity of light in cells of a multicolor display comprising:

changing the gray scale data signals related to one of the multicolors to correct for the wavelength dependency of transmissivity and thereby create a corrected gray scale data signal different from the inputted gray scale data signal for that color, and synchronizing the timing of the gray scale data signals by **delaying the output for any other color of the multicolors with gray scale data signals not subject to a correction by the amount of time taken for correction of the one color** to synchronize the timing of the gray scale data signals for all said multicolors.

**LGD's Claim Construction**

**delaying the output for any other color of the multicolors with gray scale data signals not subject to a correction by the amount of time taken for correction of the one color**<sup>1</sup> – holding or deferring the output of the remaining color video signals that are not subject to compensations values by the amount of time taken to modify the one color video signal

<sup>1</sup> Disputed Term “delaying the output for any other color of the multicolors with gray scale data signals not subject to a correction by the amount of time taken for correction of the one color ” also appears in asserted claim 12 in the same context.

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DELAYING THE OUTPUT FOR ANY OTHER COLOR OF THE MULTICOLORS WITH GRAY SCALE DATA SIGNALS NOT SUBJECT TO A CORRECTION BY THE AMOUNT OF TIME TAKEN FOR CORRECTION OF THE ONE COLOR”:**

The Claims in the application are rejected under 35 USC §103(a) as being unpatentable over Kennedy in view of Kanie et al. The Examiner points out that the Kennedy patent fails to teach the use of a buffer to eliminate phase shifts in color transmission. From what the applicants' attorney can see, there is a reason for this. There is no apparent delay of the gray scale levels from one color relative to the other colors resulting from the gray scale signals being transmitted through the apparatus of Kennedy. Each of the R, G & B channels in Kennedy is subjected to the same correction. Therefore, there is no need to delay the gray scale data of one relative to another. In fact, such a delay, with respect to one color, would be detrimental since it would skew the timing of information for that one color relative to the other colors. The purpose of the apparatus in the Kennedy patent is to make the incoming gray scale signals each conform to the same standard binary range of 000 (lowest intensity) to 111 (maximum intensity). The purpose of the present invention is to vary the level of at least one of the gray scale signals relative to the other gray scale signals to compensate for differences in transmissivity through the display device.

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**INTRINSIC EVIDENCE FOR DISPUTED TERM “DELAYING THE OUTPUT FOR ANY OTHER COLOR OF THE MULTICOLORS WITH GRAY SCALE DATA SIGNALS NOT SUBJECT TO A CORRECTION BY THE AMOUNT OF TIME TAKEN FOR CORRECTION OF THE ONE COLOR” (cont’d):**

Reasons for allowance	
1.	Claims 1-13 are allowed.
2.	The following is an examiner's statement of reasons for allowance:
	None of the references, either singularly or in combination, teach or fairly suggests:
	<i>A liquid crystal color display comprising:</i>
a)	<i>a display cell containing a light transmitting medium,</i>
b)	<i>driver means connected to said display cell for driving the display cell with sets of gray scale data signals each signal for a different color, and</i>
c)	<i>data control means for receiving gray scale data signals related to the setting of a gray scale for the display cell and outputting said gray scale data signals to said driver with a predetermined timing, wherein said data control means includes:</i>
i)	<i>computing means for changing the level of the gray scale data signals for at least one color relative to the other colors to a different gray scale level to compensate for a variation in intensity between the colors due to wavelength related differences in transmissivity between the colors through the light transmitting medium, and</i>
ii)	<i>buffer means for delaying any uncorrected gray scale signal related to the other colors for the time delay caused by said corrected gray scale data signal being corrected.</i>

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**EXHIBIT S**  
**U.S. PATENT NO. 6,008,786**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 5**

**5.** A method of gray scale data control for eliminating the effect wavelength dependency of transmissivity of light in a multicolor display cell comprising:

changing the level of gray scale data signals related to at least one of the multicolors supplied to the display cell to create a corrected gray scale data signal with a level different from the inputted gray scale data signal to compensate for differences in transmissivity of the colors that result from wavelength dependence, and synchronizing the output of the gray scale data signals by delaying the output for at least one other of the multicolor by the time taken for correction of said at least one color to **simultaneously output the gray scale data of all said multicolors.**

**ASSERTED CLAIM 5**

**12.** A method of gray scale data control for reducing the effect wavelength dependency on transmissivity of light in cells of a multicolor display comprising:

changing the gray scale data signals related to one of the multicolors to correct for the wavelength dependency of transmissivity and thereby create a corrected gray scale data signal different from the inputted gray scale data signal for that color, and synchronizing the timing of the gray scale data signals by delaying the output for any other color of the multicolors with gray scale data signals not subject to a correction by the amount of time taken for correction of the one color to **synchronize the timing of the gray scale data signals for all said multicolors.**

**LGD's Claim Construction**

**simultaneously output the gray scale data of all said multicolors**<sup>1</sup> – provides all multicolor gray scale data to the data driver during the same predetermined time interval

**synchronize the timing of the gray scale data signals for all said multicolors**<sup>2</sup> – provides all multicolor gray scale data signals to the data driver during the same predetermined time interval

<sup>1</sup> Disputed Term “simultaneously output the gray scale data of all said multicolors ” also appears in asserted claim 5 in the same context.

<sup>2</sup> Disputed Term “synchronize the timing of the gray scale data signals for all said multicolors ” also appears in asserted claim 12 in the same context.

**INTRINSIC EVIDENCE FOR DISPUTED TERM “SIMULTANEOUSLY OUTPUT THE GRAY SCALE DATA OF ALL SAID MULTICOLORS” :**

In using TFTLCDs to display pictures, it is necessary to provide gray scale data of the picture to the LCD to drive the LCD. FIG. 1 shows the construction of the control unit of the TFTLCD. The array/cell portion 1 of the LCD is connected to an X-driver 3 and a Y-driver 5. The X-driver 3, when it is supplied with gray scale data, applies a voltage corresponding to the gray scale data to the cell. The Y-driver 5 is connected to the gate of a switching element, and conducts/does not conduct the voltage applied to the cell by the X-driver 3 at a predetermined time.

Gray scale data is supplied to the X-driver by data control unit 10. The data control unit 10 consists of a data control circuit 12 for latching and storing the externally supplied R/G/B data in a buffer, and a timing control circuit 14 for outputting the gray scale data stored in the buffer to the X-driver 3 at a predetermined time. A clock signal is externally supplied to the data control circuit 12 and the timing control circuit 14 to control the timing. A power supply 7 is connected to the X-driver, Y-driver 5, and data control unit 10.

1:26-45

As an example of the second category (2), is a method in which the reference voltage (gray scale voltage) given to the data driver is tailored to the characteristics for each color. This method can compensate for the color dependency of the transmissivity/applied voltage characteristics. However, the circuits needed to independently control the reference voltages, raise the cost and cause difficulties in the implementation. Another method that falls within this second category, is to use the voltage for one of the colors of R/G/B as a reference voltage, and use offset voltages for each of other colors. This methods has the same problems as the method in which the reference voltages are separately applied, and in addition, cannot accomplish desired effect if the gradients of the curves showing the transmissivity/applied voltage characteristics of R/G/B vary with applied voltage. That is, in accordance with the offset voltage method, correction is carried out by applying a uniform offset voltage for all applied voltages, and thus the correction cannot be effectively performed unless the gradients of the curves showing the transmissivity/applied voltage characteristics are the same over the whole applied voltage range.

2:46-67

**INTRINSIC EVIDENCE FOR DISPUTED TERM “SIMULTANEOUSLY OUTPUT THE GRAY SCALE DATA OF ALL SAID MULTICOLORS” (cont’d):**

Japanese Published Unexamined Patent Application No. 01-101586 discloses a technique in which different liquid crystal driving voltage levels are set for each of the colors, and that level is applied to each pixel. Japanese Published Unexamined Patent Application No. 03-6986 discloses a technique in which the driving voltage is made to vary a predetermined voltage from color to color to obtain uniformity in transmissivity. Japanese Published Unexamined Patent Application No. 03-290618 discloses a technique in which a similar object is accomplished by independently inputting a gray scale control signal for each color.

Therefore, first object of the subject invention is to provide a driving method for a TFTLCD in which the dependency on color of the transmissivity/applied voltage characteristics is effectively corrected.

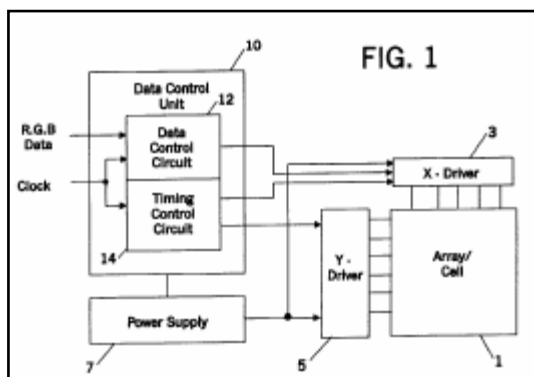
A second object of the subject invention is to realize the effective correction using a very simple method which enables the above described correction to be made without increase in complexity of the control method, and the restrictions on the implementation by addition of circuits.

**SUMMARY OF THE INVENTION**

In accordance with the present invention, the above described problems are solved by gray scale data (a bit string for a color liquid crystal display) wherein the data control means includes a computing circuit for performing an addition or subtraction of the gray scale related to at least one color to generate a corrected gray scale, and also includes delay means for delaying the outputting of the uncorrected gray scales, during the time which the gray scale of the one color is being corrected.

3:1-32

**INTRINSIC EVIDENCE FOR DISPUTED TERM “SIMULTANEOUSLY  
OUTPUT THE GRAY SCALE DATA OF ALL SAID  
MULTICOLORS” (cont’d):**



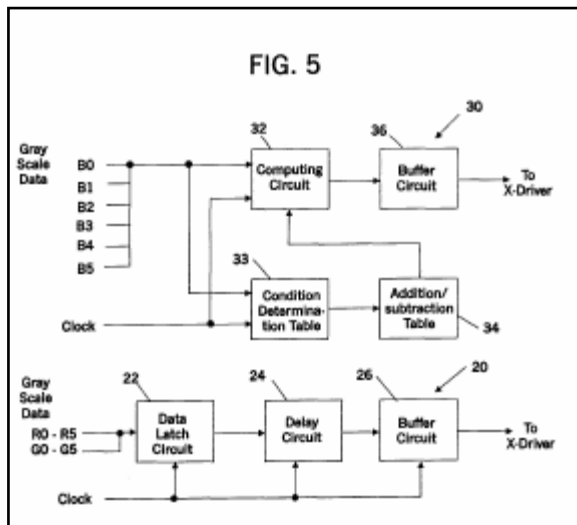
**PREFERRED EMBODIMENT**

The subject invention can be realized by improving the data control unit **10** of FIG. 1 as is shown in FIG. 5. In the background art, the data control unit consists only of a latch and a buffer. However, in the subject invention, the gray

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scale data related to a color, that is to be corrected, is temporarily inputted to a computing circuit. An addition or subtraction operation is applied to that gray scale data to shift it by one or more gray scale levels, to thereby achieve transmissivity equivalent to the other colors which are not to be corrected.

3:62-4:6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “SIMULTANEOUSLY  
OUTPUT THE GRAY SCALE DATA OF ALL SAID  
MULTICOLORS” (cont’d):**



In FIG. 5, the color to be corrected is blue (B), and the colors which are not to be corrected are red (R) and green (G). The gray scale data related to R or G are shown by R0 to R5 or G0 to G5 in FIG. 5.

A portion 20 to which gray scale data related to R and G are inputted includes a data latch circuit 22 and a buffer circuit 26, like that in the data control unit in the background art. However, in addition to the data control unit in the background art, it includes a delay circuit 24. This is to compensate for the time during which the gray scale data B0 to B5 related to B is operated on by a computing circuit 32 in accordance with a condition determination table 36, as described later. The delay circuit 25 thereby assumes the outputting of the R and G gray scale data to the driver with the same timing as the corrected B gray scale data.

The gray data B0 to B5 for blue is a bit string for representing a 64-level gray scale. It is comprised of a bit string (B0, B1, B2, B3, B4, B5). For instance, if the gray scale is “4”, (B0, B1, B2, B3, B4, B5)=(001000), and if the gray scale is “28”, (B0, B1, B2, B3, B4, B5)=(001110). The same applied for R0 to R5 or G0 to G5 which are the gray scale data for red or green, respectively.

4:7-29

**INTRINSIC EVIDENCE FOR DISPUTED TERM “SIMULTANEOUSLY  
OUTPUT THE GRAY SCALE DATA OF ALL SAID  
MULTICOLORS” (cont’d):**

Gray Scale	Condition
0 - 3	A
4 - 10	B
11 - 53	C
54 - 60	B
61 - 63	A

FIG. 6

Further, the gray scale data for Blue is also supplied to a condition determination table 33. The condition determination table 33 determines the amount of the adjustment of the gray scale data. A diagrammatic representation of the condition determination table 33 is shown in FIG. 6. As shown, conditions A to C, corresponding to various gray scale levels, are set in the condition determination table 33. The

4:38-44

**INTRINSIC EVIDENCE FOR DISPUTED TERM “SIMULTANEOUSLY OUTPUT THE GRAY SCALE DATA OF ALL SAID MULTICOLORS” (cont’d):**

FIG. 7

Condition	Addition/ Subtraction Amount
A	0
B	-2
C	-4
⋮	⋮

levels, are set in the condition determination table 33. The condition corresponding to a gray scale is outputted from the condition determination table 33 to an addition/subtraction table 34. The addition/subtraction table 34 has the function of setting the actual amount of the addition or subtraction. A diagrammatic representation of the addition/subtraction table 34 is shown in FIG. 7. That is, the addition/subtraction tables set the amount to be added or subtracted according to the condition provided from the condition determination table 33. The amount of the addition or subtraction to correct the gray scale is supplied to the computing circuit 32.

The condition determination table 33 and the addition/subtraction table 34 can be implemented by software. The

4:45-57

**INTRINSIC EVIDENCE FOR DISPUTED TERM “SIMULTANEOUSLY OUTPUT THE GRAY SCALE DATA OF ALL SAID MULTICOLORS” (cont’d):**

Where the gray scale data level is “20,” or the grey scale level signal (B0, B1, B2, B3, B4, B5)=(001010), the condition determination table 33 provides condition C signal to the addition/subtraction table 34 as shown in FIG. 6. In response, the addition/subtraction table 34 provides a signal to the computing circuit to subtract four grey scale levels (the amount as shown as -4 in FIG. 7). Accordingly, the gray scale level “20” is corrected by the computing circuit 32 to a gray scale level “16”(20-4=16) which level is provided to the X-driver via the buffer circuit 36. In this way, corrections are made to the transmissivity/applied voltage characteristics where, as shown in FIG. 3, they are not uniform for each color.

5:11-29

Operation of the circuit 30 to which gray scale data for blue is inputted, and of the circuit 20 to which gray scale data related to Red and Green are inputted is as follows. When a gray scale level “2” is received, or (B0, B1, B2, B3, B4, B5)=(010000) is inputted, the input to the display is determined by the condition determination table 33. As shown in FIG. 6, in the condition determination table 33, the condition A is outputted to the addition/subtraction table 34, and thereafter, in the addition/subtraction table 34, “0” is outputted to the computing circuit as the addition or subtraction amount as shown in FIG. 7. Accordingly, the gray scale “2” is provided unconnected to the X-driver via a buffer circuit 36. The above described processing causes a predetermined delay. Thus, the gray scale data for Red and Green corresponding to the gray scale data related to Blue are delayed for time taken for the processing by a delay circuit 24. As a result, the gray scale data related to B is outputted from the buffer circuit 36 to the X-driver is synchronized with the gray scale data for Red and Green for simultaneous output from the buffer circuit 26 to the X-driver.

5:30-43

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “SIMULTANEOUSLY OUTPUT THE GRAY SCALE DATA OF ALL SAID MULTICOLORS” AND “SYNCHRONIZE THE TIMING OF THE GRAY SCALE DATA SIGNALS FOR ALL SAID MULTICOLORS”:**

The Claims in the application are rejected under 35 USC §103(a) as being unpatentable over Kennedy in view of Kanie et al. The Examiner points out that the Kennedy patent fails to teach the use of a buffer to eliminate phase shifts in color transmission. From what the applicants' attorney can see, there is a reason for this. There is no apparent delay of the gray scale levels from one color relative to the other colors resulting from the gray scale signals being transmitted through the apparatus of Kennedy. Each of the R, G & B channels in Kennedy is subjected to the same correction. Therefore, there is no need to delay the gray scale data of one relative to another. In fact, such a delay, with respect to one color, would be detrimental since it would skew the timing of information for that one color relative to the other colors. The purpose of the apparatus in the Kennedy patent is to make the incoming gray scale signals each conform to the same standard binary range of 000 (lowest intensity) to 111 (maximum intensity). The purpose of the present invention is to vary the level of at least one of the gray scale signals relative to the other gray scale signals to compensate for differences in transmissivity through the display device.

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**INTRINSIC EVIDENCE FOR DISPUTED TERMS “SIMULTANEOUSLY OUTPUT THE GRAY SCALE DATA OF ALL SAID MULTICOLORS” AND “SYNCHRONIZE THE TIMING OF THE GRAY SCALE DATA SIGNALS FOR ALL SAID MULTICOLORS” (cont’d):**

Reasons for allowance	
1.	Claims 1-13 are allowed.
2.	The following is an examiner's statement of reasons for allowance:
	None of the references, either singularly or in combination, teach or fairly suggests:
	<i>A liquid crystal color display comprising:</i>
a)	<i>a display cell containing a light transmitting medium,</i>
b)	<i>driver means connected to said display cell for driving the display cell with sets of gray scale data signals each signal for a different color, and</i>
c)	<i>data control means for receiving gray scale data signals related to the setting of a gray scale for the display cell and outputting said gray scale data signals to said driver with a predetermined timing, wherein said data control means includes:</i>
i)	<i>computing means for changing the level of the gray scale data signals for at least one color relative to the other colors to a different gray scale level to compensate for a variation in intensity between the colors due to wavelength related differences in transmissivity between the colors through the light transmitting medium, and</i>
ii)	<i>buffer means for delaying any uncorrected gray scale signal related to the other colors for the time delay caused by said corrected gray scale data signal being corrected.</i>

App. 08/832,640; 07/19/1999 Office  
Action; pg. 2

**EXHIBIT S**  
**U.S. PATENT NO. 6,008,786**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 1**

1. A liquid crystal color display comprising:  
a) a display cell containing a light transmitting medium,  
b) **driver means** connected to said display cell for driving the display cell with sets of grey scale data signals each signal for a different color, and  
c) **data control means** for receiving gray scale data signals related to the setting of a gray scale for the display cell and outputting said gray scale data signals to said driver with a predetermined timing, wherein said data control means includes:  
i) computing means for changing the level of the gray scale data signals for at least one color relative to the other colors to a different gray scale level to compensate for a variation in intensity between the colors due to wavelength related differences in transmissivity between the colors through the light transmitting medium, and  
ii) buffer means for delaying any uncorrected gray scale signal related to the other colors for the time delay caused by said corrected gray scale data signal being corrected.

**ASSERTED CLAIM 3**

3. A liquid crystal color display of claim 1 wherein: said adjusting means is for the **data control means** to simultaneously output the corrected and uncorrected gray scale data signals.

**LGD's Claim Construction**

**driver means**<sup>1</sup> - Interpreted per 35 USC §112 ¶6.

*function:* driving the display cell with sets of grey scale data signals.

*structure:* Fig. 1, element 3.

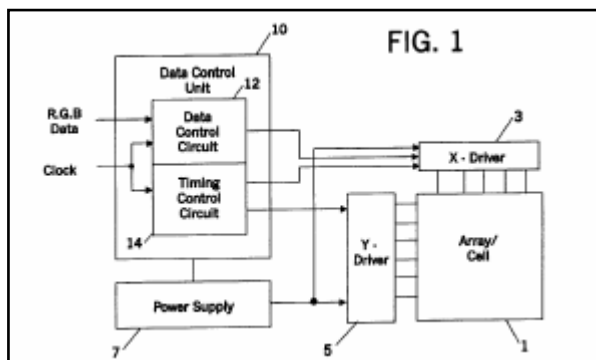
**data control means**<sup>2</sup> – Interpreted per 35 USC §112¶6.

*function:* receiving gray scale data signals related to the setting of a gray scale for the display cell and outputting said gray scale data signals to said driver with a predetermined timing.

*structure:* Fig. 5, all elements; Figs. 6-8.

<sup>1-2</sup> Disputed Terms “driver means & data control means” also appears in asserted claims 1 & 3 in the same context.

## INTRINSIC EVIDENCE FOR DISPUTED TERM “DRIVER MEANS”:



The subject invention can be realized by improving the data control unit 10 of FIG. 1 as is shown in FIG. 5. In the background art, the data control unit consists only of a latch and a buffer. However, in the subject invention, the gray scale data related to a color, that is to be corrected, is temporarily inputted to a computing circuit. An addition or subtraction operation is applied to that gray scale data to shift it by one or more gray scale levels, to thereby achieve transmissivity equivalent to the other colors which are not to be corrected.

3:64-4:6

In using TFTLCDs to display pictures, it is necessary to provide gray scale data of the picture to the LCD to drive the LCD. FIG. 1 shows the construction of the control unit of the TFTLCD. The array/cell portion 1 of the LCD is connected to an X-driver 3 and a Y-driver 5. The X-driver 3, when it is supplied with gray scale data, applies a voltage corresponding to the gray scale data to the cell. The Y-driver 5 is connected to the gate of a switching element, and conducts/does not conduct the voltage applied to the cell by the X-driver 3 at a predetermined time.

Gray scale data is supplied to the X-driver by data control unit 10. The data control unit 10 consists of a data control

1: 27-38

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DRIVER MEANS” (cont’d):**

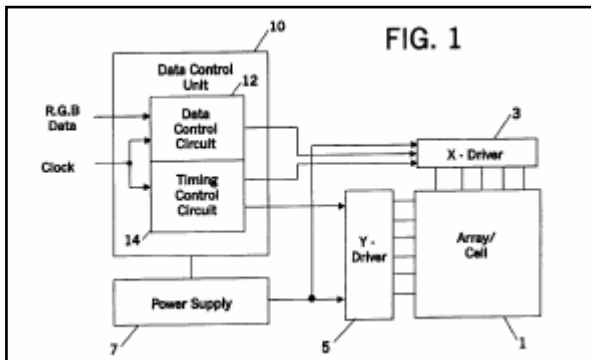
As an example of the second category (2), is a method in which the reference voltage (gray scale voltage) given to the data driver is tailored to the characteristics for each color. This method can compensate for the color dependency of the transmissivity/applied voltage characteristics. However, the circuits needed to independently control the reference voltages, raise the cost and cause difficulties in the implementation. Another method that falls within this second category, is to use the voltage for one of the colors of R/G/B as a reference voltage, and use offset voltages for each of other colors. This methods has the same problems as the method in which the reference voltages are separately applied, and in addition, cannot accomplish desired effect if the gradients of the curves showing the transmissivity/applied voltage characteristics of R/G/B vary with applied voltage. That is, in accordance with the offset voltage method, correction is carried out by applying a uniform offset voltage for all applied voltages, and thus the correction cannot be effectively performed unless the gradients of the curves showing the transmissivity/applied voltage characteristics are the same over the whole applied voltage range.

2:46-67

Japanese Published Unexamined Patent Application No. 01-101586 discloses a technique in which different liquid crystal driving voltage levels are set for each of the colors, and that level is applied to each pixel. Japanese Published Unexamined Patent Application No. 03-6986 discloses a technique in which the driving voltage is made to vary a predetermined voltage from color to color to obtain uniformity in transmissivity. Japanese Published Unexamined Patent Application No. 03-290618 discloses a technique in which a similar object is accomplished by independently inputting a gray scale control signal for each color.

3:1-11

## INTRINSIC EVIDENCE FOR DISPUTED TERM “DATA CONTROL MEANS”:



In using TFTLCDs to display pictures, it is necessary to provide gray scale data of the picture to the LCD to drive the LCD. FIG. 1 shows the construction of the control unit of the TFTLCD. The array/cell portion 1 of the LCD is connected to an X-driver 3 and a Y-driver 5. The X-driver 3, when it is supplied with gray scale data, applies a voltage corresponding to the gray scale data to the cell. The Y-driver 5 is connected to the gate of a switching element, and conducts/does not conduct the voltage applied to the cell by the X-driver 3 at a predetermined time.

Gray scale data is supplied to the X-driver by data control unit 10. The data control unit 10 consists of a data control circuit 12 for latching and storing the externally supplied R/G/B data in a buffer, and a timing control circuit 14 for outputting the gray scale data stored in the buffer to the X-driver 3 at a predetermined time. A clock signal is externally supplied to the data control circuit 12 and the timing control circuit 14 to control the timing. A power supply 7 is connected to the X-driver, Y-driver 5, and data control unit 10.

1:27-46

Ideally, the relationship between gray scale, applied voltage, and transmissivity is the same for each of the R/G/B

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colors. However in actuality, the gray scale and the achieved transmissivity have a slight difference depending on color. This is because the degree of light modulation for the specific twist of the twisted noematic liquid crystal is slightly different depending on wavelength. That is, even though a light passes through a liquid crystal layer in a similarly twisted state, the degree of the modulation given to the passing light is wavelength dependent, and thus the scattering of brightness that occurs for a given gray scale is color dependent. This is shown in FIG. 3. The transmissivity

1:66-2:10

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DATA CONTROL MEANS” (cont’d):**

displaying of intermediate colors. Thus, the correlation between transmissivity and applied voltage (hereinafter referred to as transmissivity/applied voltage characteristics) has a color (wavelength) dependency. If the displaying is performed without providing any correction, the graduation of color translates to blue more than called for by the halftone data, and the picture on the whole takes on a bluish hue. FIG. 4 shows this state represented by a chromaticity

2:16-24

As an example of the second category (2), is a method in which the reference voltage (gray scale voltage) given to the data driver is tailored to the characteristics for each color. This method can compensate for the color dependency of the transmissivity/applied voltage characteristics. However, the circuits needed to independently control the reference voltages, raise the cost and cause difficulties in the implementation. Another method that falls within this second category, is to use the voltage for one of the colors of R/G/B as a reference voltage, and use offset voltages for each of other colors. This methods has the same problems as the method in which the reference voltages are separately applied, and in addition, cannot accomplish desired effect if the gradients of the curves showing the transmissivity/applied voltage characteristics of R/G/B vary with applied voltage. That is, in accordance with the offset voltage method, correction is carried out by applying a uniform offset voltage for all applied voltages, and thus the correction cannot be effectively performed unless the gradients of the curves showing the transmissivity/applied voltage characteristics are the same over the whole applied voltage range.

2:46-67

Japanese Published Unexamined Patent Application No. 01-101586 discloses a technique in which different liquid crystal driving voltage levels are set for each of the colors, and that level is applied to each pixel. Japanese Published Unexamined Patent Application No. 03-6986 discloses a technique in which the driving voltage is made to vary a predetermined voltage from color to color to obtain uniformity in transmissivity. Japanese Published Unexamined Patent Application No. 03-290618 discloses a technique in which a similar object is accomplished by independently inputting a gray scale control signal for each color.

3:1-11

## **INTRINSIC EVIDENCE FOR DISPUTED TERM “DATA CONTROL MEANS” (cont’d):**

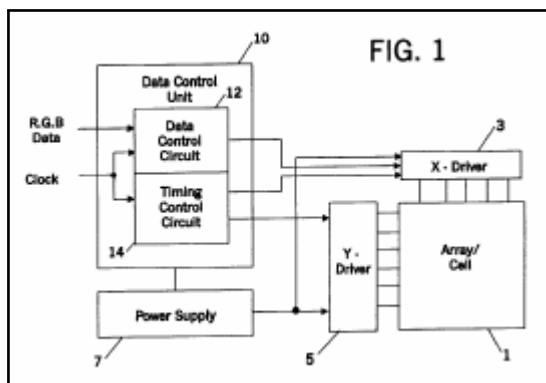
Therefore, first object of the subject invention is to provide a driving method for a TFTLCD in which the dependency on color of the transmissivity/applied voltage characteristics is effectively corrected.

A second object of the subject invention is to realize the effective correction using a very simple method which enables the above described correction to be made without increase in complexity of the control method, and the restrictions on the implementation by addition of circuits.

3:12-21

In accordance with the present invention, the above described problems are solved by gray scale data (a bit string for a color liquid crystal display) wherein the data control means includes a computing circuit for performing an addition or subtraction of the gray scale related to at least one color to generate a corrected gray scale, and also includes delay means for delaying the outputting of the uncorrected gray scales, during the time which the gray scale of the one color is being corrected.

3:24-31

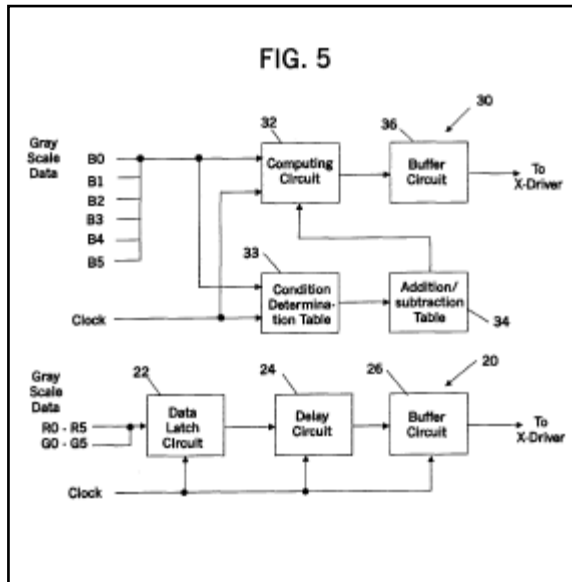


The subject invention can be realized by improving the data control unit 10 of FIG. 1 as is shown in FIG. 5. In the background art, the data control unit consists only of a latch and a buffer. However, in the subject invention, the gray

scale data related to a color, that is to be corrected, is temporarily inputted to a computing circuit. An addition or subtraction operation is applied to that gray scale data to shift it by one or more gray scale levels, to thereby achieve transmissivity equivalent to the other colors which are not to be corrected.

3:64-4:6

## INTRINSIC EVIDENCE FOR DISPUTED TERM “DATA CONTROL MEANS” (cont’d):



In FIG. 5, the color to be corrected is blue (B), and the colors which are not to be corrected are red (R) and green (G). The gray scale data related to R or G are shown by R0 to R5 or G0 to G5 in FIG. 5.

A portion 20 to which gray scale data related to R and G are inputted includes a data latch circuit 22 and a buffer circuit 26, like that in the data control unit in the background art. However, in addition to the data control unit in the background art, it includes a delay circuit 24. This is to compensate for the time during which the gray scale data B0 to B5 related to B is operated on by a computing circuit 32 in accordance with a condition determination table 36, as described later. The delay circuit 25 thereby assumes the outputting of the R and G gray scale data to the driver with the same timing as the corrected B gray scale data.

The gray data B0 to B5 for blue is a bit string for representing a 64-level gray scale. It is comprised of a bit string (B0, B1, B2, B3, B4, B5). For instance, if the gray scale is “4”, (B0, B1, B2, B3, B4, B5)=(001000), and if the gray scale is “28”, (B0, B1, B2, B3, B4, B5)=(001110). The same applied for R0 to R5 or G0 to G5 which are the gray scale data for red or green, respectively.

4:7-29

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DATA CONTROL MEANS” (cont’d):**

Gray Scale	Condition
0 - 3	A
4 - 10	B
11 - 53	C
54 - 60	B
61 - 63	A

FIG. 6

Further, the gray scale data for Blue is also supplied to a condition determination table 33. The condition determination table 33 determines the amount of the adjustment of the gray scale data. A diagrammatic representation of the condition determination table 33 is shown in FIG. 6. As shown, conditions A to C, corresponding to various gray scale levels, are set in the condition determination table 33. The

4:38-44

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DATA CONTROL MEANS” (cont’d):**

FIG. 7

Condition	Addition/ Subtraction Amount
A	0
B	-2
C	-4
⋮	⋮

levels, are set in the condition determination table 33. The condition corresponding to a gray scale is outputted from the condition determination table 33 to an addition/subtraction table 34. The addition/subtraction table 34 has the function of setting the actual amount of the addition or subtraction. A diagrammatic representation of the addition/subtraction table 34 is shown in FIG. 7. That is, the addition/subtraction tables set the amount to be added or subtracted according to the condition provided from the condition determination table 33. The amount of the addition or subtraction to correct the gray scale is supplied to the computing circuit 32.

The condition determination table 33 and the addition/subtraction table 34 can be implemented by software. The

4:45-56

**INTRINSIC EVIDENCE FOR DISPUTED TERM “DATA CONTROL MEANS” (cont’d):**

Operation of the circuit 30 to which gray scale data for blue is inputted, and of the circuit 20 to which gray scale data related to Red and Green are inputted is as follows. When a gray scale level “2” is received, or (B0, B1, B2, B3, B4, B5)=(010000) is inputted, the input to the display is determined by the condition determination table 33. As shown in FIG. 6, in the condition determination table 33, the condition A is outputted to the addition/subtraction table 34, and thereafter, in the addition/subtraction table 34, “0” is outputted to the computing circuit as the addition or subtraction amount as shown in FIG. 7. Accordingly, the gray scale “2” is provided unconnected to the X-driver via a buffer circuit 36. The above described processing causes a predetermined delay. Thus, the gray scale data for Red and Green corresponding to the gray scale data related to Blue are delayed for time taken for the processing by a delay circuit 24. As a result, the gray scale data related to B is outputted from the buffer circuit 36 to the X-driver is synchronized with the gray scale data for Red and Green for simultaneous output from the buffer circuit 26 to the X-driver.

5: 11-29

Where the gray scale data level is “20,” or the grey scale level signal (B0, B1, B2, B3, B4, B5)=(001010), the condition determination table 33 provides condition C signal to the addition/subtraction table 34 as shown in FIG. 6. In response, the addition/subtraction table 34 provides a signal to the computing circuit to subtract four grey scale levels (the amount as shown as -4 in FIG. 7). Accordingly, the gray scale level “20” is corrected by the computing circuit 32 to a gray scale level “16”(20-4=16) which level is provided to the X-driver via the buffer circuit 36. In this way, corrections are made to the transmissivity/applied voltage characteristics where, as shown in FIG. 3, they are not uniform for each color.

5: 30-43

With the method of the subject invention, only an additional circuit such as a computing circuit, is needed to effectively correct the differences in the transmissivity/applied voltage characteristics for colors. The above correction is made while avoiding the problems in complexity of control methods in the background art. That is, to implement

5:58-63

**EXHIBIT S**  
**U.S. PATENT NO. 6,008,786**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 1**

I. A liquid crystal color display comprising:  
a) a display cell containing a light transmitting medium,  
b) driver means connected to said display cell for driving the display cell with sets of grey scale data signals each signal for a different color, and  
c) data control means for receiving gray scale data signals related to the setting of a gray scale for the display cell and outputting said gray scale data signals to said driver with a predetermined timing, wherein said data control means includes:  
i) **computing means** for changing the level of the gray scale data signals for at least one color relative to the other colors to a different gray scale level to compensate for a variation in intensity between the colors due to wavelength related differences in transmissivity between the colors through the light transmitting medium, and  
ii) **buffer means** for delaying any uncorrected gray scale signal related to the other colors for the time delay caused by said corrected gray scale data signal being corrected.

**LGD's Claim Construction**

**computing means**<sup>1</sup> –

Interpreted per  
35 USC §112 ¶6.

*function:* changing the level of the gray scale data signals for at least one color relative to the other colors to a different gray scale level to compensate for a variation in intensity between the colors due to wavelength related differences in transmissivity between the colors through the light transmitting medium.

*structure:* Fig. 5, elements 32, 33, 34; Figs. 6-8

**buffer means**<sup>2</sup> – Interpreted per 35 USC §112 ¶6.

*function:* delaying any uncorrected gray scale signal related to the other colors for the time delay caused by said corrected gray scale data signal being corrected.

*structure:* Fig. 5, element 24.

Indefinite.

<sup>1</sup> Disputed Term “computing means” also appears in asserted claim 1 in the same context.

<sup>2</sup> Disputed Term “buffer means” also appears in asserted claim 1 in the same context.

## **INTRINSIC EVIDENCE FOR DISPUTED TERM “COMPUTING MEANS”:**

As an example of the second category (2), is a method in which the reference voltage (gray scale voltage) given to the data driver is tailored to the characteristics for each color. This method can compensate for the color dependency of the transmissivity/applied voltage characteristics. However, the circuits needed to independently control the reference voltages, raise the cost and cause difficulties in the implementation. Another method that falls within this second category, is to use the voltage for one of the colors of R/G/B as a reference voltage, and use offset voltages for each of other colors. This methods has the same problems as the method in which the reference voltages are separately applied, and in addition, cannot accomplish desired effect if the gradients of the curves showing the transmissivity/applied voltage characteristics of R/G/B vary with applied voltage. That is, in accordance with the offset voltage method, correction is carried out by applying a uniform offset voltage for all applied voltages, and thus the correction cannot be effectively performed unless the gradients of the curves showing the transmissivity/applied voltage characteristics are the same over the whole applied voltage range.

2:46-67

Japanese Published Unexamined Patent Application No. 01-101586 discloses a technique in which different liquid crystal driving voltage levels are set for each of the colors, and that level is applied to each pixel. Japanese Published Unexamined Patent Application No. 03-6986 discloses a technique in which the driving voltage is made to vary a predetermined voltage from color to color to obtain uniformity in transmissivity. Japanese Published Unexamined Patent Application No. 03-290618 discloses a technique in which a similar object is accomplished by independently inputting a gray scale control signal for each color.

Therefore, first object of the subject invention is to provide a driving method for a TFTLCD in which the dependency on color of the transmissivity/applied voltage characteristics is effectively corrected.

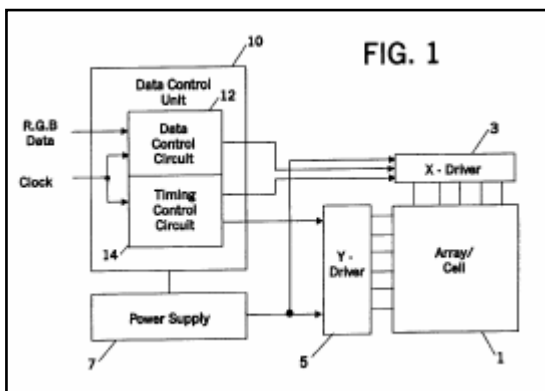
3: 1-11

## **INTRINSIC EVIDENCE FOR DISPUTED TERM “COMPUTING MEANS” (cont’d):**

### **SUMMARY OF THE INVENTION**

In accordance with the present invention, the above described problems are solved by gray scale data (a bit string for a color liquid crystal display) wherein the data control means includes a computing circuit for performing an addition or subtraction of the gray scale related to at least one color to generate a corrected gray scale, and also includes delay means for delaying the outputting of the uncorrected gray scales, during the time which the gray scale of the one color is being corrected.

3: 24-32



### **PREFERRED EMBODIMENT**

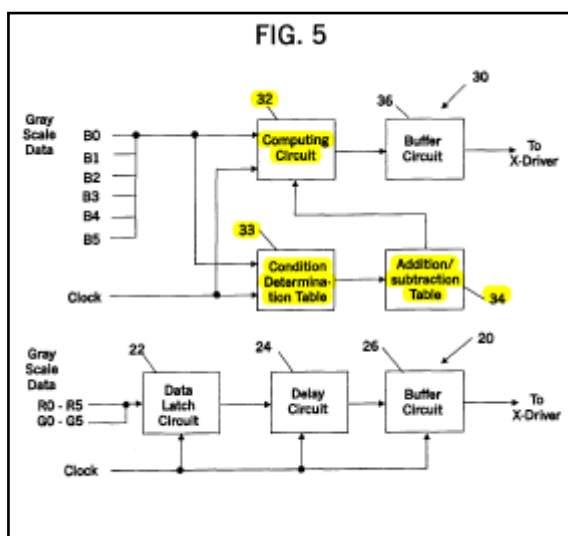
The subject invention can be realized by improving the data control unit 10 of FIG. 1 as is shown in FIG. 5. In the background art, the data control unit consists only of a latch and a buffer. However, in the subject invention, the gray

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scale data related to a color, that is to be corrected, is temporarily inputted to a computing circuit. An addition or subtraction operation is applied to that gray scale data to shift it by one or more gray scale levels, to thereby achieve transmissivity equivalent to the other colors which are not to be corrected.

3:64-4:6

## INTRINSIC EVIDENCE FOR DISPUTED TERM “COMPUTING MEANS” (cont’d):



In FIG. 5, the color to be corrected is blue (B), and the colors which are not to be corrected are red (R) and green (G). The gray scale data related to R or G are shown by R0 to R5 or G0 to G5 in FIG. 5.

A portion 20 to which gray scale data related to R and G are inputted includes a data latch circuit 22 and a buffer circuit 26, like that in the data control unit in the background art. However, in addition to the data control unit in the background art, it includes a delay circuit 24. This is to compensate for the time during which the gray scale data B0 to B5 related to B is operated on by a computing circuit 32 in accordance with a condition determination table 36, as described later. The delay circuit 25 thereby assumes the outputting of the R and G gray scale data to the driver with the same timing as the corrected B gray scale data.

The gray data B0 to B5 for blue is a bit string for representing a 64-level gray scale. It is comprised of a bit string (B0, B1, B2, B3, B4, B5). For instance, if the gray scale is “4”, (B0, B1, B2, B3, B4, B5)=(001000), and if the gray scale is “28”, (B0, B1, B2, B3, B4, B5)=(001110). The same applied for R0 to R5 or G0 to G5 which are the gray scale data for reg or green, respectively.

4: 6-29

**INTRINSIC EVIDENCE FOR DISPUTED TERM “COMPUTING MEANS” (cont’d):**

Gray Scale	Condition
0 - 3	A
4 - 10	B
11 - 53	C
54 - 60	B
61 - 63	A

FIG. 6

Further, the gray scale data for Blue is also supplied to a condition determination table 33. The condition determination table 33 determines the amount of the adjustment of the gray scale data. A diagrammatic representation of the condition determination table 33 is shown in FIG. 6. As shown, conditions A to C, corresponding to various gray scale levels, are set in the condition determination table 33. The

4:38-44

**INTRINSIC EVIDENCE FOR DISPUTED TERM “COMPUTING MEANS” (cont’d):**

FIG. 7

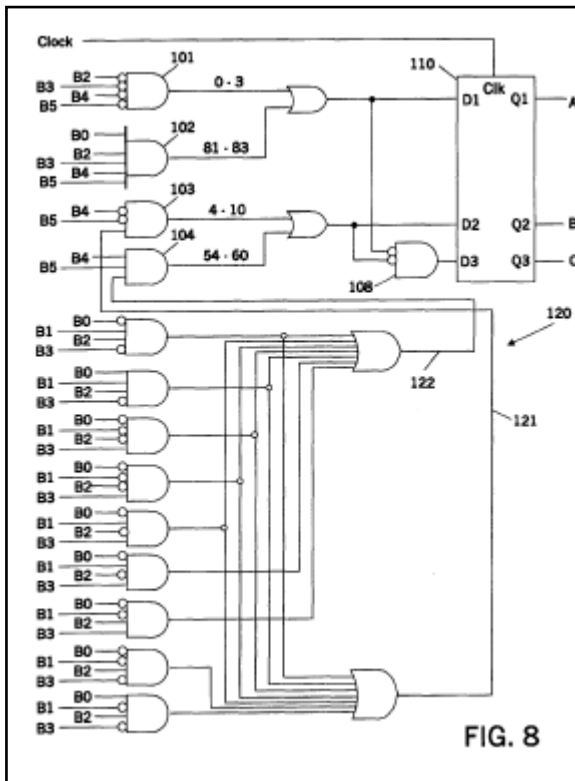
Condition	Addition/ Subtraction Amount
A	0
B	-2
C	-4
⋮	⋮

levels, are set in the condition determination table 33. The condition corresponding to a gray scale is outputted from the condition determination table 33 to an addition/subtraction table 34. The addition/subtraction table 34 has the function of setting the actual amount of the addition or subtraction. A diagrammatic representation of the addition/subtraction table 34 is shown in FIG. 7. That is, the addition/subtraction tables set the amount to be added or subtracted according to the condition provided from the condition determination table 33. The amount of the addition or subtraction to correct the gray scale is supplied to the computing circuit 32.

The condition determination table 33 and the addition/subtraction table 34 can be implemented by software. The

4:45-56

## **INTRINSIC EVIDENCE FOR DISPUTED TERM “COMPUTING MEANS” (cont’d):**



subtraction table 34 can be implemented by software. The condition determination table can also be implemented by hardware by using the logic circuit shown in FIG. 8. To implement the specific conditions represented in FIG. 6, the gray scale data B0 to B5 are inputted to the logic circuit as shown. The gray scale data of B2 to B5 are inverted and inputted to an AND circuit 101 to create a condition corresponding to condition A in FIG. 6 for gray scale levels 0 to 3. Similarly, the gray scale data B0, B2 to B5 for gray scale levels 61 to 63 corresponding to condition A is inputted into AND circuit 102. The outputs of the AND circuit 101 and the AND circuit 102 are inputted to an OR circuit 106, and

the condition A is outputted by circuit 110. AND circuit 103 and AND circuit 104 are circuits for generating condition B. Inputted to ANDs 103 and 104 is an output 122 separately created in a group of logic circuits 120, to thereby output the condition B for desired gray scale data levels 4 to 10 and 54 to 60. If there is no output from OR circuits 106 and 107, condition C is set. In this case, an output is provided by an AND circuit 108 to the circuit 110 to achieve the generation of condition C. Conditions A, B, and C are outputted from Q1 to Q3 of the circuit 110.

4:56-5:9

**INTRINSIC EVIDENCE FOR DISPUTED TERM “COMPUTING MEANS” (cont’d):**

Operation of the circuit 30 to which gray scale data for blue is inputted, and of the circuit 20 to which gray scale data related to Red and Green are inputted is as follows. When a gray scale level “2” is received, or (B0, B1, B2, B3, B4, B5)=(010000) is inputted, the input to the display is determined by the condition determination table 33. As shown in FIG. 6, in the condition determination table 33, the condition A is outputted to the addition/subtraction table 34, and thereafter, in the addition/subtraction table 34, “0” is outputted to the computing circuit as the addition or subtraction amount as shown in FIG. 7. Accordingly, the gray scale “2” is provided unconnected to the X-driver via a buffer circuit 36. The above described processing causes a predetermined delay. Thus, the gray scale data for Red and Green corresponding to the gray scale data related to Blue are delayed for time taken for the processing by a delay circuit 24. As a result, the gray scale data related to B is outputted from the buffer circuit 36 to the X-driver is synchronized with the gray scale data for Red and Green for simultaneous output from the buffer circuit 26 to the X-driver.

5:10-29

Where the gray scale data level is “20,” or the grey scale level signal (B0, B1, B2, B3, B4, B5)=(001010), the condition determination table 33 provides condition C signal to the addition/subtraction table 34 as shown in FIG. 6. In response, the addition/subtraction table 34 provides a signal to the computing circuit to subtract four grey scale levels (the amount as shown as -4 in FIG. 7). Accordingly, the gray scale level “20” is corrected by the computing circuit 32 to a gray scale level “16”(20-4=16) which level is provided to the X-driver via the buffer circuit 36. In this way, corrections are made to the transmissivity/applied voltage characteristics where, as shown in FIG. 3, they are not uniform for each color.

5:30-43

With the method of the subject invention, only an additional circuit such as a computing circuit, is needed to effectively correct the differences in the transmissivity/applied voltage characteristics for colors. The above correction is made while avoiding the problems in complexity of control methods in the background art. That is, to implement

5:58-63

## **INTRINSIC EVIDENCE FOR DISPUTED TERM “BUFFER MEANS”:**

transmissivity/applied voltage characteristics. However, the circuits needed to independently control the reference voltages, raise the cost and cause difficulties in the implementation. Another method that falls within this second category, is to use the voltage for one of the colors of R/G/B as a reference voltage, and use offset voltages for each of other colors. This methods has the same problems as the method in which the reference voltages are separately applied, and in addition, cannot accomplish desired effect if the gradients of the curves showing the transmissivity/applied voltage characteristics of R/G/B vary with applied voltage. That is, in accordance with the offset voltage method, correction is carried out by applying a uniform offset voltage for all applied voltages, and thus the correction cannot be effectively performed unless the gradients of the curves showing the transmissivity/applied voltage characteristics are the same over the whole applied voltage range.

2:50-67

Japanese Published Unexamined Patent Application No. 01-101586 discloses a technique in which different liquid crystal driving voltage levels are set for each of the colors, and that level is applied to each pixel. Japanese Published Unexamined Patent Application No. 03-6986 discloses a technique in which the driving voltage is made to vary a predetermined voltage from color to color to obtain uniformity in transmissivity. Japanese Published Unexamined Patent Application No. 03-290618 discloses a technique in which a similar object is accomplished by independently inputting a gray scale control signal for each color.

3:1-11

Therefore, first object of the subject invention is to provide a driving method for a TFTLCD in which the dependency on color of the transmissivity/applied voltage characteristics is effectively corrected.

3:12-20

A second object of the subject invention is to realize the effective correction using a very simple method which enables the above described correction to be made without increase in complexity of the control method, and the restrictions on the implementation by addition of circuits.

**INTRINSIC EVIDENCE FOR DISPUTED TERM “BUFFER MEANS” (cont’d):**

**SUMMARY OF THE INVENTION**

In accordance with the present invention, the above described problems are solved by gray scale data (a bit string for a color liquid crystal display) wherein the data control means includes a computing circuit for performing an addition or subtraction of the gray scale related to at least one color to generate a corrected gray scale, and also includes delay means for delaying the outputting of the uncorrected gray scales, during the time which the gray scale of the one color is being corrected.

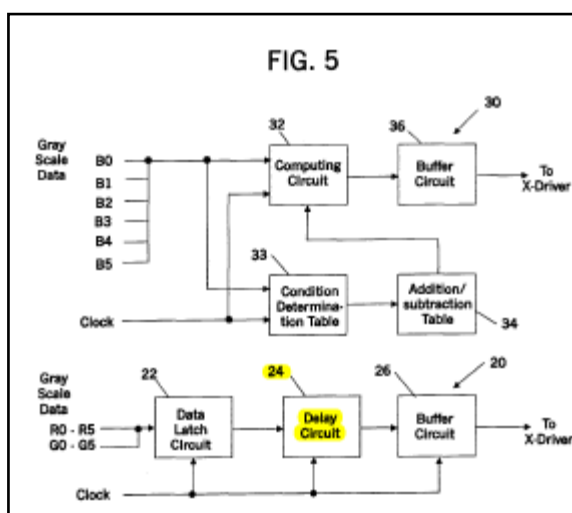
3:24-32

**PREFERRED EMBODIMENT**

The subject invention can be realized by improving the data control unit 10 of FIG. 1 as is shown in FIG. 5. In the background art, the data control unit consists only of a latch and a buffer. However, in the subject invention, the gray scale data related to a color, that is to be corrected, is temporarily inputted to a computing circuit. An addition or subtraction operation is applied to that gray scale data to shift it by one or more gray scale levels, to thereby achieve transmissivity equivalent to the other colors which are not to be corrected.

3:63-4:6

**INTRINSIC EVIDENCE FOR DISPUTED TERM “BUFFER MEANS” (cont’d):**



A portion 20 to which gray scale data related to R and G are inputted includes a data latch circuit 22 and a buffer circuit 26, like that in the data control unit in the background art. However, in addition to the data control unit in the background art, it includes a delay circuit 24. This is to compensate for the time during which the gray scale data B0 to B5 related to B is operated on by a computing circuit 32 in accordance with a condition determination table 36, as described later. The delay circuit 25 thereby assumes the outputting of the R and G gray scale data to the driver with the same timing as the corrected B gray scale data.

The gray data B0 to B5 for blue is a bit string for representing a 64-level gray scale. It is comprised of a bit string (B0, B1, B2, B3, B4, B5). For instance, if the gray scale is “4”, (B0, B1, B2, B3, B4, B5)=(001000), and if the gray scale is “28”, (B0, B1, B2, B3, B4, B5)=(001110). The same applied for R0 to R5 or G0 to G5 which are the gray scale data for red or green, respectively.

4:7-29

**INTRINSIC EVIDENCE FOR DISPUTED TERM “BUFFER MEANS” (cont’d):**

Gray Scale	Condition
0 - 3	A
4 - 10	B
11 - 53	C
54 - 60	B
61 - 63	A

FIG. 6

Further, the gray scale data for Blue is also supplied to a condition determination table 33. The condition determination table 33 determines the amount of the adjustment of the gray scale data. A diagrammatic representation of the condition determination table 33 is shown in FIG. 6. As shown, conditions A to C, corresponding to various gray scale levels, are set in the condition determination table 33. The

4:38-4

**INTRINSIC EVIDENCE FOR DISPUTED TERM “BUFFER MEANS”(cont’d):**

FIG. 7

Condition	Addition/ Subtraction Amount
A	0
B	-2
C	-4
⋮	⋮

levels, are set in the condition determination table 33. The condition corresponding to a gray scale is outputted from the condition determination table 33 to an addition/subtraction table 34. The addition/subtraction table 34 has the function of setting the actual amount of the addition or subtraction. A diagrammatic representation of the addition/subtraction table 34 is shown in FIG. 7. That is, the addition/subtraction tables set the amount to be added or subtracted according to the condition provided from the condition determination table 33. The amount of the addition or subtraction to correct the gray scale is supplied to the computing circuit 32.

The condition determination table 33 and the addition/subtraction table 34 can be implemented by software. The

4:44-56

**EXHIBIT S**  
**U.S. PATENT NO. 6,008,786**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 2**

2. A liquid crystal color display of claim 1 wherein: said data control means comprises adjusting means for varying the amount of correction accorded to the gray scale data signals for said at least one color.

**LGD's Claim Construction**

**adjusting means**<sup>1</sup> –

Interpreted per  
35 USC §112 ¶6.

*function:* varying the amount  
of correction accorded to the  
gray scale data signals for  
said at least one color.

*structure:* Fig. 5, element 33,  
34; Figs. 6-8.

**INTRINSIC EVIDENCE FOR DISPUTED TERM “ADJUSTING MEANS”:**

As an example of the second category (2), is a method in which the reference voltage (gray scale voltage) given to the data driver is tailored to the characteristics for each color. This method can compensate for the color dependency of the transmissivity/applied voltage characteristics. However, the circuits needed to independently control the reference voltages, raise the cost and cause difficulties in the implementation. Another method that falls within this second category, is to use the voltage for one of the colors of R/G/B as a reference voltage, and use offset voltages for each of other colors. This methods has the same problems as the method in which the reference voltages are separately applied, and in addition, cannot accomplish desired effect if the gradients of the curves showing the transmissivity/applied voltage characteristics of R/G/B vary with applied voltage. That is, in accordance with the offset voltage method, correction is carried out by applying a uniform offset voltage for all applied voltages, and thus the correction cannot be effectively performed unless the gradients of the curves showing the transmissivity/applied voltage characteristics are the same over the whole applied voltage range.

2:46-67

Japanese Published Unexamined Patent Application No. 01-101586 discloses a technique in which different liquid crystal driving voltage levels are set for each of the colors, and that level is applied to each pixel. Japanese Published Unexamined Patent Application No. 03-6986 discloses a technique in which the driving voltage is made to vary a predetermined voltage from color to color to obtain uniformity in transmissivity. Japanese Published Unexamined Patent Application No. 03-290618 discloses a technique in which a similar object is accomplished by independently inputting a gray scale control signal for each color.

Therefore, first object of the subject invention is to provide a driving method for a TFTLCD in which the dependency on color of the transmissivity/applied voltage characteristics is effectively corrected.

A second object of the subject invention is to realize the effective correction using a very simple method which enables the above described correction to be made without increase in complexity of the control method, and the restrictions on the implementation by addition of circuits.

3:1-20

**INTRINSIC EVIDENCE FOR DISPUTED TERM “ADJUSTING MEANS” (cont’d):**

**SUMMARY OF THE INVENTION**

In accordance with the present invention, the above described problems are solved by gray scale data (a bit string for a color liquid crystal display) wherein the data control means includes a computing circuit for performing an addition or subtraction of the gray scale related to at least one color to generate a corrected gray scale, and also includes delay means for delaying the outputting of the uncorrected gray scales, during the time which the gray scale of the one color is being corrected.

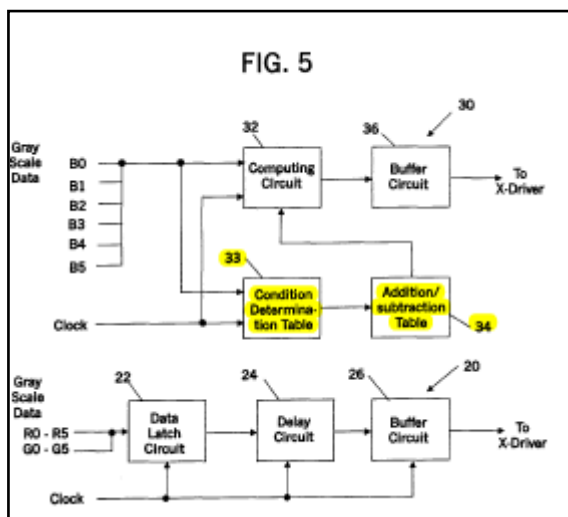
2:46-67

**PREFERRED EMBODIMENT**

The subject invention can be realized by improving the data control unit 10 of FIG. 1 as is shown in FIG. 5. In the background art, the data control unit consists only of a latch and a buffer. However, in the subject invention, the gray scale data related to a color, that is to be corrected, is temporarily inputted to a computing circuit. An addition or subtraction operation is applied to that gray scale data to shift it by one or more gray scale levels, to thereby achieve transmissivity equivalent to the other colors which are not to be corrected.

3:63-4:6

## **INTRINSIC EVIDENCE FOR DISPUTED TERM “ADJUSTING MEANS” (cont’d):**



In FIG. 5, the color to be corrected is blue (B), and the colors which are not to be corrected are red (R) and green (G). The gray scale data related to R or G are shown by R0 to R5 or G0 to G5 in FIG. 5.

A portion 20 to which gray scale data related to R and G are inputted includes a data latch circuit 22 and a buffer circuit 26, like that in the data control unit in the background art. However, in addition to the data control unit in the background art, it includes a delay circuit 24. This is to compensate for the time during which the gray scale data B0 to B5 related to B is operated on by a computing circuit 32 in accordance with a condition determination table 36, as described later. The delay circuit 25 thereby assumes the outputting of the R and G gray scale data to the driver with the same timing as the corrected B gray scale data.

The gray data B0 to B5 for blue is a bit string for representing a 64-level gray scale. It is comprised of a bit string (B0, B1, B2, B3, B4, B5). For instance, if the gray scale is “4”, (B0, B1, B2, B3, B4, B5)=(001000), and if the gray scale is “28”, (B0, B1, B2, B3, B4, B5)=(001110). The same applied for R0 to R5 or G0 to G5 which are the gray scale data for red or green, respectively.

4:7-29

**INTRINSIC EVIDENCE FOR DISPUTED TERM “ADJUSTING MEANS” (cont’d):**

Gray Scale	Condition
0 - 3	A
4 - 10	B
11 - 53	C
54 - 60	B
61 - 63	A

FIG. 6

Further, the gray scale data for Blue is also supplied to a condition determination table 33. The condition determination table 33 determines the amount of the adjustment of the gray scale data. A diagrammatic representation of the condition determination table 33 is shown in FIG. 6. As shown, conditions A to C, corresponding to various gray scale levels, are set in the condition determination table 33. The

4:38-44

Condition	Addition/ Subtraction Amount
A	0
B	-2
C	-4
⋮	⋮

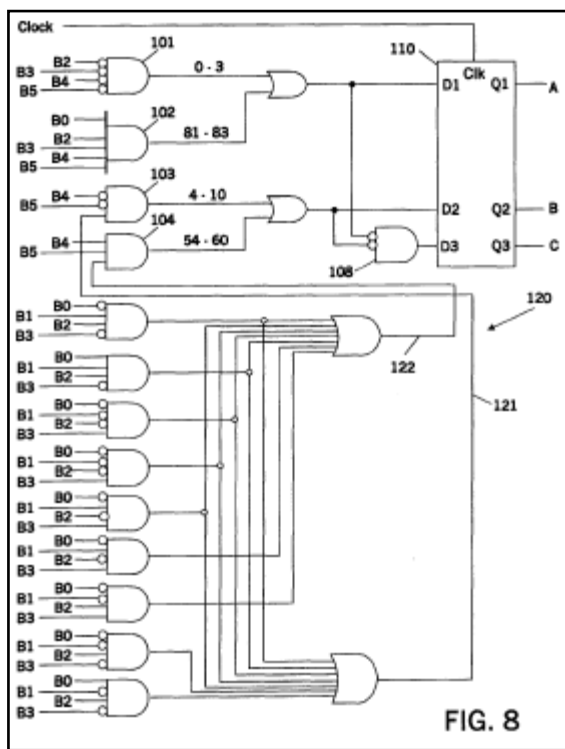
FIG. 7

levels, are set in the condition determination table 33. The condition corresponding to a gray scale is outputted from the condition determination table 33 to an addition/subtraction table 34. The addition/subtraction table 34 has the function of setting the actual amount of the addition or subtraction. A diagrammatic representation of the addition/subtraction table 34 is shown in FIG. 7. That is, the addition/subtraction tables set the amount to be added or subtracted according to the condition provided from the condition determination table 33. The amount of the addition or subtraction to correct the gray scale is supplied to the computing circuit 32.

The condition determination table 33 and the addition/subtraction table 34 can be implemented by software. The

4:45-56

## **INTRINSIC EVIDENCE FOR DISPUTED TERM “ADJUSTING MEANS” (cont’d):**



The condition determination table 33 and the addition/subtraction table 34 can be implemented by software. The condition determination table can also be implemented by hardware by using the logic circuit shown in FIG. 8. To implement the specific conditions represented in FIG. 6, the gray scale data B0 to B5 are inputted to the logic circuit as shown. The gray scale data of B2 to B5 are inverted and inputted to an AND circuit 101 to create a condition corresponding to condition A in FIG. 6 for gray scale levels 0 to 3. Similarly, the gray scale data B0, B2 to B5 for gray scale levels 61 to 63 corresponding to condition A is inputted into AND circuit 102. The outputs of the AND circuit 101 and the AND circuit 102 are inputted to an OR circuit 106, and the condition A is outputted by circuit 110. AND circuit 103 and AND circuit 104 are circuits for generating condition B. Inputted to ANDs 103 and 104 is an output 122 separately created in a group of logic circuits 120, to thereby output the condition B for desired gray scale data levels 4 to 10 and 54 to 60. If there is no output from OR circuits 106 and 107, condition C is set. In this case, an output is provided by an AND circuit 108 to the circuit 110 to achieve the generation of condition C. Conditions A, B, and C are outputted from Q1 to Q3 of the circuit 110.

4:55-5:9

**INTRINSIC EVIDENCE FOR DISPUTED TERM “ADJUSTING MEANS” (cont’d):**

Operation of the circuit 30 to which gray scale data for blue is inputted, and of the circuit 20 to which gray scale data related to Red and Green are inputted is as follows. When a gray scale level “2” is received, or (B0, B1, B2, B3, B4, B5)=(010000) is inputted, the input to the display is determined by the condition determination table 33. As shown in FIG. 6, in the condition determination table 33, the condition A is outputted to the addition/subtraction table 34, and thereafter, in the addition/subtraction table 34, “0” is outputted to the computing circuit as the addition or subtraction amount as shown in FIG. 7. Accordingly, the gray scale “2” is provided unconnected to the X-driver via a buffer circuit 36. The above described processing causes a predetermined delay. Thus, the gray scale data for Red and Green corresponding to the gray scale data related to Blue are delayed for time taken for the processing by a delay circuit 24. As a result, the gray scale data related to B is outputted from the buffer circuit 36 to the X-driver is synchronized with the gray scale data for Red and Green for simultaneous output from the buffer circuit 26 to the X-driver.

5:10-30

Where the gray scale data level is “20,” or the grey scale level signal (B0, B1, B2, B3, B4, B5)=(001010), the condition determination table 33 provides condition C signal to the addition/subtraction table 34 as shown in FIG. 6. In response, the addition/subtraction table 34 provides a signal to the computing circuit to subtract four grey scale levels (the amount as shown as -4 in FIG. 7). Accordingly, the gray scale level “20” is corrected by the computing circuit 32 to a gray scale level “16”(20-4=16) which level is provided to the X-driver via the buffer circuit 36. In this way, corrections are made to the transmissivity/applied voltage characteristics where, as shown in FIG. 3, they are not uniform for each color.

5:31-43

With the method of the subject invention, only an additional circuit such as a computing circuit, is needed to effectively correct the differences in the transmissivity/applied voltage characteristics for colors. The above correction is made while avoiding the problems in complexity of control methods in the background art. That is, to implement

5:58-63

# **EXHIBIT L-34**

**Ex. L-34**  
**CMO US PATENT No. 7,280,179**

**INDEX OF DISPUTED TERMS**

<b><u>CLAIM TERMS</u></b>	<b><u>PAGE</u></b>
forming a sealing member having a main portion enclosing a display region .....	1
the sealing member has a main portion enclosing a display region.....	8
overlapping area extends along one side of the display region .....	1
applying the sealing material along the display region to form the main portion of the sealing member .....	1

**EXHIBIT L-34**  
**U.S. PATENT NO. 7,280,179**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 1**

1. A method for manufacturing a liquid crystal display cell comprising the following steps:  
forming a sealing member having a main portion enclosing a display region and a protrusion part extending from the main portion wherein the sealing member is formed by the following steps:  
applying a sealing material to either one of a pair of substrates from a position outside of the display region toward the display region to form the protrusion part of the sealing member; and  
continuing applying the sealing material along the display region to form the main portion of the sealing member, wherein positions of an initial end and an overlapping area within the sealing member are different and the overlapping area extends along one side of the display region;  
dispensing a liquid crystal material upon one of the pair of substrates;  
superposing one of the pair of substrates upon the other one such that the liquid crystal material is enclosed by the sealing member;  
curing the sealing member;  
cutting the pair of substrates to obtain the liquid crystal display cell.

**LGD's Claim Construction**

**forming a sealing member having a main portion enclosing a display region** – depositing sealant material parallel to the edges of the display region so that it encloses the display region

**overlapping area extends along one side of the display region<sup>1</sup>** – a segment of the sealing member main portion where sealant material is applied on top of previously applied sealant material along one edge of the display region

**applying the sealing material along the display region to form the main portion of the sealing member<sup>2</sup>** – depositing sealant material parallel to the edges of the display region

<sup>1</sup> Disputed Term “overlapping area extends along one side of the display region” also appears in asserted claims 8 and 15 in the same context.

<sup>2</sup> Disputed Term “applying the sealing material along the display region to form the main portion of the sealing member” also appears in asserted claims 5 and 8 in the same context.

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “FORMING A SEALING MEMBER HAVING A MAIN PORTION ENCLOSING A DISPLAY REGION” AND “APPLYING THE SEALING MATERIAL ALONG THE DISPLAY REGION TO FORM THE MAIN PORTION OF THE SEALING MEMBER”:**

A liquid crystal display cell and a method for manufacturing the same are disclosed. The method includes the following steps. First, a sealing member including a main portion enclosing a display region and a protrusion part extending from the main portion is formed. Then, a liquid crystal material is dispensed upon one of a pair of substrates, and then one substrate is superposed upon the other substrate so as to perform alignment and assembly processes. After the

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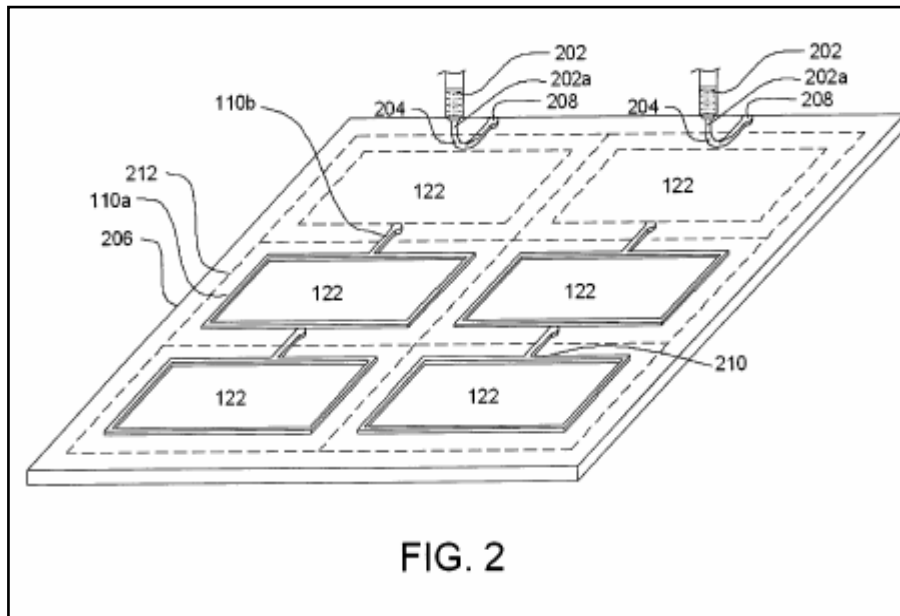
and the other substrate is covered thereupon. This technique greatly reduces the steps of a process of making LCD panels and improves manufacturing efficiencies. More specifically, the one drop fill (ODF) method includes the following steps. First, a sealant is applied to the whole periphery of one of a pair of substrates so as to form a sealing member and then a liquid crystal material is dispensed upon one of the pair of substrates. After the dispensing step, one substrate is super-

1:25-32

However, in the ODF method, the sealing member formed before the liquid crystal material being dispensed is required to fully enclose a display region of one substrate without leaving any opening thereof. When the sealing member is formed by an application manner, it is designed to have an overlapping segment between the initial end and the final end of the sealant so as to ensure that the formed sealing member can fully enclose the display region. However, the

1:49-56

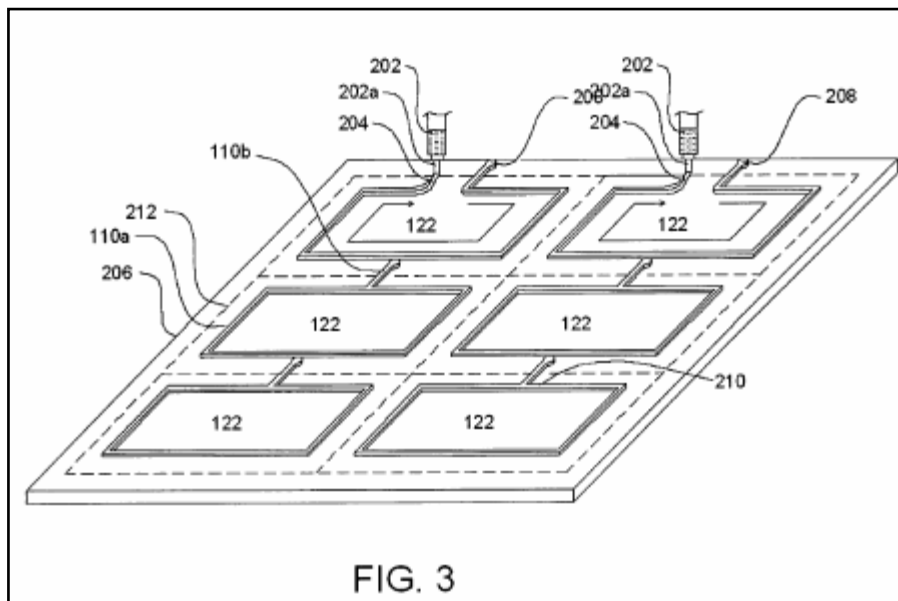
**INTRINSIC EVIDENCE FOR DISPUTED TERMS “FORMING A SEALING MEMBER HAVING A MAIN PORTION ENCLOSING A DISPLAY REGION” AND “APPLYING THE SEALING MATERIAL ALONG THE DISPLAY REGION TO FORM THE MAIN PORTION OF THE SEALING MEMBER” (cont’d):**



uncontrollably over-applied. Therefore, the present invention provides a novel applying method. Referring to FIG. 2, the needle 202a of the injector 202 is set to a position outside the display region 122 for starting to apply the sealing material 204, and then the sealing material 204 is applied toward the display region 122 to form the protrusion part 110b of the sealing member 110. Referring to FIG. 3, the

4:12-23

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “FORMING A SEALING MEMBER HAVING A MAIN PORTION ENCLOSING A DISPLAY REGION” AND “APPLYING THE SEALING MATERIAL ALONG THE DISPLAY REGION TO FORM THE MAIN PORTION OF THE SEALING MEMBER” (cont’d):**



10b of the sealing member 110. Referring to FIG. 3, the sealing material 204 is then continued being applied along the display region 122 according to the arrow direction till forming a small overlapping area 210, thereby enclosing the display region 122 and thus forming the main portion 110a of the sealing member 110. Preferably, the main portion

4:18-23

**INTRINSIC EVIDENCE FOR DISPUTED TERMS “FORMING A SEALING MEMBER HAVING A MAIN PORTION ENCLOSING A DISPLAY REGION” AND “APPLYING THE SEALING MATERIAL ALONG THE DISPLAY REGION TO FORM THE MAIN PORTION OF THE SEALING MEMBER” (cont’d):**

FIG. 4

FIG. 8

As seen in the figures above, the Yoshizoe reference does not teach the feature, “wherein positions of an initial end and an overlapping area within the sealing member are different and the overlapping area extends along one side of the display region,” as illustrated in FIG. 4 from the present invention below (area 210).

FIG. 4

Applicants submit that if anything, the Yoshizoe reference actually teaches away from the feature in claim 1 reciting, “the overlapping area extends along one side of the display region.” The Yoshizoe reference states the following:

... the sealant is coated such that the sealant is formed traveling apart gradually from the display region toward start and termination points of the sealant while overlapping a part thereof outside the closed loop portion and therefore, even when the two substrates are adhered to each other to

13

~

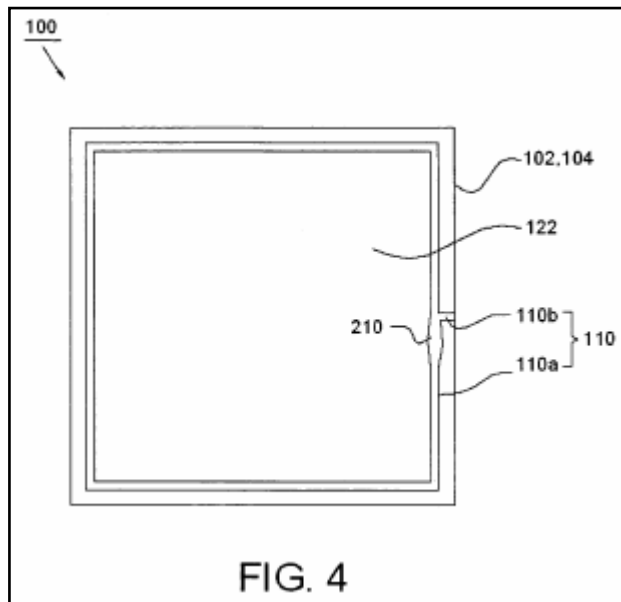
resultantly widen the width of the sealant, the sealant never intrudes into the display region.

(Col. 2, lines 33-40; *Emphasis added.*) That is, the Yoshizoe reference teaches that the “overlapping area” lies outside the display region rather than extending along one side of the display region as taught in claim 1.

**INTRINSIC EVIDENCE FOR DISPUTED TERM “OVERLAPPING AREA EXTENDS ALONG ONE SIDE OF THE DISPLAY REGION”:**

However, in the ODF method, the sealing member formed before the liquid crystal material being dispensed is required to fully enclose a display region of one substrate without leaving any opening thereof. When the sealing member is formed by an application manner, it is designed to have an overlapping segment between the initial end and the final end of the sealant so as to ensure that the formed sealing member can fully enclose the display region. However, the usage amount of the sealant for forming this overlapping segment is generally more than that for forming other parts.

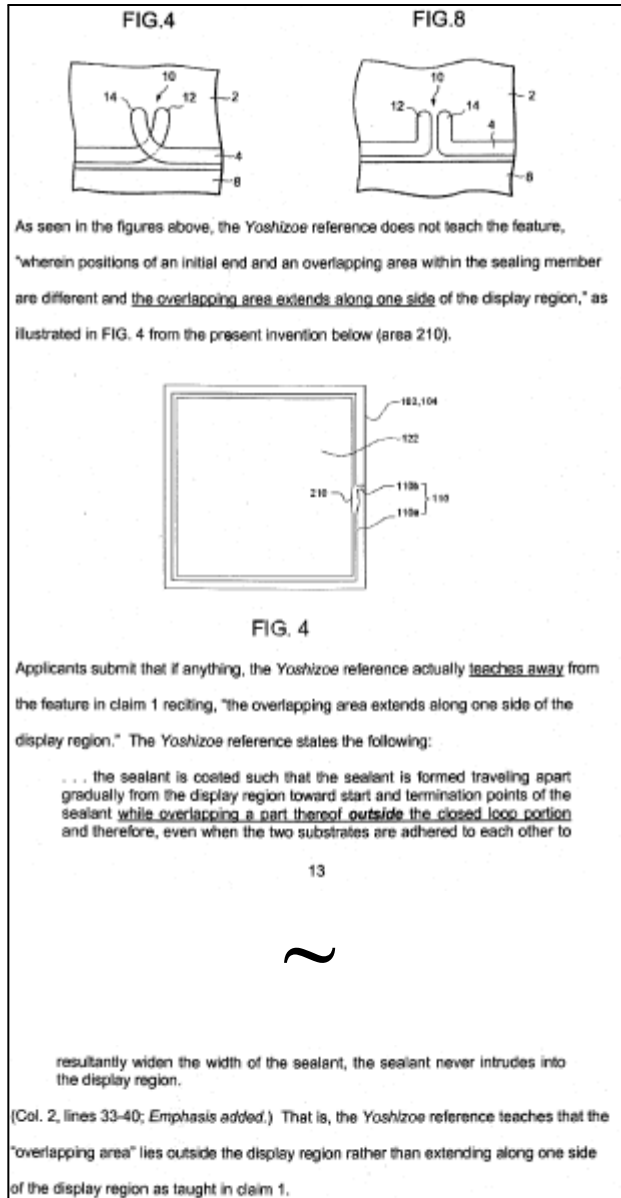
1:49-58



10b of the sealing member 110. Referring to FIG. 3, the sealing material 204 is then continued being applied along the display region 122 according to the arrow direction till forming a small overlapping area 210, thereby enclosing the display region 122 and thus forming the main portion 110a of the sealing member 110. Preferably, the main portion 110a and the protrusion part 110b of the sealing member 110 are formed at a time. Accordingly, the initial end 208 of the sealing material 204 can be kept away from the display region 122 such that the width and volume of the sealing member, especially the overlapping area 210, can be more accurately controlled and the formed sealing member 110 is not overlapped with the light-shielding matrix 114 (see FIG. 1).

4:18-31

**INTRINSIC EVIDENCE FOR DISPUTED TERM “OVERLAPPING AREA EXTENDS ALONG ONE SIDE OF THE DISPLAY REGION”**  
**(cont’d):**



**EXHIBIT 32**  
**U.S. PATENT NO. 7,280,179**  
**TERMS IN DISPUTE**

**ASSERTED CLAIM 8**

8. A liquid crystal display device including at least a backlight module and a liquid crystal display cell, wherein the liquid crystal display cell comprises:

- a first substrate;
- a second substrate;
- a liquid crystal layer sandwiched between the first substrate and the second substrate; and
- a sealing member disposed between the first and second substrates for fixing the first substrate to the second substrate, wherein the sealing member has a main portion enclosing a display region and a protrusion part extending from the main portion and the sealing member is formed by the following steps:
  - applying a sealing material to either one of a pair of substrates from a position outside of the display region toward the display region to form the protrusion part of the sealing member; and
  - continuing applying the sealing material along the display region to form the main portion of the sealing member after forming the protrusion part, wherein positions of an initial end and an overlapping area within the sealing member are different and the overlapping area extends along one side of the display region.

**LGD's Claim Construction**

**the sealing member has a main portion enclosing a display region<sup>1</sup>** – the sealing member has a portion of sealant material that is parallel to the edges of and encloses the display region

<sup>1</sup> Disputed Term “the sealing member has a main portion enclosing a display region” also appears in asserted claims 5, 11 and 15 in the same context.

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE SEALING MEMBER HAS A MAIN PORTION ENCLOSING A DISPLAY REGION”:**

A liquid crystal display cell and a method for manufacturing the same are disclosed. The method includes the following steps. First, a sealing member including a main portion enclosing a display region and a protrusion part extending from the main portion is formed. Then, a liquid crystal material is dispensed upon one of a pair of substrates, and then one substrate is superposed upon the other substrate so as to perform alignment and assembly processes. After the

Abstract, p. 1

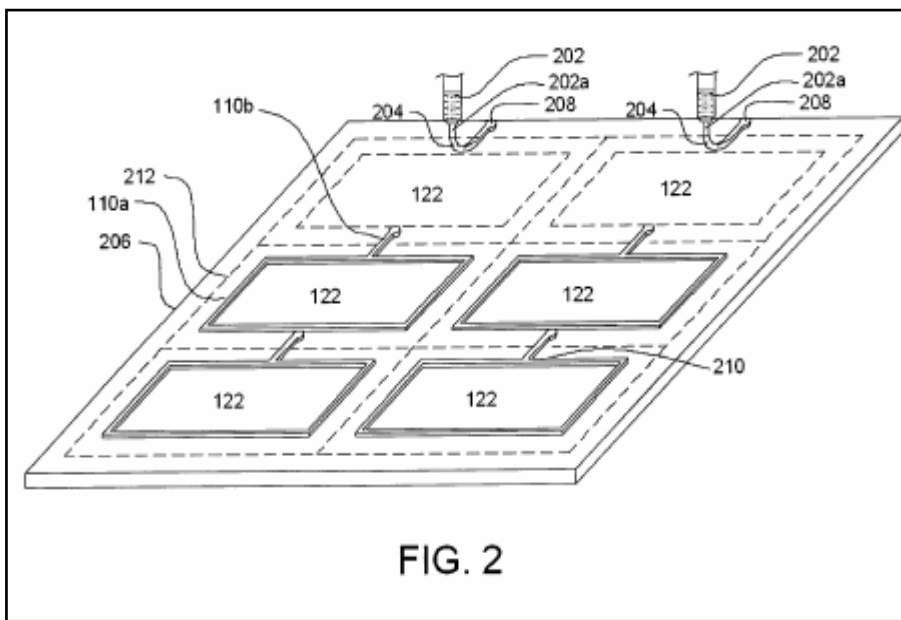
and the other substrate is covered thereupon. This technique greatly reduces the steps of a process of making LCD panels and improves manufacturing efficiencies. More specifically, the one drop fill (ODF) method includes the following steps. First, a sealant is applied to the whole periphery of one of a pair of substrates so as to form a sealing member and then a liquid crystal material is dispensed upon one of the pair of substrates. After the dispensing step, one substrate is super-

1:25-32

However, in the ODF method, the sealing member formed before the liquid crystal material being dispensed is required to fully enclose a display region of one substrate without leaving any opening thereof. When the sealing member is formed by an application manner, it is designed to have an overlapping segment between the initial end and the final end of the sealant so as to ensure that the formed sealing member can fully enclose the display region. However, the

1:49-56

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE SEALING MEMBER HAS A MAIN PORTION ENCLOSING A DISPLAY REGION” (cont’d):**



uncontrollably over-applied. Therefore, the present invention provides a novel applying method. Referring to FIG. 2, the needle 202a of the injector 202 is set to a position outside the display region 122 for starting to apply the sealing material 204, and then the sealing material 204 is applied toward the display region 122 to form the protrusion part 110b of the sealing member 110. Referring to FIG. 3, the

4:12-23

**INTRINSIC EVIDENCE FOR DISPUTED TERM “THE SEALING MEMBER HAS A MAIN PORTION ENCLOSING A DISPLAY REGION” (cont’d):**

